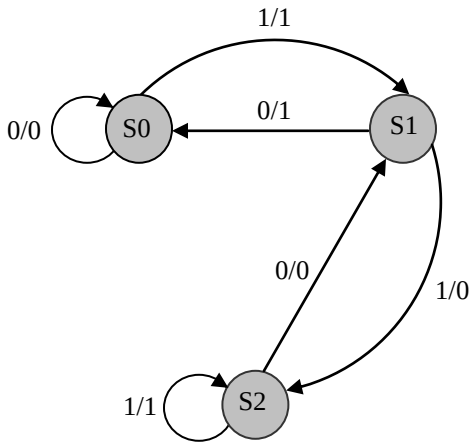
Name: KEY **Id#**

COE 202, Term 112
Digital Logic Design

Quiz# 6

Date: Monday, May 7

Q1. It is required to design a sequential circuit that receives a serial input X, and produces a serial output Z, equivalent to 3*X, i.e., Z=3*X. The state diagram for this circuit is shown below:



(i) Show the state table of the sequential circuit.

Current State	Input (X)	Next State	Output (Z)
S0	0	S0	0
S0	1	S1	1
S1	0	S0	1
S1	1	S2	0
S2	0	S1	0
S2	1	S2	1

(iii) Implement the sequential circuit using D-FFs and the smallest number of gates possible assuming the state assignment: S0=00, S1=01, and S2=10. Minimize your equations using K-map method.

(iv) Draw the circuit diagram.

We need two flip flops to implement the design F1 and F0.

Transition Table:

Current State (F1 F0)	Input (X)	Next State (F1 F0)	Output (Z)
00	0	00	0
00	1	01	1
01	0	00	1
01	1	10	0
10	0	01	0
10	1	10	1
11	0	xx	x
11	1	xx	x

	00	01	11	10
0	0	0	1	0
1	0	1	*	*

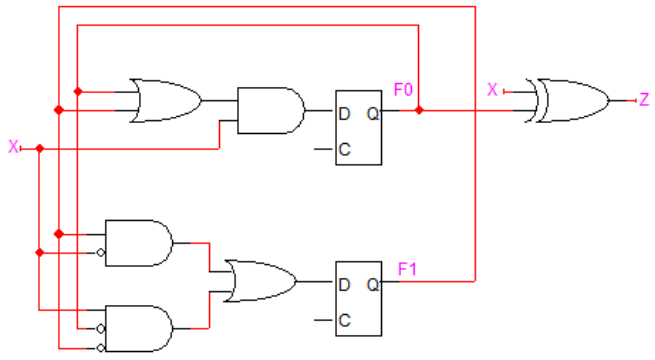
D1 = F1 X + F0 X = X (F1 + F0)

	00	01	11	10
0	0	1	0	0
1	1	0	*	*

D0 = F1 X' + F1' F0' X

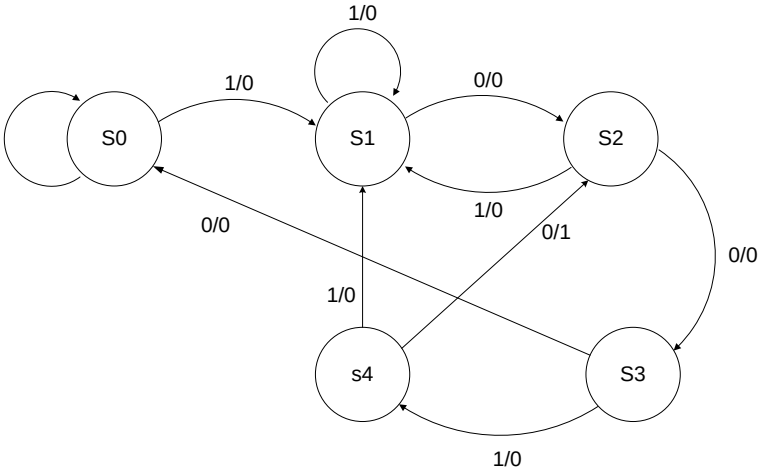
	00	01	11	10
0	0	1	0	1
1	0	1	*	*

Z = F0' X + F0 X' = F0 ⊕ X



Q2. It is required to design a sequential circuit that receives a serial input X and produces a serial output Z. The output Z will be 1 when the circuit detects the sequence 10010 assuming overlapping sequence detection.

(i) Derive the state diagram for your circuit assuming Mealy model.



(ii) Derive the state diagram for your circuit assuming Moore model.