Name: KEY Id#

COE 202, Term 122

Digital Logic Design

Quiz# 5

 Date: Monday, April 29

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# **Q1**.

* 1. Design a D-Latch using only NAND gates and inverters.



* 1. Design a D-Latch using only a 2x1 Multiplexer.



* 1. Design a **rising-edge** triggered D flip flop using only D-Latches and inverters.



# **Q2**. Design a **falling-edge** triggered JK flip flop using a **rising-edge** triggered D flip flop. Show the design steps.



**Q3**.

1. Derive the state table and state diagram for the following circuit with a single input X, and a single output Z and determine whether the circuit is Mealy or Moore:



The circuit is Mealy since the output depends on both the current state and the input.



1. Complete the following waveform for the positive-edge triggered circuit that implements the state diagram provided below. Assume the circuit is initially at the state Q1Q0 = 00.

