Name: Id#

COE 202, Term 141

Digital Logic Design

Quiz# 5

Date: Thursday, Nov. 27

# **Q1** a. Fill in all blank cells in the two tables below.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Binary | Equivalent decimal value with the binary interpreted as: | | | | |
| Unsigned number | Signed-magnitude number | Signed-1’s complement number | Signed-2’s complement number | BCD number |
| 10000000 |  |  |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| Decimal | Binary representation in 8 bits: | | |
| Signed-magnitude notation | Signed-1’s complement notation | Signed-2’s complement notation |
| - 75 |  |  |  |

b. Using 2’s-complement signed arithmetic in 5 bits, do the following operations **in binary**. Show all your work, and:

- Verify that you get the expected decimal results.

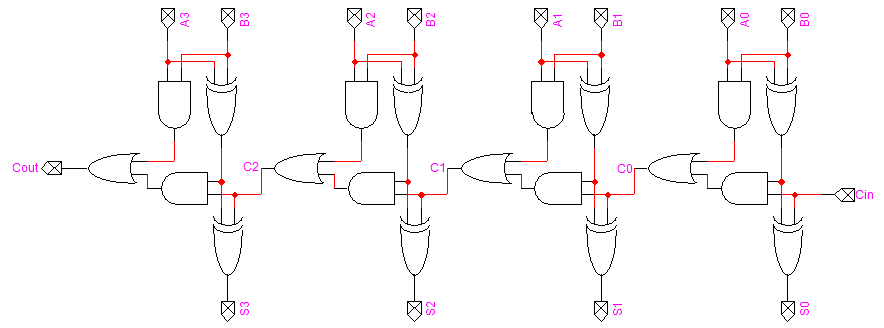
- Check for overflow and mark clearly any overflow occurrences.

|  |  |
| --- | --- |
| (i)  00111  - 10101 | (ii)  10110  - 10011 |

c. Consider the signed 2’s complement arithmetic operation A - B in 6 bits. With B = 101100, the largest value allowed for A in order to avoid the occurrence of overflow is (\_\_\_\_\_\_\_\_\_)2.

**Q2** Assume that the delay of a 2-input XOR gate is 3ns while the delay of other gates is equal to the gate’s number of inputs, i.e. the delay of an inverter is 1ns, the delay of a 2-input AND gate is 2ns, the delay of a 2-input OR is 2ns, the delay of a 3-input AND gate is 3ns, the delay of a 3-input OR gate is 3ns, etc.

1. **(6 points)** A 4-bit **Ripple Carry Adder** (RCA) is given below:



Determine and compute the **longest delay** in the **4-bit Ripple Carry Adder** (RCA).

1. **(4 points)** Show the design of a **2-bit Carry Look-Ahead Adder** (CLA) by drawing its logic diagram.
2. **(3 points)** Using the delay assumptions given in the beginning of the question, determine and compute the **longest delay** in the **2-bit Carry Look-Ahead Adder** (CLA).