Name: KEY Id#

COE 202, Term 121

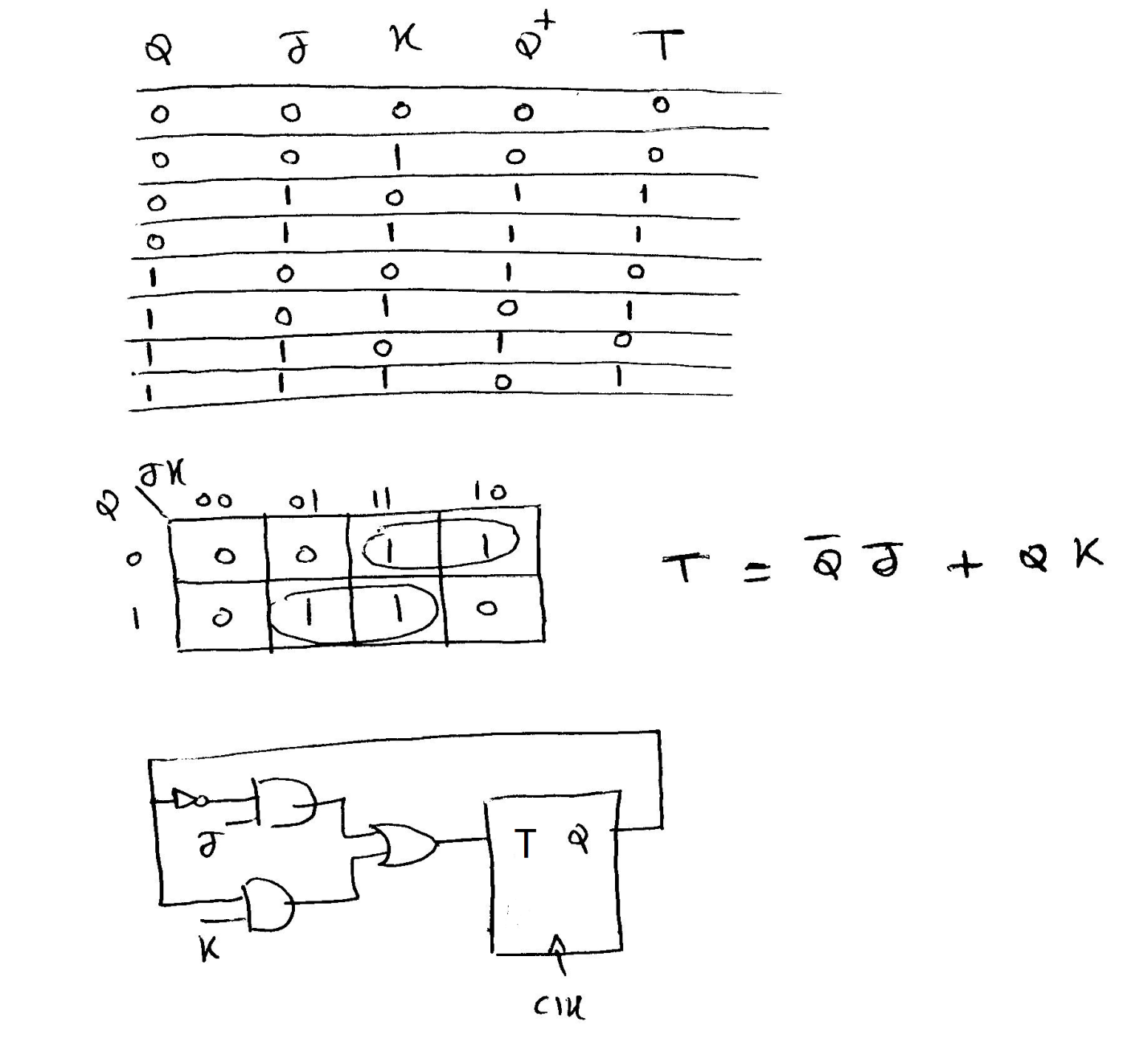
Digital Logic Design

Quiz# 4

Date: Monday, Dec. 10

# 

# **Q1**. Design a JK flip flop using a T flip flop.



# **Q2**. Given the following synchronous sequential circuit with two inputs {X, Y} and one output {Z}:

# Derive the state table of the circuit.

# Show the state diagram of the circuit.

# Is the circuit Mealy or Moore?

# Determine the output sequence for the input sequence XY={00, 01, 10, 11, 00}. Note that 00 is the start of the sequence. Assume that the machine is reset to the state 0.

