KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
*COMPUTER ENGINEERING DEPARTMENT*

COE 202 Digital Logic Design

 Term 151 Lecture Breakdown

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| **Lec#** | **Date** | **Topics** | **Ref.** |
| 1 | U23/8 | Syllabus & Course Introduction. Numbering Systems, Weighted Number Systems. The Radix, Radix Point. Binary, Octal and Hexadecimal systems. | Chapter 1 |
| 2 | T 25/8 | Important Properties. Number Base Conversion. Converting Whole (Integer) Numbers, Converting from Decimal to Other Bases, Various Methods of Conversion from Decimal to Binary. Converting Fractions. | Chapter 1 |
| 3 | TH 27/8 | Converting Fractions. Binary and Hexadecimal Addition, Subtraction. | Chapter 1 |
| 4 | U 30/8 | Binary and Hexadecimal Addition, Subtraction, Binary and Hexadecimal Multiplication. Binary Codes for Decimal Digits. Character Storage, ASCII Code. | Chapter 1 |
| 5 | T 1/9 | Error Detection, Parity Bit. Elements of Boolean Algebra (Binary Logic), Logic Gates & Logic Operations. Boolean Algebra. | Chapter 1 & 2.2 |
| 6 | TH 3/9 | Basic Identities of Boolean Algebra, Duality Principle, Operator Precedence. Properties of Boolean Algebra. Algebraic Manipulation. | 2.2-2.4 & 2.7 |
| 7 | U 6/9 | Algebraic Manipulation. **(Quiz#1)** | 2.7 |
| 8 | T 8/9 | Minterms, Expressing Functions as a Sum of Minterms. Canonical Forms. Maxterms | 2.7 & 2.5 |
| 9 | TH 10/9 | Expressing Functions as a Product of Maxterms. Operations on functions based on operations on minterms, Canonical Forms. Standard Forms, Two-Level Implementations of Standard Forms. | 2.5 |
| 10 | U 13/9 | Propagation delay, Timing Diagrams, Critical Path. Introduction to Verilog: Verilog Syntax, Definition of a Module, Gate Level Modeling. |  |
| 11 | T 15/9 | Introduction to Verilog: Verilog Syntax, Definition of a Module, Gate Level Modeling, Module Instantiation, Propagation Delay, Boolean Equation-Based Behavioral Models of Combinational Logic, Assign Statement, Propagation Delay & Continuous Assignment, Test Bench Example. |  |
| 12 | TH 17/9 | Using Modelsim simulation tool. **(Quiz#2)** |  |
|  | 18/9-4/10 | **Id al-Adha Vacation** |  |
| 13 | U 4/10 | ***Map method of simplification***: Two-, Three-and Four-variable K-Map. Implicants, Prime Implicants. | 3.1-3.4 |
| 14 | T 6/10 | Prime Implicants. Essential Prime Implicants. Simplification procedure. Don’t Care Conditions. | 3.1-3.4 |
| 15 | TH 8/10 | Simplification procedure using Don’t Cares. POS simplification | 3.1-3.4 |
|  | S 10/10 | **Major Exam I** |  |
| 16 | U 11/10 | Five-variable K-map simplification. Six-variable K-map simplification. Types of gates: primitive vs. complex gates. | 3.3-3.5 |
| 17 | T 13/10 | Buffer & Tri-state buffer, Nand gate, Nor gate, NAND as a universal gates. Two-Level Implementation using Nand gates, NOR as a universal gates Two-Level Implementation using NOR gates. Implementing circuits using Nand/Nor gates. | 2.6, 2.8 |
| 18 | TH 15/10 | Complex Gates, Exclusive OR (XOR) Gate, Exclusive NOR (XNOR) Gate, XOR Implementations, Properties of XOR/XNOR Operations. XOR/XNOR for >2 Variables. The Odd & Even Functions. | 2.6, 2.8 |
|  | TH 15/10 | **Last Day for Dropping with W** |  |
| 19 | U 18/10 | Parity Generation and Checking. Combinational Logic Circuits, Combinational Circuits Design Procedure. Y=X^2 design example.BCD to Excess-3 code conversion. BCD to 7-Segment Decoder for LED. Iterative Arithmetic Combinational Circuits. | 5.1 |
| 20 | T 20/10 | Iterative Magnitude Comparator. Adder Design. Half Adder, Full Adder, 4-bit Ripple Carry Adder. | 5.1 |
| 21 | TH 22/10 | Iterative Design Examples: Y=X+1, Y=X-Y, Y=3\*X,  | 5.1 |
| 22 | U 25/10 | **(Quiz#3)** |  |
| 23 | T 27/10 | 4-bit RCA: Carry Propagation & Delay. Representation of signed numbers: sign-magnitude. | 1.2.3-1.24 & 5.1.2-5.1.3 & 5.8 |
|  | W 28/10(Makeup) | Representation of signed numbers: sign-magnitude, 1`s complement, and 2`s complement. Overflow detection, Adder/Subtractor for Signed 2’s Complement. | 1.2.3-1.24 & 5.1.2-5.1.3 & 5.8 |
| 24 | TH 29/10 | Overflow detection, Enabling Function, Decoders. Implementing Functions using Decoders. | 5.2-5.4 |
| 25 | U 1/11 | Implementing Functions using Decoders. Hierarchical design of decoders. **Encoders**: Priority Encoders. Applications of decoders and encoders. | 5.2-5.4 |
| 26 | T 3/11 | **(Quiz#4)** |  |
| 27 | TH 5/11 | No Class |  |
| 28 | U 8/11 | **Multiplexers:** 2x1, 4x1. Function implementation using multiplexers. Arithmetic unit design. | 5.2-5.4 |
| 29 | T 10/11 | Function implementation using multiplexers, Constructing large MUXs from smaller ones. Demultiplexer. Design Examples using MSI Functional Blocks. Absolute Value of a number, Selecting the larger of two 4-bit numbers (unsigned & signed). | 5.4 & 5.8 |
| 30 | TH 12/11 | Adding Three 4-bit numbers, Multiplication and division by a constant. Introduction to Verilog: Verilog Operators. | 5.4 & 5.8 |
|  | TH 12/11 | **Last Day for Dropping all Courses with W** |  |
| 31 | U 15/11 | Introduction to Verilog: Verilog Operators, Behavioral Description of an Adder, Always block, Procedural Assignment. |  |
| 32 | T 17/11 | If Statements, Case Statements, Comparator, Arithmetic & Logic Unit. Multiplexor, Encoder, Priority Encoder. |  |
| 33 | TH 19/11 | Decoder, Seven Segment Display Decoder. Introduction to Sequential Circuits. Synchronous vs asynchronous sequential circuits, NOR Set–Reset (SR) Latch. NAND Set–Reset (SR) Latch. Clocked (or controlled) D Latch. | 6.1-6.3 |
|  | S 21/11 | **Major Exam II** |  |
| 34 | U 22/11 | Timing Problem of the transparent Latch. Flip flops, Edge-Triggered D-type Flip-Flop. Synchronous and asynchronous reset. Verilog modeling of D-latch & D-FF. | 6.1-6.3 |
| 35 | T 24/11 | Flip-Flop Timing Parameters: Setup and hold times, flip-flop propagation delay. Speed of sequential circuit. | 6.1-6.3 |
| 36 | TH 26/11 | Sequential Circuit Analysis: One-Dimensional State Table. | 6.4 |
| 37 | U 29/11 | Two-Dimensional State Table, Sate Diagram. Moore and Mealy Models. Analysis of sequential circuit. Implementation and Design of Sequential Circuits. | 6.4 & 7.4 |
| 38 | T 1/12 | Analysis of sequential circuit. Implementation and Design of Sequential Circuits. | 6.4 & 7.4 |
| 39 | TH 3/12 | Sequential Circuit Design Examples: Y=X-1, Z=2X-Y, Sequence Detector, Password Detection, Sequential Comparator, BCD-to-excess-3 code conversion. | 7.4 |
| 40 | U 6/12 | Verilog modeling of D-Latch, D Flip Flop – Synchronous Set/Reset, D Flip Flop–Asynchronous Set/Reset. Verilog Structural modeling of sequential circuits, Verilog FSM modeling, Registers, 4-bit Register, with Clear & Selective Parallel Load by clock gating, Avoiding clock gating. Shift Registers. | 8.1 |
| 41 | T 8/12 | Shift Register Applications. Linear Feedback Shift Register (LFSR). Designing Synchronous Counters using FSMs. Designing Synchronous Counters using registers and adder. Up-Down Synchronous Counter with Enable & Parallel Load. Synchronous Counters. Building Large counters from Small counters. | 8.2 |
| 42 | TH 10/12 | **(Quiz#5)** |  |
|  | TH 10/12 | **Dropping all Courses with WP/WF** |  |
| 43 | U 13/12 | Modulo counters. Counters as Frequency Dividers. | 8.2 |
| 44 | T 15/12 | Verilog modeling of: Parallel Load Register, Shift Register, Up-Down Counter. Read Only Memory (ROM), Combinational Circuit implementation using ROMs. | 5.6 |
| 45 | TH 17/12 | Sequential Circuit implementation using ROMs. Programmable Implementation Technologies: Overview, Why Programmable Logic? Programmable Logic Configurations: ROM. | 5.6 |