KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 202 Digital Logic Design

Term 142 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	T 27/1	Syllabus & Course Introduction. Information Processing and representation. Digital vs. Analog quantities. Digitization of Analog signals. Minimizing Quantization Error.	
2	TH 29/1	Digital representation of information. Effect of noise on the reliability and choice of digital system, Maximizing Noise Margin. Numbering Systems, Weighted Number Systems. The Radix, Radix Point. Binary, Octal and Hexadecimal systems. Important Properties.	Chapter 1
3	U 1/2	Number Base Conversion. Converting Whole (Integer) Numbers, Converting from Decimal to Other Bases, Various Methods of Conversion from Decimal to Binary. Converting Fractions.	Chapter 1
4	T 3/2	Binary and Hexadecimal Addition, Subtraction, Binary and Hexadecimal Multiplication. Binary Codes for Decimal Digits.	Chapter 1
5	TH 5/2	Character Storage, ASCII Code. Error Detection, Parity Bit. Elements of Boolean Algebra (Binary Logic), Logic Gates & Logic Operations.	Chapter 1 & 2.2
6	U 8/2	Logic Gates & Logic Operations. Boolean Algebra, Basic Identities of Boolean Algebra, Duality Principle, Operator Precedence. Properties of Boolean Algebra. Algebraic Manipulation.	2.2-2.4 & 2.7
7	T 10/2	Algebraic Manipulation. **(Quiz#1)**	2.2-2.4 & 2.7
8	TH 12/2	Algebraic Manipulation. Minterms, Expressing Functions as a Sum of Minterms,	2.7 & 2.5
9	U 15/2	Expressing Functions as a Sum of Minterms, Maxterms, Expressing Functions as a Product of Maxterms.	2.5
10	T 17/2	Operations on functions based on operations on minterms, Canonical Forms. Standard Forms,	2.5

		Two-Level Implementations of Standard Forms.	
11	TH 19/2	Allowed Voltage Levels, Input & Output Voltage Ranges, Noise Margin. Propagation Delay. Timing Diagrams.	
12	U 22/2	Critical Path (Quiz#2)	
13	T 24/2	Fanin Limitations, Fanout Limitations. Use of High-Drive Buffers, Use of Multiple Drivers. Gates with Tri-State Outputs.	
14	TH 26/2	Introduction to Verilog: Verilog Syntax, Definition of a Module, Gate Level Modeling, Using Modelsim simulation tool.	
	S 28/2	**Major Exam I**	
15	U 1/3	Introduction to Verilog: Module Instantiation, Propagation Delay, Test Bench Example, Behavioral Modeling, Boolean Equation-Based Behavioral Models of Combinational Logic, Assign Statement, Verilog Operators	
16	T 3/3	Introduction to Verilog: Verilog Operators, Propagation Delay & Continuous Assignment, Behavioral Description of an Adder. *Map method of simplification*: Two-, and Three-variable K-Map.	3.1
	TH 5/3	**Last Day for Dropping with W**	
17	TH 5/3	*Map method of simplification*: Three-variable K-Map, Four-variable K-Map. Implicants, Prime Implicants. Essential Prime Implicants. Simplification procedure.	3.1-3.4
18	U 8/3	Simplification procedure. POS simplification.	3.3-3.5
19	T 10/3	Don't Care Conditions, Simplification procedure using Don't Cares. Five-variable K-map simplification. Six-variable K-map simplification.	3.3-3.5
20	TH 12/3	Types of gates: primitive vs. complex gates. Buffer & Tri-state buffer, Nand gate, Nor gate, NAND as a universal gates, Two-Level Implementation using Nand gates, NOR as a universal gates Two-Level Implementation using NOR gates. Implementing circuits using Nand/Nor gates.	2.6, 2.8
21	U 15/3	Complex Gates, Exclusive OR (XOR) Gate, Exclusive NOR (XNOR) Gate, XOR Implementations, Properties of XOR/XNOR Operations. XOR/XNOR for >2 Variables. The Odd & Even Functions. Parity Generation and Checking.	2.6, 2.8

22	T 17/3	Combinational Logic Circuits, Combinational Circuits Design Procedure. Y=X^2 design example. **(Quiz#3)**	5.1
23	TH 19/3	BCD to Excess-3 code conversion. BCD to 7-Segment Decoder for LED. Hierarchical Design, Iterative Arithmetic Combinational Circuits.	5.1
	20-28/3	**MIDTERM VACATION**	
24	U 29/3	Iterative Magnitude Comparator. Adder Design. Half Adder, Full Adder, 4-bit Ripple Carry Adder.	5.1
25	T 31/3	Iterative Y=3*x, Subtractor Design. 4-bit RCA: Carry Propagation & Delay.	5.1
26	TH 3/4	**(Quiz#4)**	
27	S 4/4	Representation of signed numbers: sign-magnitude, 1`s complement, and 2`s complement.	1.2.3-1.24 & 5.1.2-5.1.3 & 5.8
28	U 5/4	Overflow detection, Adder/Subtractor for Signed 2's Complement.	1.2.3-1.24 & 5.1.2-5.1.3 & 5.8
29	T 7/4	Review of signed number representation. Binary Multiplier.	1.2.3-1.24 & 5.1.2-5.1.3 & 5.8
	W 8/4	Enabling Function, Decoders. Implementing Functions using Decoders. Hierarchical design of decoders. **Encoders**: Priority Encoders.	5.2-5.4
	TH 9/4	**Last Day for Dropping all Courses with W**	
30	TH 9/4	**Multiplexers:** 2x1, 4x1. Constructing large MUXs from smaller ones. Function implementation using multiplexers.	5.2-5.4
31	U 12/4	Demultiplexer, Design Examples using MSI Functional Blocks. Arithmetic unit design, Absolute Value of a number, Multiplication and division by a constant. Selecting the larger of two 4-bit numbers (unsigned & signed). Adding Three 4-bit numbers.	5.4 & 5.8
32	T 14/4	Adding two 16-bit numbers using 4-bit adders, Building 4-to-16 Decoders using 2-to-4 Decoders with Enable, BCD-toExcess3 code conversion using decoder-encoder. Review of decoders, encoders and multiplexers.	5.4 & 5.8
33	TH 16/4	Introduction to Verilog: Lecture 3: Always block, Procedural Assignment, If Statements, Case Statements, Comparator, Arithmetic & Logic Unit	
	S 18/4	**Major Exam II**	
34	U 19/4	Introduction to Verilog: Lecture 3: Multiplexor, Encoder, Priority Encoder, Decoder, Seven Segment Display Decoder.	

35	T 21/4	Introduction to Sequential Circuits. Synchronous vs asynchronous sequential circuits, NOR Set–Reset (SR) Latch. NAND Set–Reset (SR) Latch.	6.1-6.3
36	TH 23/4	Clocked (or controlled) D Latch. Timing Problem of the transparent Latch. Flip flops, Edge-Triggered D-type Flip-Flop.	6.1-6.3
37	U 26/4	Synchronous and asynchronous reset. Sequential Circuit Analysis: One-Dimensional State Table. Two-Dimensional State Table, Sate Diagram. Moore and Mealy Models. Analysis of sequential circuit.	6.4
38	T 28/4	Analysis of sequential circuit examples.	6.4
39	TH 30/4	Sequential Circuit Design Procedure, sequence detector (overlapping vs non-overlapping). Sequential Circuit Implementation examples: Sequence detector, 2's complement.	7.4
40	U 3/5	Sequential Circuit Design Examples: Y=3*X, Y=3*X+1, Y=3*X-1, Sequential Subtractor, Sequential Comparator.	7.4
41	T 5/5	Sequential Circuit Design Examples: Password detection, BCD-to-excess-3 code conversion. **(Quiz#5)**	7.4
	TH 7/5	**Dropping all Courses with WP/WF**	
42	TH 7/5	Flip-Flop Timing Parameters: Setup and hold times, flip-flop propagation delay. Speed of sequential circuit. Verilog modeling of D-Latch, D Flip Flop – Synchronous Set/Reset, D Flip Flop–Asynchronous Set/Reset.	6.1-6.3
43	U 10/5	Verilog Structural modeling of sequential circuits, Verilog FSM modeling, Registers, 4-bit Register, with Clear & Selective Parallel Load by clock gating, Avoiding clock gating. Shift Registers. Shift Register Applications.	8.1
44	T 12/5	Linear Feedback Shift Register (LFSR). Designing Synchronous Counters using FSMs. Designing Synchronous Counters using registers and adder.	8.2
45	TH 14/5	Up-Down Synchronous Counter with Enable & Parallel Load. Synchronous Counters. Building Large counters from Small counters. Modulo counters. Counters as Frequency Dividers. Verilog modeling of: Parallel Load Register, Shift Register, Up-Down Counter	8.2