KING FAHD UNIVERSITY OF PETROLEUM & MINERALS  
*COMPUTER ENGINEERING DEPARTMENT*

COE 202 Digital Logic Design

Term 141 Lecture Breakdown

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| **Lec#** | **Date** | **Topics** | **Ref.** |
| 1 | U 31/8 | Syllabus & Course Introduction. Information Processing and representation. Digital vs. Analog quantities. Digitization of Analog signals. Minimizing Quantization Error. |  |
| 2 | T 2/9 | Minimizing Quantization Error, Digital representation of information. Effect of noise on the reliability and choice of digital system, Maximizing Noise Margin. Numbering Systems, Weighted Number Systems. | Chapter 1 |
| 3 | TH 4/9 | Weighted Number Systems, the Radix, Radix Point. Binary, Octal and Hexadecimal systems. Important Properties. Number Base Conversion. | Chapter 1 |
| 4 | U 7/9 | Converting Whole (Integer) Numbers, Converting from Decimal to Other Bases, Various Methods of Conversion from Decimal to Binary. Converting Fractions. | Chapter 1 |
| 5 | T 9/9 | Binary and Hexadecimal Addition, Subtraction, Binary and Hexadecimal Multiplication. Binary Codes for Decimal Digits. | Chapter 1 |
| 6 | TH 11/9 | Binary Codes for Decimal Digits, Character Storage, ASCII Code. Error Detection, Parity Bit. Elements of Boolean Algebra (Binary Logic), Logic Gates & Logic Operations. | Chapter 1 & 2.2 |
| 7 | U 14/9 | Boolean Algebra, Basic Identities of Boolean Algebra, Duality Principle, Operator Precedence. Properties of Boolean Algebra. Algebraic Manipulation. | 2.2-2.4 & 2.7 |
| 8 | T 16/9 | Algebraic Manipulation. **(Quiz#1)** | 2.2-2.4 & 2.7 |
| 9 | TH 18/9 | Minterms, Expressing Functions as a Sum of Minterms, Maxterms, Expressing Functions as a Product of Maxterms. | 2.5 |
| 10 | U 21/9 | Canonical Forms. Standard Forms, Two-Level Implementations of Standard Forms. Allowed Voltage Levels, Input & Output Voltage Ranges, Noise Margin. Propagation Delay. | 2.5 |
|  | T 23/9 | National Day - Holiday |  |
| 11 | TH 25/9 | Timing Diagrams. Fanin Limitations, Fanout Limitations. Use of High-Drive Buffers, Use of Multiple Drivers. Gates with Tri-State Outputs. |  |
|  | 26/9 – 11/10 | Id al-Adha Vacation |  |
| 12 | U 12/10 | Gates with Tri-State Outputs. ***Map method of simplification***: Two-, and Three-variable K-Map. | 3.1 |
| 13 | T 14/10 | ***Map method of simplification***: Three-variable K-Map, Four-variable K-Map. Implicants, Prime Implicants. Essential Prime Implicants. Simplification procedure. | 3.1-3.4 |
| 14 | TH 16/10 | **(Quiz#2)** |  |
|  | S 18/10 | **Major Exam I** |  |
| 15 | U 19/10 | Simplification procedure. POS simplification. | 3.3-3.5 |
| 16 | T 21/10 | Don’t Care Conditions, Simplification procedure using Don’t Cares. | 3.3-3.5 |
| 17 | TH 23/10 | Five-variable K-map simplification. Six-variable K-map simplification. | 3.3-3.5 |
|  | TH 23/10 | **Last Day for Dropping with W** |  |
| 18 | U 26/10 | Types of gates: primitive vs. complex gates. Buffer & Tri-state buffer, Nand gate, Nor gate, XOR, XNOR gates. | 2.6, 2.8 |
| 19 | T 28/10 | NAND as a universal gates Two-Level Implementation using Nand gates. **(Quiz#3)** | 2.6, 2.8 |
| 20 | TH 30/10 | NOR as a universal gates Two-Level Implementation using NOR gates. Implementing circuits using Nand/Nor gates, Complex Gates, Exclusive OR (XOR) Gate, Exclusive NOR (XNOR) Gate | 2.6, 2.8 |
| 21 | U 2/11 | Complex Gates, Exclusive OR (XOR) Gate, Exclusive NOR (XNOR) Gate, XOR Implementations, Properties of XOR/XNOR Operations. XOR/XNOR for >2 Variables. The Odd & Even Functions. | 2.6, 2.8 |
| 22 | T 4/11 | Parity Generation and Checking. Combinational Logic Circuits, Combinational Circuits Design Procedure. BCD to Excess-3 code conversion. Tutorial on using LogicWorks for simulating circuits. | 2.1 & 5.1 |
| 23 | TH 6/11 | BCD to 7-Segment Decoder for LED. Hierarchical Design, Iterative Arithmetic Combinational Circuits. Adder Design. Half Adder, Full Adder, 4-bit Ripple Carry Adder. Iterative Magnitude Comparator. | 5.1 |
| 24 | U 9/11 | Design Examples: Subtractor, Y=3\*X. 4-bit RCA: Carry Propagation & Delay | 5.1 |
| 25 | T 11/11 | 4-bit RCA: Carry Propagation & Delay, Carry Look-ahead Adder, Delay for the 4-bit CLA Adder. (Building a device symbol in LogicWorks) | 5.1 |
| 26 | TH 13/11 | Representation of signed numbers: sign-magnitude, 1`s complement, and 2`s complement. | 1.2.3-1.2.4 & 5.1.2-5.1.3 |
| 27 | U 16/11 | overflow detection, Adder/Subtractor for Signed 2’s Complement.. BCD Adder. Binary Multiplier. | 1.2.3-1.24 & 5.1.2-5.1.3 & 5.8 |
| 28 | T 18/11 | Enabling Function, Decoders. Implementing Functions using Decoders. Hierarchical design of decoders. **Encoders**: Priority Encoders. | 5.2-5.4 |
| 29 | TH 20/11 | **Encoders**: Priority Encoders. **Multiplexers:** 2x1, 4x1. Constructing large MUXs from smaller ones. Function implementation using multiplexers. **(Quiz#4)** | 5.2-5.4 |
|  | TH 20/11 | **Last Day for Dropping all Courses with W** |  |
| 30 | U 23/11 | Demultiplexer, Design Examples using MSI Functional Blocks. Arithmetic unit design, Absolute Value of a number, Multiplication and division by a constant. | 5.4 & 5.8 |
| 31 | T 25/11 | Design Examples using MSI Functional Blocks: Adding Three 4-bit numbers, Adding two 16-bit numbers using 4-bit adders, Building 4-to-16 Decoders using 2-to-4 Decoders with Enable, Selecting the larger of two 4-bit numbers (unsigned & signed). | 5.4 & 5.8 |
| 32 | TH 27/11 | BCD-toExcess3 code conversion using decoder-encoder. **(Quiz#5)** | 5.4 & 5.8 |
|  | S 29/11 | **Major Exam II** |  |
| 33 | U 30/11 | Introduction to Sequential Circuits. Synchronous vs asynchronous sequential circuits, Mealy vs Moore model, NOR Set–Reset (SR) Latch. | 6.1-6.3 |
| 34 | T 2/12 | NOR Set–Reset (SR) Latch. NAND Set–Reset (SR) Latch, Clocked (or controlled) D Latch. Timing Problem of the transparent Latch. | 6.1-6.3 |
| 35 | TH 4/12 | Flip flops, Edge-Triggered D-type Flip-Flop. Flip-Flop Timing Parameters: Setup and hold times, flip-flop propagation delay. | 6.1-6.3 |
| 36 | U 7/12 | Flip-Flop Timing Parameters: Setup and hold times, flip-flop propagation delay. Speed of sequential circuit. Synchronous and asynchronous reset. | 6.1-6.3 |
| 37 | T 9/12 | Sequential Circuit Analysis: One-Dimensional State Table. Two-Dimensional State Table, Sate Diagram. Moore and Mealy Models. Analysis of sequential circuit (Moore model). | 6.4 |
| 38 | TH 11/12 | Analysis of sequential circuit examples. Sequential Circuit Design Procedure, sequence detector (overlapping vs non-overlapping, Mealy vs Moore). | 6.4 & 7.4 |
| 39 | U 14/12 | Sequential Circuit Implementation examples: Sequence detector, serial adder, 2’s complement | 7.4 |
| 40 | T 16/12 | Sequential Circuit Design Examples: Sequential Comparator, Y=3\*X+1, Y=3\*X-1, BCD-to-excess-3 code conversion. | 7.4 |
| 41 | TH 18/12 | Registers, 4-bit Register, with Clear & Selective Parallel Load by clock gating, Avoiding clock gating. Shift Registers. Shift Register Applications. Linear Feedback Shift Register (LFSR). | 8.1 |
|  | TH 18/12 | **Dropping all Courses with WP/WF** |  |
| 42 | U 21/12 | Designing Synchronous Counters using FSMs, Up-Down Synchronous Counter with Enable & Parallel Load. Synchronous Counters. Building Large counters from Small counters. Modulo counters. Counters as Frequency Dividers. | 8.2 |
| 43 | T 23/12 | Ripple Counter (Asynchronus). Programmable Implementation Technologies: Overview, Why Programmable Logic? Programmable Logic Configurations: ROM, PAL and PLA Configurations, Read Only Memory (ROM). | 8.2 & 5.6 |
| 44 | TH 25/12 | Sequential Circuit implementation using ROMs. Programmable Array Logic (PAL), Programmable Logic Array (PLA). **(Quiz#6)** | 5.6 |
| 45 | U 28/12 | Final Exam Review. |  |