KING FAHD UNIVERSITY OF PETROLEUM & MINERALS  
*COMPUTER ENGINEERING DEPARTMENT*

COE 202 Digital Logic Design

Term 102 Lecture Breakdown

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| **Lec#** | **Date** | **Topics** | **Ref.** |
| 1 | S 12/2 | Syllabus & Course Introduction. |  |
| 2 | M 14/2 | Information Processing and representation. Digital vs Analog quantities, Digitization of Analog signals, Digital representation of information, Effect of noise on the reliability and choice of digital system. | 1.1 |
| 3 | W 16/2 | Numbering Systems, Weighted Number Systems, the Radix, the Radix Point, Binary, Octal and Hexadecimal systems, Important Properties. | 1.2 |
| 4 | S 19/2 | Number Base Conversion, Converting Whole (Integer) Numbers, Converting from Decimal to Other Bases, Various Methods of Conversion from Decimal to Binary. Conversion between binary, Octal and Hexadecimal. | 1.3 |
| 5 | M 21/2 | Converting Fractions, Binary Addition, Subtraction and Multiplication, Hexadecimal Addition and Subtraction, Character Storage, ASCII Code, Error Detection, Parity Bit. | 1.3-1.6 |
| 6 | W 23/2 | Elements of Boolean Algebra (Binary Logic), Logic Gates & Logic Operations, Boolean Algebra, Basic Identities of Boolean Algebra, Duality Principle, Operator Precedence. Properties of Boolean Algebra, Algebraic Manipulation. | 2.1, 2.2 |
| 7 | S 26/2 | **No Class.** |  |
| 8 | M 28/2 | Algebraic Manipulation. (**Quiz#1**) | 2.2 |
| 9 | W 2/3 | MinTerms, MaxTerms, Expressing Functions as a Sum of Minterms. | 2.3 |
| 10 | S 5/3 | Functions as a Product of Maxterms, Canonical Forms, Standard Forms, Two-Level Implementations of Standard Forms. Allowed Voltage Levels, Input & Output Voltage Ranges, Noise Margin. | 2.3 & 2.9 |
| 11 | M 7/3 | Propagation Delay, Timing Diagrams, Fanin Limitations, Fanout Limitations, Use of High-Drive Buffers, Use of Multiple Drivers, Gates with Tri-State Outputs. | 2.10, 6.1, 6.2 |
| 12 | W 9/3 | ***Map method of simplification***: Two-, and Three-variable K-Map. Implicants, Prime Implicants, Essential Prime Implicants. Simplification procedure. | 2.4, 2.5 |
| 13 | S 12/3 | No Class. |  |
| 14 | M 14/3 | ***Map manipulation:*** BCD code, Four-variable k-map. (**Quiz#2**) | 2.4, 2.5 |
| 15 | W 16/3 | Don’t Care Conditions, SOP Simplification procedure using Don’t Cares. | 2.5 |
|  | W 16/3  (Makeup) | Review for Major Exam 1. |  |
|  | Th. 17/3 | **Major Exam I** |  |
| 16 | S 19/3 | Holiday. |  |
| 17 | M 21/3 | POS simplification, Five-variable & six-variable K-map simplification. Types of gates: primitive vs. complex gates. | 2.5 & 2.7 |
| 18 | W 23/3 | Buffer & Tri-state buffer, Nand gate, Nor gate, universal gates, Two-Level Implementation using Nand/Nor gates. | 2.7 |
|  | W 23/3 | **Last Day for Dropping with W** |  |
| 19 | S 26/3 | No Class. |  |
| 20 | M 28/3 | Complex Gates, Exclusive OR (XOR) Gate, Exclusive NOR (XNOR) Gate, XOR Implementations, Properties of XOR/XNOR Operations, XOR/XNOR for >2 Variables: The Odd & Even Functions, Parity Generation and Checking. Combinational Logic Circuits, Combinational Circuits Design Procedure. | 2.8 & 3.1 |
| 21 | W 30/3 | BCD to Excess 3 Code Converter, BCD to 7-Segment Decoder for LED, Hierarchical Design, Iterative Arithmetic Combinational Circuits, Adder Design. | 3.1-3.2 |
| 22 | S 2/4 | Half Adder, Full Adder, 4-bit Ripple Carry Adder, 4-bit RCA: Carry Propagation & Delay, Carry Lookahead Adder, Delay for the 4-bit CLA Adder, Signed Number Representation. | 4.1-4.4 |
|  | S 2/4 (Makeup) | Introduction to Logic Works & WinLogiLab |  |
| 23 | M 4/4 | Representation of signed numbers: sign-magnitude, 1`s complement, and 2`s complement. | 4.3-4.4 |
| 24 | W 6/4 | Adder/Subtractor for Signed 2’s Complement, BCD Adder, Binary Multiplier, Enabling Function, Decoders, Implementing Functions using Decoders. | 3.7, 4.3, 4.4 |
|  | 9-13/4 | **Midterm Vacation** |  |
| 25 | S 16/4 | **Encoders**: Priority Encoders. (**Quiz#3**) | 3.8 |
| 26 | M 18/4 | **Multiplexers:** 2x1, 4x1. Constructing large MUXs from smaller ones.Function implementation using multiplexers. | 3.9 |
| 27 | W 20/4 | No Class. |  |
| 28 | S 23/4 | Demultiplexer, Design Examples using MSI Functional Blocks: Adding Three 4-bit numbers, Adding two 16-bit numbers using 4-bit adders, Building 4-to-16 Decoders using 2-to-4 Decoders with Enable, Modular Magnitude Comparator, Selecting the larger of two 4-bit numbers, Absolute Value of a number. | 3.7-3.9 |
|  | S 23/4  (Makeup) | BCD to Excess-3 Code Converter using a decoder and straight binary encoder, ALU design, Multiplication and division by constants, Shifter Design, Sequential Circuits, Concept of memory elements, Nor-Nor SR-Latch. | 5.1 & 5.2 |
| 29 | M 25/4 | Introduction to Sequential Circuits, Types of sequential circuits: Synchronous vs. Asynchronous, NOR Set–Reset (SR) Latch, NAND Set–Reset (SR) Latch, Clocked (or controlled) SR NAND Latch, D Latch. | 5.1 & 5.2 |
| 30 | W 27/4 | Review for Major Exam II |  |
|  | W 27/4 | **Last Day for Dropping all Courses with W** |  |
|  | Th. 28/4 | **Major Exam II** |  |
| 31 | S 30/4 | Timing Problem of the transparent Latch, Flip flops, S-R Master-Slave (Pulse-Triggered) Flip-Flop, Problems with the S-R Master-Slave Flip-Flop, Edge-Triggered D-type Flip-Flop. | 5.3 |
| 32 | M 2/5 | Solution of Major Exam II. |  |
| 33 | W 4/5 | Flip-Flop Timing Parameters: Setup and hold times, flip-flop propagation delay. Standard Symbols for Storage Elements, Asynchronous vs. Synchronous reset, Other types of FFs: JK and T flip-flops. | 6.3 & 5.6 |
| 34 | S 7/5 | Characteristic table, Characteristic equation, Excitation table, Designing flip-flops using other flip-flops, Sequential Circuit Analysis. | 5.4 & 5.6 |
| 35 | M 9/5 | Sequential Circuit Analysis: One-Dimensional State Table, Two-Dimensional State Table, Sate Diagram, Moore and Mealy Models. Synchronizing sequence. | 5.4 |
| 36 | W 11/5 | Sequential Circuit Design Procedure, Bit Sequence Recognizer, Mealy vs. Moore Design. Serial Adder Design. | 5.5 |
| 37 | S 14/5 | (**Quiz#6**) Two sequence detections design example. | 5.5 |
| 38 | M 16/5 | Sequential Circuit Design of 3\*X Circuit. Registers, 4-bit Register, with Clear  & Selective Parallel Load by clock gating, Avoiding clock gating. | 7.1 |
| 39 | W 18/5 | Shift Registers, Shift Register Applications, Bi-directional Shift Register  with Parallel Load, Counters, Ripple Counter. | 7.6 |
| 40 | S 21/5 | Up-Down Ripple Counter with Enable & Parallel Load. (**Quiz#8**) | 7.6 |
| 41 | M 23/5 | Synchronous Counters with incrementer: Serial and Parallel Implementations, Up/Down Synchronous Binary Counting with Enable and Parallel Load. Using Counters as Frequency Dividers. | 7.6 |
| 42 | W 25/5 | Modulo N counters, Designing Synchronous Counters using FSMs, Handling Unused States, Counter with Arbitrary Count Sequence. | 7.6 |
|  | W 25/5 | **Dropping all Courses with WP/WF** |  |
| 43 | S 28/5 | Programmable Implementation Technologies: Overview, Why Programmable Logic? Hardware Programming Technologies, Programmable Logic Configurations: ROM, PAL and PLA Configurations, Read Only Memory (ROM). | 6.8 |
| 44 | M 30/5 | Read Only Memory (ROM) Advantages/Limitations, Programmable Array Logic (PAL), Programmable Logic Array (PLA), Memory Devices: Introduction. | 6.8 |
| 45 | W 1/6 | Capacity of a Memory Device, Basic Types of Memory Devices, RAM Memory, Types of RAM Memory, Read Only Memory (ROM), Types of ROM Devices, ROM-based Designs. | 6.8 |
|  | S 4/6 (Makeup) | (**Quiz#10**) |  |
|  | U 5/6 (Makeup) | Final Exam Review. |  |