COE 202, Term 162

Digital Logic Design

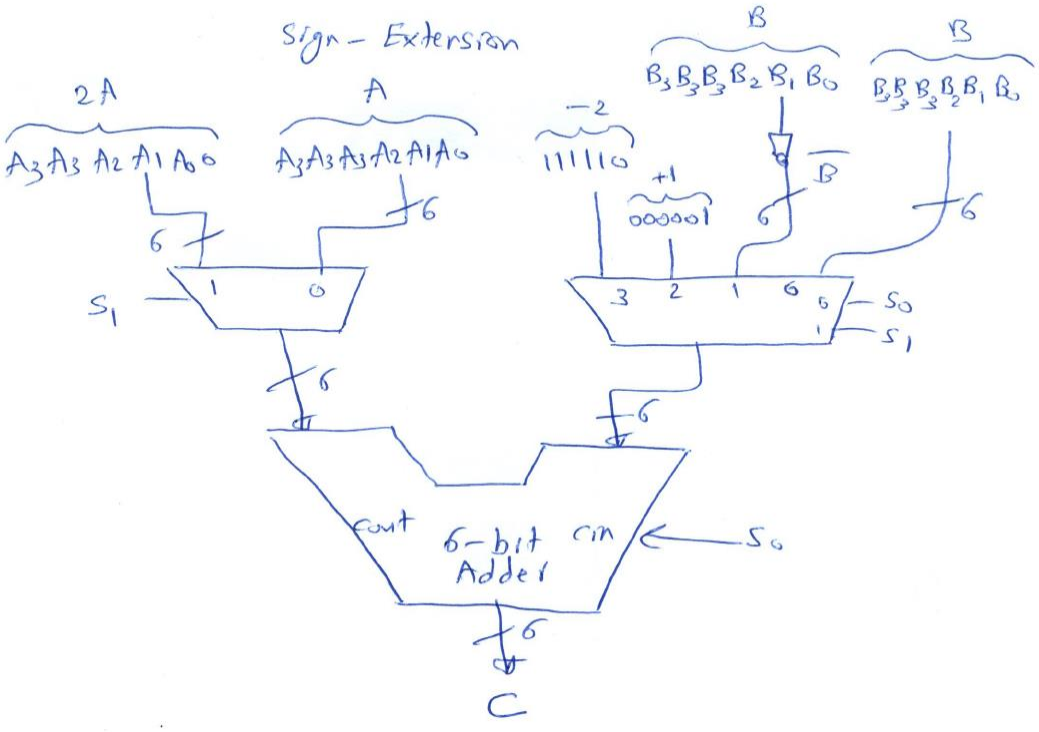
Assignment# 3 Solution

Due date: Thursday, April 27

Q.1. It is required to design a circuit that receives two **4-bit** signed numbers in 2's complement representation $\mathbf{A=A_3A_2A_1A_0}$, $\mathbf{B=B_3B_2B_1B_0}$ and produces a **6-bit output** $\mathbf{C=C_5C_4C_3C_2C_1C_0}$. The circuit implements the following functions based on the values of the two selection inputs: S1 and S0.

S1 S0	Function
0 0	C = A + B
0 1	C = A - B
1 0	C = 2A + 1
1 1	C = 2A - 1

(i) Show the block diagram design of your circuit using MSI components like Adder, Multiplexor, as needed. Use only one adder in your solution.



(ii) Model your design in Verilog by modeling each component separately i.e. adder, MUX, etc. and then instantiating these components to model your circuit.

```
module adder #(parameter width = 6)
(output cout, output [width-1:0] sum,
input [width-1:0] a, b, input cin);
        assign {cout, sum} = a + b + cin;
endmodule

module mux2x1 #(parameter width = 6)
(output [width-1:0] c,
input [width-1:0] a, b, input select);
  assign c = (select ? a : b);
endmodule

module mux4x1 #(parameter width = 6)
(output reg [width-1:0] y,
input [width-1:0] a, b, c, d, input s1, s0);
always @(a, b, c, d, s1, s0) begin
case ({s1, s0})
      2'b 00 : y = d;
      2'b 01 : y = c;
      2'b 10 : y = b;
      2'b 11 : y = a;
endcase
end
endmodule

module ALU
(output cout, output [5:0] c,
input [3:0] a, b, input s1, s0);

wire [5:0] T1, T2;

mux2x1 M1 (T1, {a[3], a, 1'b0}, {a[3],a[3],a}, s1);
mux4x1 M2 (T2, 6'b111110, 6'b1, ~{b[3],b[3],b}, {b[3],b[3],b}, s1, s0);
adder M3 (cout, c, T1, T2, s0);

endmodule
```

(iii) Write a Verilog test bench to test your design and verify its correctness by simulation. Show snapshots of your simulation to demonstrate its correctness. For each function, test at least 2 input combinations of your choice to demonstrate correct functionality.

```
module ALU_Test();

reg [3:0] A, B;
reg s1, s0;
wire Cout;
wire [5:0] C;

ALU  M1 (Cout, C, A, B, s1, s0);

initial begin
s1=0; s0=0; A=4'b0101; B=4'b0111;
#100 A=4'b0100; B=4'b1111;
#100 A=4'b0111; B=4'b0111;
#100 A=4'b1000; B=4'b1000;
#100 s1=0; s0=1; A=4'b0110; B=4'b0011;
#100 A=4'b1110; B=4'b1111;
#100 A=4'b1000; B=4'b0111;
#100 s1=1; s0=0; A=4'b0010;
#100 A=4'b1111;
#100 A=4'b0111;
#100 A=4'b1000;
#100 s1=1; s0=1; A=4'b0111;
#100 A=4'b1111;
#100 A=4'b1000;
end
endmodule
```

The test bench has been simulated and can be seen from the simulation waveform given below, the ALU is functioning correctly.