COE 202, Term 203

 Digital Logic Design

Assignment# 2 Solution

Due date: Saturday, July 10, 2021

# Given that X is a 4-bit signed number represented using 2’s complement representation. It is required to design a combinational circuit to compute the equation Y=3X-5.

## (3 points) Determine the range of output values that will be produced by this circuit. Determine the number of outputs needed for this circuit to produce the correct output without overflow.

Largest value = 3\*7-5=+16

Smallest value = 3\*-8-5=-29

Thus, we need 6 bits to represent the output correctly

## (8 points) Derive the truth table for this circuit.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| X3 | X2 | X1 | X0 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

## (12 points) Derive minimized equations for your circuit using K-Map method.

Y0 = X0’

Y1 = X1’



Y2 = X2 X0’ + X2’ X0 = X2 ⊕ X0



Y3 = X3’ X2’ X1’ + X3 X2’ X1 + X3’ X1’ X0 + X3 X1 X0 + X3’ X2 X1 X0’ + X3 X2 X1’ X0’

 = X2’(X3’ X1’ + X3 X1) + X0 (X3’ X1’ + X3 X1) + X2 X0’ (X3’ X1 + X3 X1’)

 = X2’(X1 ⊕ X3)’ + X0 (X1 ⊕ X3)’ + X2 X0’ (X1 ⊕ X3)

 = (X1 ⊕ X3)’ (X2’+ X0 ) + X2 X0’ (X1 ⊕ X3)

 = (X1 ⊕ X3) ⊕ (X2’+ X0 )



Y4 = X3’ X2’ X1’ + X2 X1 X0 + X3 X2 X1 + X3 X2 X0

 = X3’ X2’ X1’ + X2 X1 X0 + X3 X2 (X1 + X0)



Y5 = X3 + X2’ X1’

## (7 points) Write a Verilog module for modeling your circuit by using an assign statement for each output equation.

module Ass2 (output [5:0] Y, input [3:0] X);

assign Y[0] = ~X[0];

assign Y[1] = ~X[1];

assign Y[2] = X[2] ^ X[0];

assign Y[3] = (X[1] ^ X[3]) ^ (~X[2] | X[0]);

assign Y[4] = ~X[3] & ~X[2] & ~X[1] | X[2] & X[1] & X[0] | X[3] & X[2] & (X[1] | X[0]);

assign Y[5] = X[3] | ~X[2] & ~X[1];

endmodule

## (5 points) Write a Verilog test bench to test the correctness of your circuit for the following input values: X=0, X=-1, X=7, and X=-8. Allow a period of 20 ps between two consecutive test cases.

module Test\_Ass2();

wire [5:0] Y;

reg [3:0] X;

Ass2 M1 (Y, X);

 initial begin

 $dumpfile("dump.vcd");

 $dumpvars(1, Test\_Ass2);

 X = 0;

 #20 X=-1;

 #20 X=7;

 #20 X=-8;

 #20;

 end

endmodule

The simulation waveform is given below, which clearly shows correct outputs.



## (5 points) Submit a report (Word or PDF document) that should contain:

1. Problem description
2. Truth table and derived equations
3. A copy of the Verilog modules and test benches of parts (d) and (e)
4. The timing diagrams (waveforms) taken directly as snapshots from the simulator. Have as many snapshots as needed to cover all the test cases.
5. A link to your code in EDAPlayground (if you used it). If you used other tools (e.g. isim or Modelsim), you need to submit your Verilog files along with the report.

The assignment can be solved individually, or in groups of two students.

Submit a soft copy of your report on Blackboard along with Verilog files if needed.