KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS
COLLEGE OF COMPUTER SCIENCE AND ENGINEERING
***COMPUTER ENGINEERING DEPARTMENT***

# COE 200

# Fundamentals of Computer Engineering

## Syllabus – Term 051

## Catalog Description

Introduction to Computer Engineering. Digital Circuits. Boolean algebra and switching theory. Manipulation and minimization of Boolean functions. Combinational circuits analysis and design, multiplexers, decoders and adders. Sequential circuit analysis and design, basic flip-flops, clocking and edge-triggering, registers, counters, timing sequences, state assignment and reduction techniques. Register transfer level operations. ***(Prerequisite: PHYS 102)***

## Instructor

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## Course Material

1. **Text Book:** Morris Mano and Charles Kime, *Logic and Computer Design Fundamentals*, Second Edition, Prentice Hall International, 2000.
2. **Course CD:** A CD containing all course lectures with animations and sound is available. The material can be downloaded from the web page.

## Grading Policy

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| Laboratory | 20% |
| Assignments and Quizs | 15% |
| Exam I & Exam II | 35% |
| Final | 30% |

- Assignments include written and programming assignments
- Lowest two marks of the quizzes and assignments dropped
- Lowest exam counted as 15% and highest exam counted as 20%

## Course Road Map & Weekly Breakdown

| Week | Topic | CD Material | | Book Ref. |
|---|---|---|---|---|
| | | Unit | Lessons | |
| 1 | Introduction, Number System and Arithmetic | 1 | 1, 2 & 3 | 1.1-1.3 |
| 2 | Number Base conversion, Signed Numbers and Signed Numbers Arithmetic | 1 | 4, 5 & 6 | 3.9-3.10 |
| 3 | Codes and Binary Logic, Basic Identities, Algebraic Simplification | 1<br>2 | Lesson 7<br>Lesson 1 | 1.4 -1.5 &<br>2.1-2.2 |
| 4 | Canonical and Standard Forms, Physical Properties of Gates | 2 | 2 & 3 | 2.3&2.8 |
| 5 | Logic Simplification using K-Maps, K-Maps manipulation | 2 | 4 & 5 | 2.4-2.5 |
| 6 | 2-Level and Multi-level implementations, Universal Gates | 2 | 6 & 7 | 2.6-2.7 |
| 7 | Combinational Logic and Adders | 3 | 1 & 2 | 3.1-3.4 & 3.8 |
| 8 | Carry-Look-Ahead Adders and MSI Parts | 3 | 3 & 4 | 3.9-3.11 & 3.5-3.6 |
| 9 | Design with MSI Parts | 3 | 5, 6 & 7 | 3.7 |
| 10 | Sequential Circuits, Latches and FFs | 4 | 1 & 2 | 4.1-4.3 |
| 11 | Design of Sequential Circuits | 4 | 3 & 4 | 4.4 -4.7 |
| 12 | Analysis of Sequential Circuits | 4 | 5 | 4.4-4.7 |
| 13 | Registers and Counters | 5 | 1 - 4 | 5.1-5.6 |
| 14 | Programmable Logic | 6 | 1 & 2 | 6.1-6.2 & 6.5-6.9 |

## Online Lessons included on the course CD

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| | ***Unit I*** **: Number System and Codes** |
| 1 | Introduction. Information Processing, and representation. Digital vs Analog quantities. |
| 2 | Number Systems. Binary, Octal and Hexadecimal #'s |
| 3 | Number System Arithmetic. Binary arith (Addition, Subtraction & Multiplication). Arith in other systems. |
| 4 | Number base conversion (Dec to Bin, Oct, and Hex, General). Conv (Bin, OCT, Hex) |
| 5 | Binary Storage & Registers. Signed Binary Number representation, Signed Mag, R's &(R-1)'s Complement |
| 6 | Signed Binary Addition and Subtraction. R's Complement. Signed Binary Addition and Subtraction. (R-1)'s Complement |
| 7 | Codes. BCD, Excess-3, Parity Bits, ASCII & Uni-Codes |
| | ***Unit II :*** Binary Logic & Gates |
| 1 | Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra. Algebraic manipulation, Complement of a function. |
| 2 | Canonical and Standard forms, Minterms and Maxterms, Sum of products and Products of Sums. |

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| 3 | Physical properties of gates: fan-in, fan-out, propagation delay. Timing diagrams. Tri-state drivers. |
| 4 | Map method of simplification: Two-, Three-, and Four-variable K-Map. |
| 5 | Map manipulation: Essential prime implicants, Non-essential prime implicants, Simplification procedure, POS simplification, Don't care conditions and simplification, Five, and Six-variable K-Map. |
| 6 | Universal gates; NAND, NOR gates: 2-level implementation. Multilevel Circuits. |
| 7 | Exclusive-OR (XOR) and Equivalence (XNOR) gates, Odd and Even Functions, Parity generation and checking. |
| ***Unit III* : Combinational Logic** | |
| 1 | Combinational Logic, Design Procedure & Examples. |
| 2 | Half and Full Adders, Half and Full Subtractor<br>Ripple Carry Adder design and delay analysis<br>Binary Adders: 4-Bit Ripple Carry Adder, |
| 3 | Carry Look-Ahead Adder, Binary Adder-Subtractor. BCD Adder, Binary Multiplier |
| 4 | MSI parts. Decoders, Decoder expansion, combinational logic implementation using decoders, Encoders & Priority Encoders |
| 5 | Multiplexers, Function Implementation using multiplexers, Demultiplexers |
| 6 | Magnitude Comparator. |
| 7 | Examples of MSI designs |
| ***Unit IV* : Sequential Circuits** | |
| 1 | Sequential Circuits: Latches, Clocked latches: SR , D, T and JK. Race problem in clocked JK-Latch. Function & Excitation Tables of clocked latches: SR, D, and JK. |
| 2 | Flip-Flops: Master-Slave, T-FF. Function & Excitation Tables of T-FF. Asynchronous/Direct Clear and Set Inputs. Setup, Hold |
| 3 | Sequential Circuit Design: Excitation Tables. Design procedure, State diagrams and state tables. |
| 4 | Sequential Circuit Analysis: Input equations, State table. |
| 5 | Mealy vs. Moore models of FSMs. Examples. |
| ***Unit V* : Registers & Counters** | |
| 1 | Registers, Registers with parallel load, Shift Registers. Bi-directional shift register. |
| 2 | Synchronous Binary Counters: Up-Down Counters. |
| 3 | Counters with Parallel load, enable, synchronous clear and asynchronous clear. Use of available counters to build counters of different count. |
| 4 | Other counters: Ripple Counter, Arbitrary Count Sequence. |
| ***Unit VI* : Memory & PLDs** | |
| 1 | Memory devices: RAMs & ROMs . Combinational Circuit Implementation with ROM |

## Attendance Policy

- Attendance will be taken regularly. Students who are more than 10 minutes late are considered absent,
- There will be a 0.5% grade deduction for every unexcused absence,
- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.

## Ethics Policy

- All assignments are individual and only individual work will be accepted. Detected copies of assignments (written or programming assignments) will result in zeros for the whole group (including the student who actually solved the problem)
- Using unauthorized information or notes on an examination, peeking at others work, or altering a graded exam to claim more grades are severe violations of academic honesty. Remember that if you cheat, you are cheating no one but yourself. Detected situations will result in failing grades in the course, and depending on the severity of the situation, some cases may possibly end up in suspension from the university.