KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS
COLLEGE OF COMPUTER SCIENCE AND ENGINEERING
***COMPUTER ENGINEERING DEPARTMENT***

# COE 308
# Computer Architecture
# Syllabus – Term 052

## Catalog Description

Memory hierarchy and cache memory. Integer and floating point arithmetic. Instruction and arithmetic pipelining, superscalar architecture. Reduced instruction set computers. Parallel architectures and interconnection networks.
***Prerequisite:*** COE 205

## Instructor

Dr. Abdelhafid Bouhraoua Room: 22/137-1 Phone: 2178
Email: abouh@ccse.kfupm.edu.sa

## Office Hours

SMW 9:00 AM – 11:00 AM (and by appointment)

## Course Objectives

(1) To introduce students to the techniques used to enhance the performance of computer architecture including memory hierarchy, pipelining, and parallelism,

(2) To introduce students to the trade-off analysis in the design of various aspects of Computer Architecture including Instruction Set Design, Memory Hierarchy, Instruction Level Pipeline, and Multiprocessing.

## Course Learning Outcome

1. Ability to apply knowledge of mathematics, probability, and statistics in performance evaluation. This includes computing the CPU execution time, computing the CPI, speedup analysis, pipeline performance analysis, stall cycles, memory performance analysis, cache performance analysis, and I/O performance analysis.

2. Knowledge of contemporary Computer Architecture issues. This includes knowledge of the basic computer components, knowledge of integer and floating-point arithmetic and standards, knowledge of instruction set architectures, knowledge of the various memory technologies, and knowledge of virtual memory and its support in the processor architecture.

3. Ability to design a single-cycle integer datapath and its control, a multi-cycle datapath and its control, and a pipelined datapath and its control for a MIPS like

processor. Ability to detect and eliminate structural hazards in the design of the datapath. Ability to detect data hazards and design forwarding logic to eliminate stall cycles. Ability to stall the pipeline for hazards that cannot be eliminated. Ability to predict branches and handle control hazards.

4. Ability to use simulator tools in computer architecture evaluation. This includes the evaluation of instruction pipelines and cache-memory. (Project oriented)

5. Ability to function as an effective team member on a course project. (Project oriented)

6. Ability to engage in self-learning for a small subset of the course which is provided online. (Online course material oriented)

## Textbook

*Computer Organization & Design – The Hardware/Software Interface*: David A. Patterson and John L. Hennessy, Third Edition, Morgan Kaufmann, 2005

## References

1. Computer Architecture : Design and Performance, Barry Wilkinson, Prentice-Hall, 2nd Edition 1996
2. Computer Organization and Architecture : Designing for Performance, William Stallings, Prentice Hall, Fourth Edition, 2001

## Exams, Quizzes and Assignments

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|---|---|
| 5-6 | Written Assignments (Reading and Problem Solving) |
| 4-5 | Quizzes |
| 2 | Major Exams |
| 1 | Final |
| 1 | Project |

## Exam Dates

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|---|---|
| Major Exam 1 | Sunday March 26th 2006 |
| Major Exam 2 | Tuesday May 9th 2006 |
| Final Exam | Monday June 5th 2006 |

## Grading Policy

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|---|---|
| Quizzes and Assignments | 20% |
| Project | 15 % |
| Major Exam 1 | 20% |
| Major Exam 2 | 20% |
| Final | 25% |

- Assignments may include written and programming assignments
- Lowest two, three or four marks of the quizzes and assignments dropped

- Assignments are to be submitted in class (or by email) in the specified due date.
- Late assignments will be accepted for five days after the due date and be penalized 10% per each late day
- Assignments include:
  - Reading assignments
  - Problem solving
- The project will include some programming and architecture design

## Course Topics

1. **Introduction (1 lecture)**
   Introduction to computer Architecture (Sections 1.1 1.3), computer technology (Sections 1.4 1.5).

2. **The MIPS Instruction Set (1 lecture)**
   Brief introduction to the MIPS machine, registers, instruction set, instruction format, addressing modes, assembly, SPIM simulator

3. **Computer Performance (1.5 weeks or 3 lectures)**
   CPU Performance and Metrics (Sections 2.1 2.3, evaluating performance and benchmarks (Sections 2.4 2.8).

4. **Computer Arithmetic**. **(2 weeks or 4 lectures)**
   Signed and Unsigned Numbers (Sections 4.1 and 4.2), addition and subtraction (Section 4.3), logical operations (Section 4.4), constructing ALU (Section 4.5), multiplication and division (Sections 4.6 and 4.7), floating point representation (Section 4.8), and brief discussion on floating point in PowerPC and 80x86 (Section 4.9).

5. **Instructions: the language of the machine. (1 week or 2 lectures)**
   Introduction and operations of the computer hardware and its operands (Section 3.1 3.3), instruction Representation (Section 3.4), and making decisions, supporting procedure, addressing modes (Sections 3.5 3.8), and brief overview of MIPS instruction set (Section 4.11).

6. **Datapath and Control (2 weeks or 4 lectures)**
   Single-cycle datapath (Sections 5.1 5.2), implementation datapath (Section 5.3), and multi-cycle implementation (Section 5.4).

7. **Enhancing performance with pipelining (3 weeks or 6 lectures)**
   Pipelined datapath (Sections 6.1 6.2), pipelined control (Section 6.3), data hazards and forwarding (Section 6.4), data hazards and stalls (Section 6.5), branch hazards (Section 6.6), exceptions (Section 6.7), and superscalar and dynamic pipelining (Section 6.8 6.9).

8. **Memory System Design (3 weeks or 6 lectures)**
   Introduction and basics of caches (Sections 7.1 - 7.2), measuring and improving cache performance (Section 7.3), virtual memory and memory hierarchy (Sections 7.4 - 7.5), examples of memory hierarchies (Section 7.6), and performance and trends (Section 7.7 - 7.8).

9. **I/O and Buses (1 week or 2 lectures)**
   Introduction and I/O performance measure (Section 8.1), types and characteristics of I/O (Section 8.3), and connecting I/O devices to processor and memory using buses, (Section 8.4)

## Ethics Policy

- All assignments are individual and only individual work will be accepted. Detected copies of assignments (written or programming assignments) will result in zeros for the whole group (including the student who actually solved the problem)
- Using unauthorized information or notes on an examination, peeking at others work, or altering a graded exam to claim more grades are severe violations of academic honesty. Remember that if you cheat, you are cheating no one but yourself. Detected situations will result in failing grades in the course, and depending on the severity of the situation, some cases may possibly end up in suspension from the university.