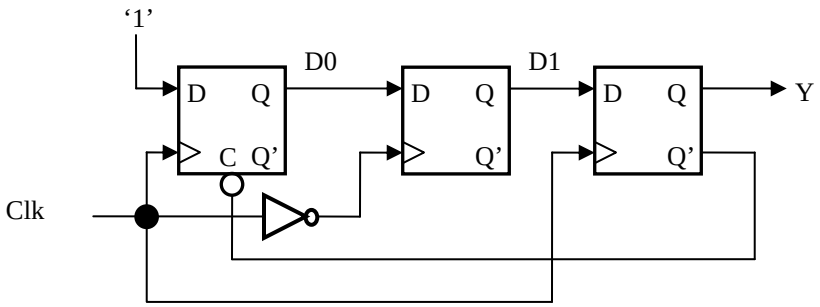
KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS
COLLEGE OF COMPUTER SCIENCE AND ENGINEERING
COMPUTER ENGINEERING DEPARTMENT

COE 202 - Term 053
Assignment #5

Q.1 (10 points)
Consider the following circuit:



All the flip-flops are positive edge triggered. At initialization, they are all initialized to 0.
Draw the timing diagram showing **Clk** and **Y**. You may want to represent any intermediate signal (**D0** or **D1** or both) to help you determine the value of **Y**. The representation of **D0** or **D1** is not mandatory.

Q.2 (20 points)
A designer needs a circuit that detects the binary sequence **0111**. The circuit should have one input **I** and one output **Y**. The input is synchronous to a clock **Ck** and changes on the positive edge of **Ck**.

1. Design a state machine (Moore type) that detects the sequence **0111** and draw its state diagram.
2. Represent the state transistion table of the state machine
3. Represent the excitation table of the state machine using D-type flip flops
4. Give the equations and draw the circuit of the state machine.

Q.3 (30 points)
A designer of a binary transmission system wants to balance the number of 1s and 0s. To do that, it decides to flip the 5^{th} bit of value 1 in a sequence of five 1s and flip the 5^{th} bit of value 0 in a sequence of five 0s.

1. Design the state machine that detects a sequence of five consecutive 1s and a sequence of five consecutive 0s. The state machine should be of Mealy type and should have a single output Y which should be 1 only when 5 consecutive bits of value 1 or value 0 have been detected. Y should be 1 during the same clock cycle as the 5^{th} bit of the sequence.

2. Represent the state transition table and the state excitation table. Extract the equations and represent the circuit.

Q.4 (10 points)

1. Design an 8 bits shift register that has the following characteristics:
   - Capable of shifting left or right (selectable using **LR** input: **LR** = 0: left; **LR** = 1: right)
   - Single serial input **SI** for both shift left and right
   - Uses positive edge-triggered D-type flip-flops.
2. Using this shift register design a shift register that maintains a single bit at 1 while all the other 7 bits will be at 0. The 1 is inserted on the first shift (either left or right) through the serial input **SI** to the MSB or LSB (depending on the shift). All subsequent shifts will move the 1 either left or right. After initialization the register should have a single bit at 1 all the time and any sequence of shifts should maintain this characteristic.

Q.5 (20 points)

Using blocks 4-bits synchronous binary counters with synchronous clear design a counter that divides a clock by 384. This means that the frequency of the output should be equal to the frequency of the input clock divided by 384.

Q.6 (20 points)

We want to design the basic building block of a human clock that displays the current time. This is a BCD counter that counts from 00 to 59 or from 00 to 12.

1. Design a single digit BCD counter that counts from 0 to 9 using a 4-bits synchronous binary counter with synchronous clear (reset).
2. Design a two digit BCD counter that counts from 00 to 12 using 2 4-bits synchronous binary counters with synchronous clear (reset).
3. Design a two digit BCD counter that counts from 00 to 59 using 2 4-bits synchronous binary counters with synchronous clear (reset).
4. Merge the design of 2 and 3 to make a single BCD counter that is capable of counting from 00 to:
   - either 12
   - or 59

   The max is selectable using a single input **K**.