Ref: Online course on EE-390, KFUPM

Handout 16

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Memory Interface Circuits 80x86 processors

Objective:

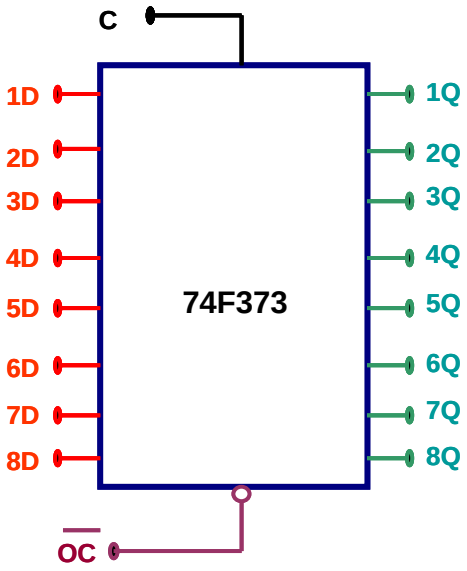
- To learn how memory interface blocks, such as Bus-controller, Address bus latch, Address decoder, Memory bank control logic for 8086 and Data bus transceiver buffer IC's are implemented using logic circuits.

- To discuss the operating detail of these circuits.

Slide 1: **8-bit Address Bus-latch IC for Memory interface:**

- Address-bus latch ("74F373") is controlled by ALE signal and used to latch the valid physical address ('ALE'$_{CPU}$ ➔ 'C'$_{74F373}$).

- The CLK ('C') signal is used to switch the outputted signals to transparent (input ➔ output) and latched (fixed output) states.



- The output control ('$\overline{OC}$') signal is used to assign high impedance state to the output lines (Q's),

Inputs			Output
'OC'	'C'	D's	Q's
L	H	H	H
L	H	L	L
L	L	x	Q_0
H	x	x	high-Z

Note: the circuitry used to construct this IC and their operating details are discussed in the following slides. Note that if the clock (C) input is logic low, the output logic level (Q's) remained unchanged or unaffected by inputted data (D's).

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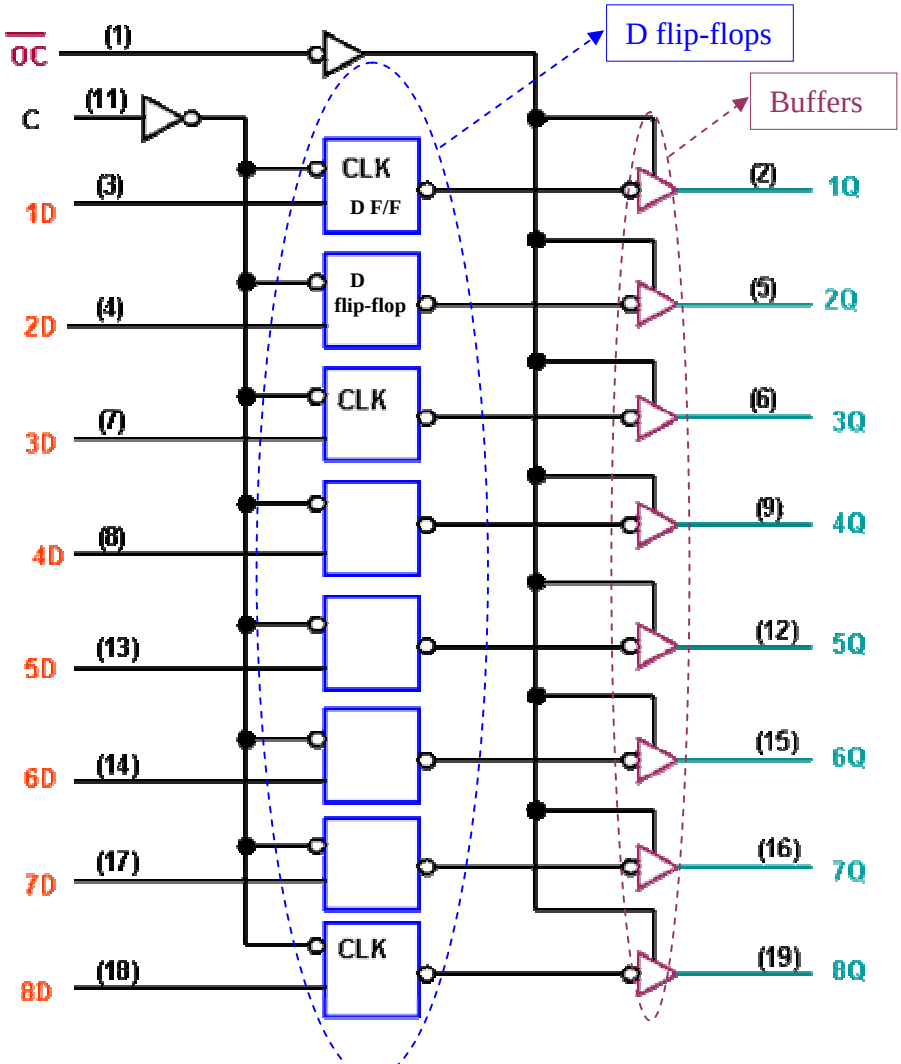
Slide 2: **Circuit diagram of 8-bit Address latch IC “74F373”:**

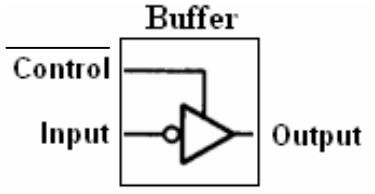


- The main components of this circuit are ‘D’ type flip-flops (in blue) and buffers (in brown)

Note: before explaining the operation of this circuit, lets discuss the construction and operation of these components.

Slide 3: **‘Flip-flops and Buffers used in Address bus latch circuit:**

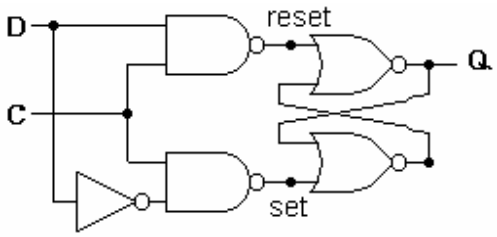
- Buffers are used to control and boast signal strength. For ‘logic 0’ control signal, buffers are in “transparent mode” and the inputted data is directly outputted.



- With ‘logic 1’ control input, high-impedance state is outputted.

- Flip-flops are memory elements in a sequential circuit.

- The circuit and transition-table of a D-type flip-flop are shown:



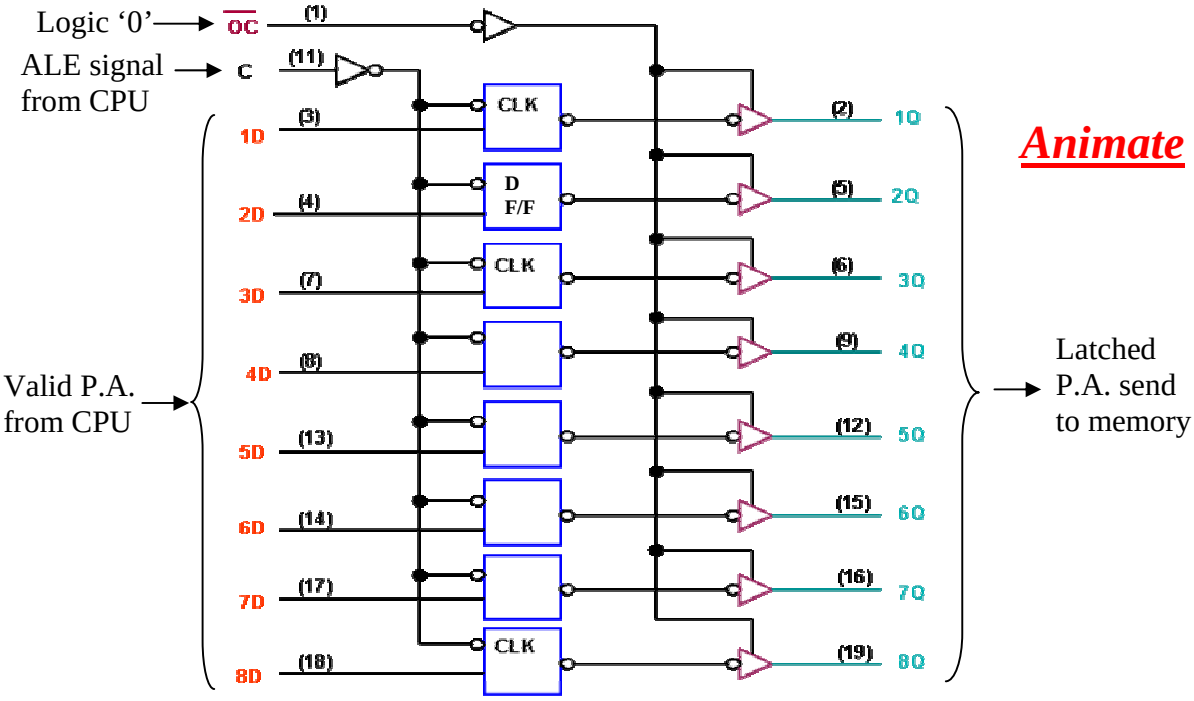
Q(t)	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

- Note that only ‘logic 1’ clock (C) signal activates NAND gates, which drives the NOR gate based ‘SR (set-reset)’ flip-flop.

Typically, all flip-flops provide a complemented output ($\overline{Q}$).

Note: *The maximum delay of latching D-type circuit is 13 nano second. It is important to keep this delay to a minimum. Also, the outputs of the latch can sink a maximum of 24 milli-ampere current.*

Slide 4: **Operation of 8-bit Address bus latch "74F373" IC:**



Animate

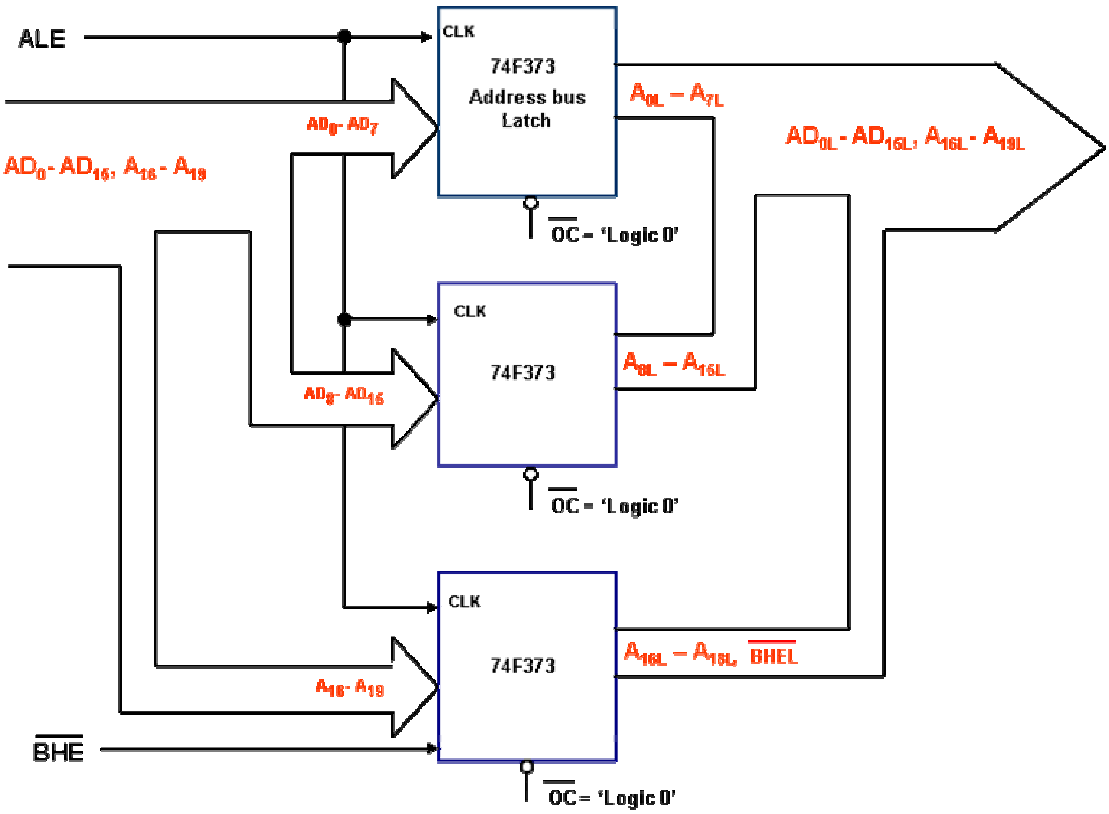
NOTE: If valid physical address is applied to the eight input pins (D's) of the IC and then ALE pulse is applied into the clock input of the IC, the D flip-flops will be activated and latch the inputted information.

Due to 'Logic 0' input of the output control pin, the buffers are activated and behave in transparent mode. Thus, the latched 8-bit physical address is outputted through the Q-pins.

Slide 5: **Operation of 20-bit Address bus latch circuit:**

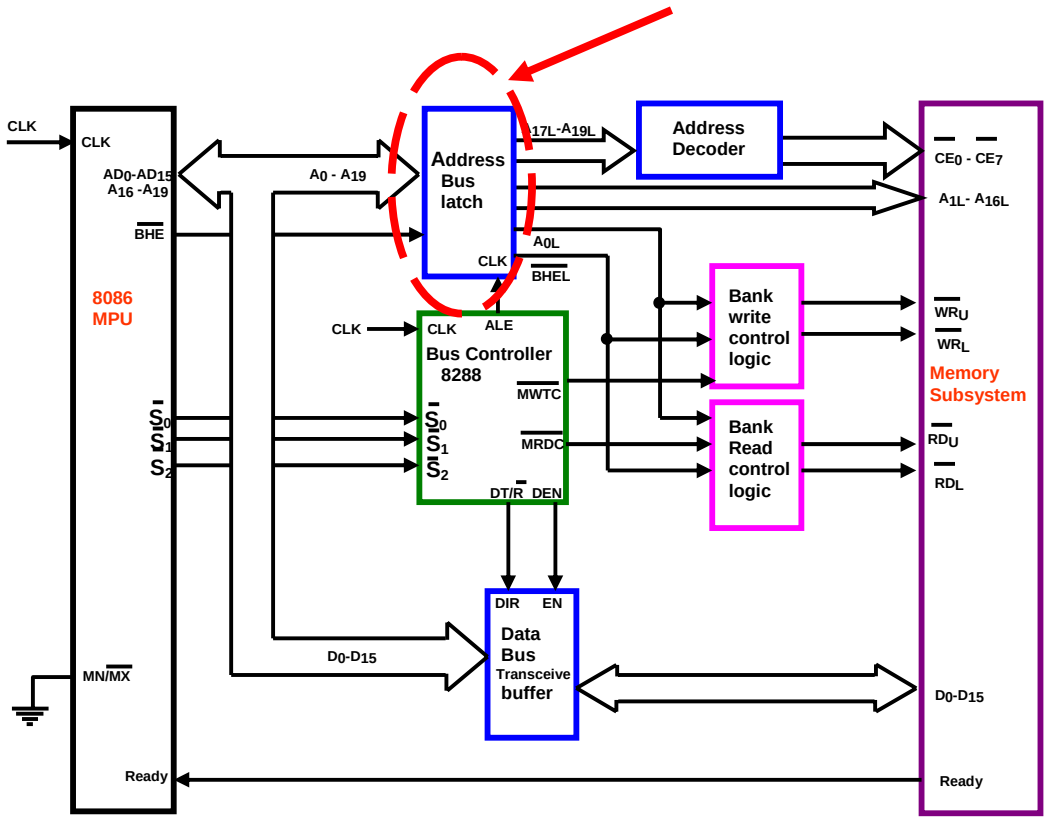
- Three 74F373 octal bus IC's are connected in parallel to construct the complete address bus latch circuit, which can latch 20 bit physical address and $\overline{BHE}$ signal (for 8086 case).

Such a circuit for 8086 memory interface is shown below:



The complete memory interface with this circuit component as "Address Bus Latch" is show in next figure.

Note: Note that each of the 74F373 IC's are used to latch 8-bit information as per ALE pulses, as buffers works in transparent mode. This diagram consists the Address bus latch block, of the memory interface discussed before. Click the link to see this complete circuit.

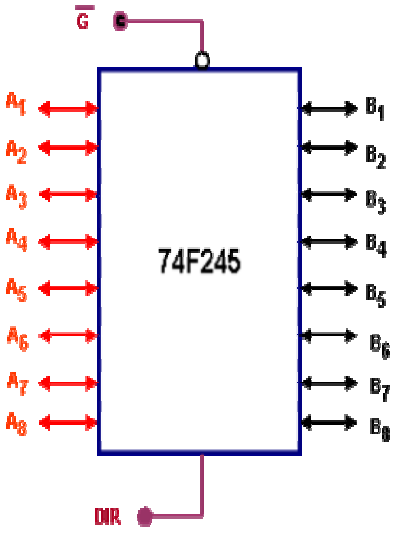


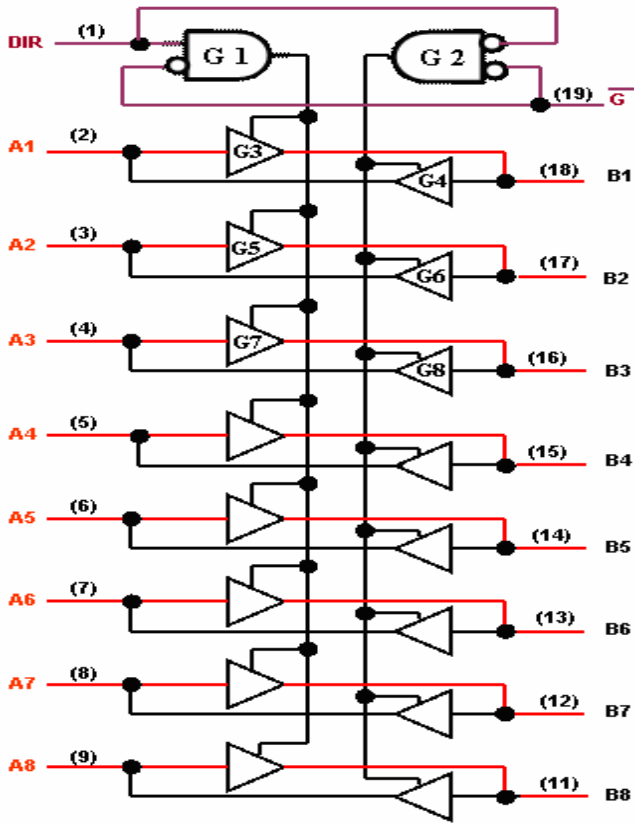
The complete memory interface circuit

Slide 6: **Operation of Data bus transceiver buffer:**

- Data bus transceiver buffer in 8088 system is implemented using 74F245 octal bus IC's, where the control inputs 'DIR' and '$\overline{G}$' is used to control the data flow (A_n ➔ B_n or B_n ➔ A_n)

Animate





- Once enabled with $\overline{G}$ = 0

  DIR = '0' ➔ B_n => A_n ;

  DIR = '1' ➔ A_n => B_n ;

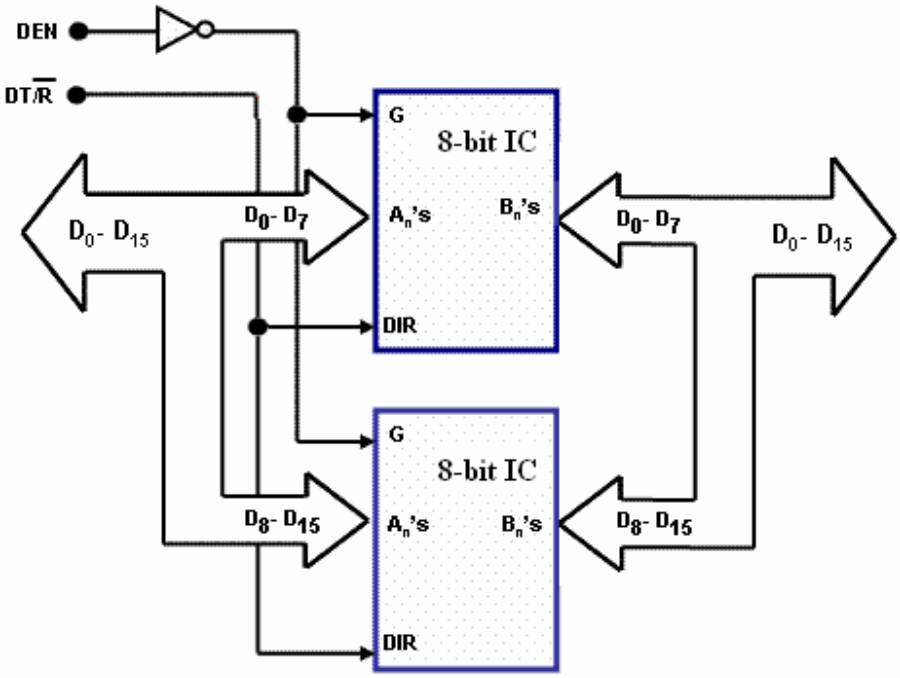
***Note:**. The figures above shows the block and circuit diagram of the 8-bit Data bus transceiver buffer IC. Also note that G bar input is used to enable the buffer operation, whereas DIR input selects the direction of intended data transfer.*

Assume that the device is enabled by applying G bar = 0. Now if DIR is set to logic 0, the output of AND gate 1 will be 0 and all the odd numbered buffers (G3, G5, G7 and so on) will be off. So the data path from An to Bn will be disabled. But the output of AND gate 2 will be logic 1 and all the even numbered buffers (G4, G6, G8 and so on) will be ON. Consequently, the data path from Bn to An will be ENABLED.

Similarly, for G bar = 0 and DIR = logic 1, data path from An to Bn will be ENABLED.,

Slide 7: **Operation of Data bus transceiver buffer (cont'd):**

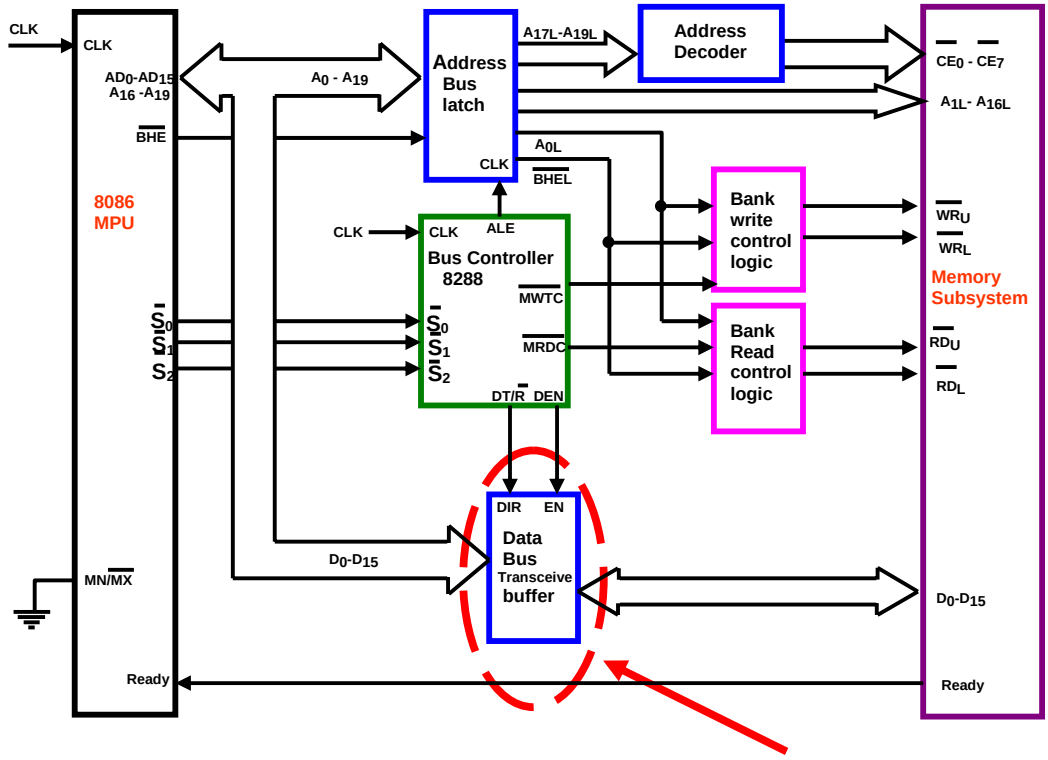
- The transceiver buffer in 8086 system is implemented using two parallel IC's capable of 16-bit bidirectional data transfer



The complete memory interface with this circuit component as "Data Bus Transceiver Buffer" is show in next figure.

Note: Here two octal buffer IC's are parallely connected to achieve 16-bit bidirectional data bus transceiver buffer operation. The complete memory interface circuit with this transceiver buffer component can be seen by clicking the given link.

Note that the enable signal (G) that comes from the DEN signal of the CPU, requires logic -1 to enable the buffer, unlike that of 8088.

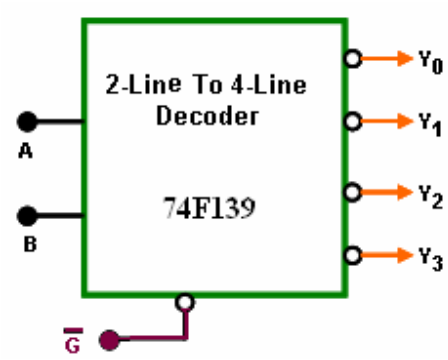


The complete memory interface circuit

Slide 8: **Decoder circuits used in 8088/8086 memory interfaces:**

- Decoder circuit's implements Address-decoder in both 8088 & 8086 interface and Bus-controller in 8086 based system.

- The operation of a 2-line by 4-line decoder is presented below:



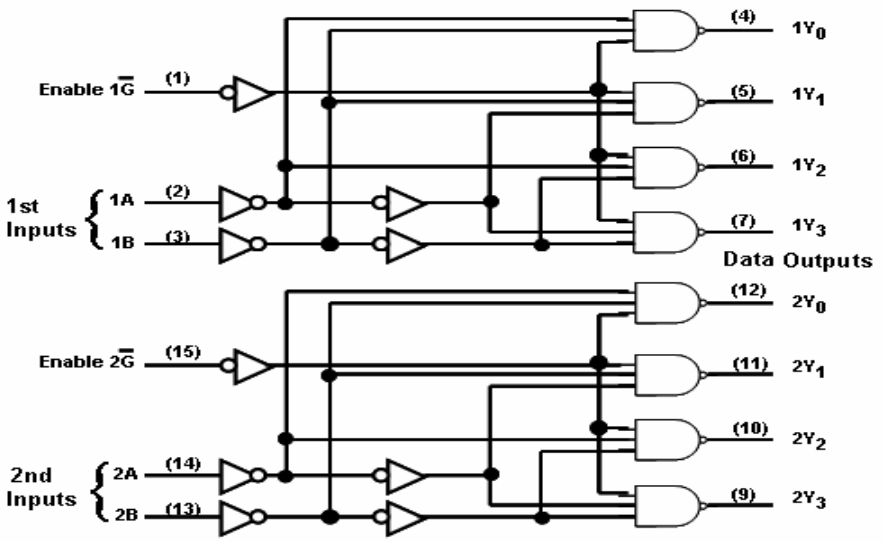
INPUTS			OUTPUTS			
Enable	Select					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

- Note that $\overline{G}$ input is the control input that enables the decoder. Once enabled, any of the four outputs (Y_0 to Y_3) are selected depending on logic levels of inputs 'A' & 'B', as shown in Table

Note: Note that due to the output inverters of the IC, when selected, the outputs generated a logic low signal.

Slide 10: **Decoder Circuits used in Memory Interface (Cont'd):**

- The circuit diagram of a decoder/demultiplexer (74F139) is:



- The device has two independent decoders, each accepting 2-inputs and providing 4 mutually exclusive active LOW outputs.

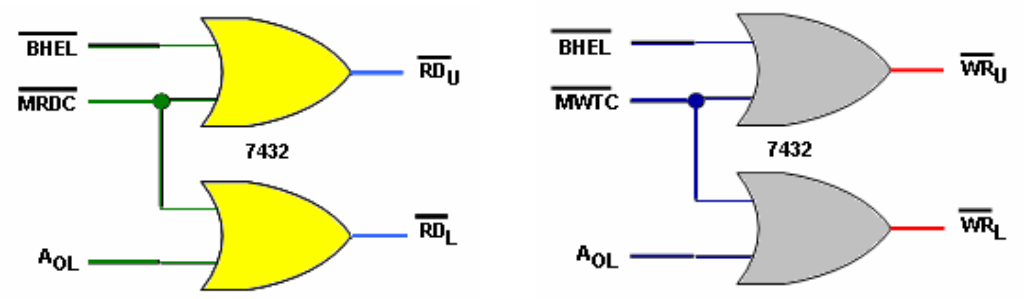
Note: *Each decoder has an active LOW Enable input, which can be used to activate the decoder.*

Slide11: **Controller circuits of 8086 Memory Interface:**

- Bank read and write control logic circuits enables even and odd address byte transfer, as per logic levels of $\overline{BHE}$ and A_0 signals.
  Note: Detail discussion in this topic can be found in next lecture.

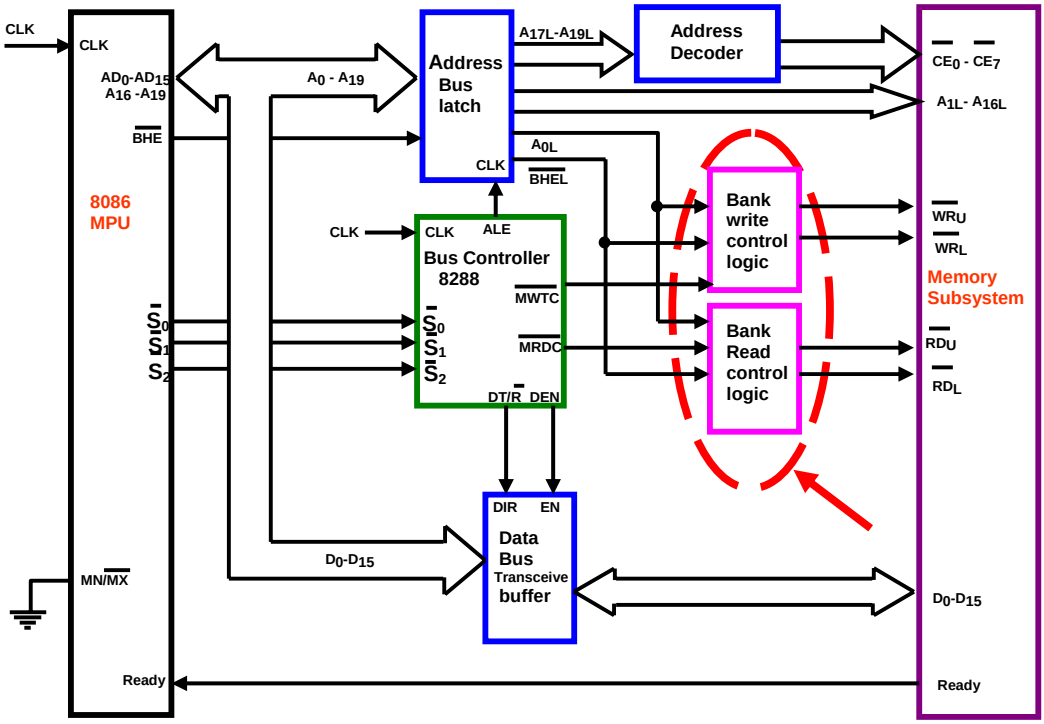
- For even addressed words, both $\overline{BHE}$ and A_0 signals are activated at the same time to initiate 16-bit data transfer

- Read and Write bank control logic circuits are as given below:



Note: Note proper read or write signal should also be generated by the CPU to activate these controllers.

The complete memory interface circuit where this above component is used is:

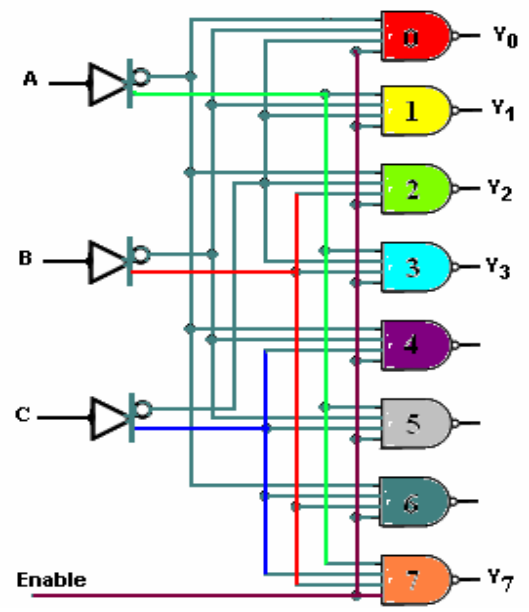


Slide 12: **Example 1: Design a Decoder circuit**

QUESTION: Using 4-input NAND gates, design a 3-line by 8-line decoder circuit with one enable input. Thus, when 'Enable' input is at logic 1 and the three coded inputs (CBA) are at logic 0 state ('C'='B'='A'='0') the corresponding decoded output should be enabled or at logic 0 level ('Y_0'='0') and all the remaining seven outputs should be disabled or at logic 1 state.

SOLUTION: The required circuit is shown in the figure. Note that when Enable ='logic-1' and C=B=A are at 'logic-0' state, only AND gate-0 has all its four inputs at logic-1 level. Consequently, the output Y_0 will be enabled or at logic-0 state.

All other AND gates have one or more inputs at logic-0, and the corresponding output (Y_1 to Y_7) will be disabled or stay at logic-1 state.

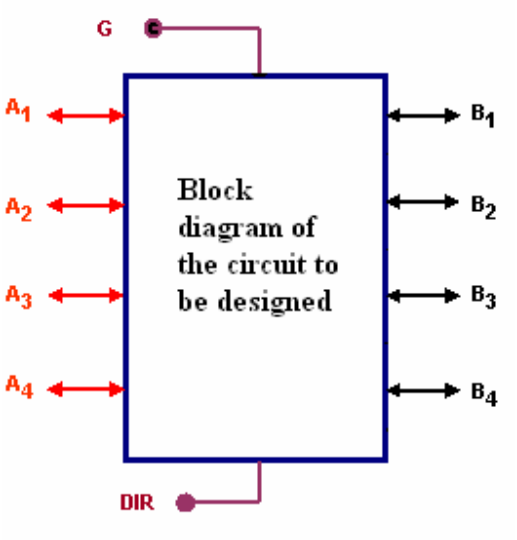


Slide 13: **Exercise 1:**

Using eight buffer circuits, design a 4-bit data bus transceiver buffer circuit that once enabled with G = 1, transfers data according to following DIR input.

(a) $B_n \rightarrow A_n$ if DIR = '1'

(b) $A_n \rightarrow B_n$ if DIR = '0' ;



SOLUTION: