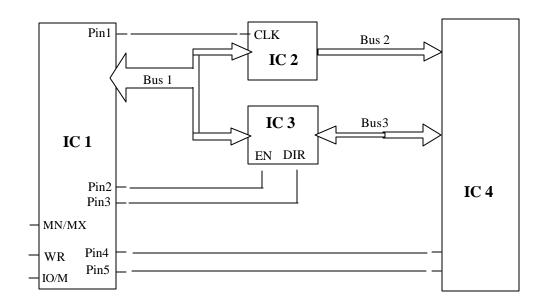
Home work Dr. S. Iqbal

1. The pin connections the 8088 MPU in Min mode (IC1), address bus latch (IC2), data bus transceiver buffer (IC3) and the memory system (IC4) is given in the following figure. For a memory **read** bus cycle, **label** and **name** the required **pins** and **buses**.



(a) Write the name and the Logic-levels of the following pins for above operation;

Pin 1:_______; Bus 3:________;

(b) Write the steps that are performed by CPU to complete the above operation;

ill the following	questions:			
(i) 8086 microprocessor has bit address-bus and bit data-bus.				
(ii) In 8086, the bus cycle consist of at least clock pulses and if required wait status can be inserted by using the pin of the microprocessor.				
 Define the following functions according to the <u>preceding</u> order (to occure in 1st, 2nd and 3rd) during a write bus cycly : DEN, IO/M and ALE. 				
	Signal name		Function	
1 st to occure				
2 nd to occure				
3 rd to occure				
	(i) 8086 microprofii) In 8086, the between wait status can be status of the follow in 1st, 2nd and 1st to occure 2nd to occure	Define the following functions according I^{st} , 2^{nd} and 3^{rd}) during a write Signal name I^{st} to occure I^{nd} to occure	(i) 8086 microprocessor has bit address-bus at least classically consist of at least classically can be inserted by using the before the following functions according to the preceder in 1 st , 2 nd and 3 rd) during a write bus cycly: Signal name 1 st to occure 2 nd to occure 2 ⁿ	(i) 8086 microprocessor has bit address-bus and (ii) In 8086, the bus cycle consist of at least clock pulses a wait status can be inserted by using the pin of the preceding order (the in 1st, 2nd and 3rd) during a write bus cycly: DEN, IO/M Signal name

4. Solve the problems of Chapter 8.