A New 8-Folds CMOS Current-Mode Saw-Tooth Folding Amplifier

Journal:	*International Journal of Electronics*
Manuscript ID	TETL-2017-0009
Manuscript Type:	International Journal of Electronics Letters (2500 word limit)
Date Submitted by the Author:	03-Jan-2017
Complete List of Authors:	Al-Absi, Munir; KFUPM, EE Abuelma'atti, Muhammad Taher; King Fahd University of Petroleum and Minerals, College of Engineering Elhassan, Mohanad; King Fahd University of Petroleum and Minerals, EE Dhar, Sagar; King Fahd University of Petroleum and Minerals, EE
Keywords:	Folding amplifier, current mode, analog-to-digital converter, folding flash, saw tooth

A New 8-Folds CMOS Current-Mode Saw-Tooth Folding Amplifier

Munir A. AL-Absi, M. Taher ABuelma'atti, Mohanad Elhassan and Sagar Dhar

Electrical Engineering Department, King Fahd University of Petroleum & Mineral, Dharan City, Saudi Arabia

Munir A. AL-Absi mkulaib@kfupm.edu.sa

A New 8-Folds CMOS Current-Mode Saw-Tooth Folding Amplifier

This paper presents a new 8-folds current-mode sawtooth folding amplifier. The proposed circuit is compact and minimizes the delay in the signal path between the input and output by minimizing the number of current mirrors in this path. This improves the speed of the proposed amplifier. The functionality of the proposed circuit was tested and confirmed using LFoundry 150nm process in Cadence simulation tools. Simulation results obtained from the proposed 8-folds folding amplifier show that the settling time for the full scale rising and falling edges are 8.4ns and 3.5ns respectively. For comparison with already existing folding amplifiers, the proposed circuit was scaled down to provide 4 folds. Simulation results obtained from the 4-folds amplifier show that a full scale delay of 5.9ns can be achieved. This is more than four times faster than already existing designs in the open literature. Furthermore, the simulation results obtained from a sinusoidal and a triangular input current confirm the workability of both the 4- folds and the 8-folds amplifiers. The simulation results also show that the circuit is temperature insensitive and is functioning as expected in the temperature range -25°C to 125°C.

Keywords: Folding amplifier; current mode; analog-to-digital converter.

;

Introduction

Analog to digital converters (ADC) are basic building blocks in modern mixed-mode analog and digital signal processing. This justifies the quest for designing low voltage, low power, high speed and compact ADCs. Over the years different architectures of ADCs have been developed. Among the available ADC designs it is well known that the full flash ADC is the fastest. Unfortunately, an N-bits full flash ADC

requires $2^N - 1$ comparators and 2^N equal-value resistors. This would require large area on the chip and consume relatively large powers. Thus, the full flash ADC is considered to be impractical for relatively large number of bits. Fortunately, using the concept of folding ADC can reduce the number of active and passive components of flash ADC with a reasonable cost in terms of reducing the conversion speed of the ADC. In a folding ADC a folding amplifier must be used. In order to avoid the use of correcting circuits to reduce the errors resulting from the folding process it is preferable to use a folding amplifier with sawtooth input-output characteristics.

Conventional voltage-mode folding amplifiers have been reported in the literature [1]-[7]. In references [1]-[4] the folding ADCs use the voltage-mode folding amplifiers with a sinusoidal or a triangular folding characteristics. Folding ADCs exhibiting the nonlinear sinusoidal or the triangular transfer characteristics cause error in digitization [5]. Thus, additional circuits would be required for error correction/compensation. Obviously this would increase the power consumption and the area on the chip and may add additional time delay. Moreover, the nonlinearity of the differential amplifier used would limit the operation of the folding amplifier to relatively large voltages and the circuits proposed in [1]-[4] would not be suitable for low voltage applications. In references [6] and [7] the proposed voltage-mode folding amplifiers offer sawtooth transfer characteristics but are subjected to exact voltage generation which would require extra power management circuitry.

Recently the current-mode approach has attracted the attention of many designers. This is attributed to the simple circuitry, faster response and low-voltage operation of current-mode circuits compared to the voltage-mode counterparts [8]. Thus, current-mode folding amplifiers with sawtooth transfer characteristics and faster response would be of interest. However, despite the obvious advantages that make such amplifiers excellent candidates for the design of improved flash folding ADCs, in the open literature only very few current mode folding amplifiers are reported [9]-[14].

In references [9] and [10], the authors present current-mirror based folding amplifiers exhibiting triangular transfer characteristic. This would cause conversion error in the ADC applications and would require further correction circuits, more power consumption and area on the chip in addition to possible delays. The current mode folding amplifier reported in [11] uses the current steering technique and exhibits a sinusoidal transfer characteristic. Again, this would lead to errors in ADC applications and would require further correction circuits with possible delays, additional area on the chip and increased power consumption. In reference [12] a current-mode folding amplifier with sawtooth transfer characteristic was realized using two building blocks; one of the blocks is used for producing a linear portion and the other one is used for producing the sharp transition of the sawtooth. However, the sharp transition was realized using large transistors (to obtain large current-mirror ratio) which caused slower response of the overall folding amplifier. A regeneration of the folding amplifier reported in [12] shows a response time of about 235ns with $0.35\mu m$ technology. This is relatively large delay which will be a major drawback for the realization of a high speed folding ADC.

In [13] the authors presented a new design for a 4-fold current mode folding amplifier which reduced the response time to 25ns. However, in terms of speed and accuracy, it is observed that the major bottleneck in the design of current-mode folding amplifier is the current mirrors. This is attributed to the relatively long time required to charge (or discharge) the relatively large pair of gate-to-source capacitances ($2C_{GS}$) especially when switching OFF or ON. As such it is desirable to reduce the number of current mirrors in the signal path between input and output.

In [14] a further improvement of the 4-fold folding amplifier has been presented. The resulting circuit uses the minimum number of current mirrors in the signal path. Thus, reducing the time delay. Simulation results obtained from the circuit proposed in [14] using LFoundary 150nm technology in Cadence Tools shows a 5.9 ns full scale delay time from input to output. This is far better than the results reported using the circuits presented in [12] and [13].

The major intention of this paper is to build upon the results obtained in [14] and to present an 8-fold current-mode folding amplifier. For further investigation of the folding amplifier performance, the paper will also present results obtained from the transient analysis of the folding amplifier excited by a triangular input current, a sinusoidal input current and the effect of temperature variations on the performance of the amplifier.

The rest of this paper is arranged in three sections as follows: Section II presents the folding amplifier block diagram and the circuit implementation of the different blocks. Section III discusses the simulation results of the folding amplifier. The paper is concluded in Section IV.

Proposed Folding Amplifier

The block diagram of a folding amplifier based ADC system is shown in Fig 1. A folding amplifier is characterized by the number of folds, N, and the fold size I_F. Conceptually, the folding amplifier maps the input into the output in a modulo division fashion [11], [15]. If the signal is larger than the fold size, then I_F is repeatedly subtracted from it until it is smaller than the fold size. This leads to a sawtooth characteristic as shown in Fig. 2. To realize such characteristics two elements are required: mirroring the input to output and subtracting the value once the input is beyond certain points. These points are of course: I_F, $2I_F$, $3I_F$,...,$(N-1)I_F$ for an N fold amplifier.

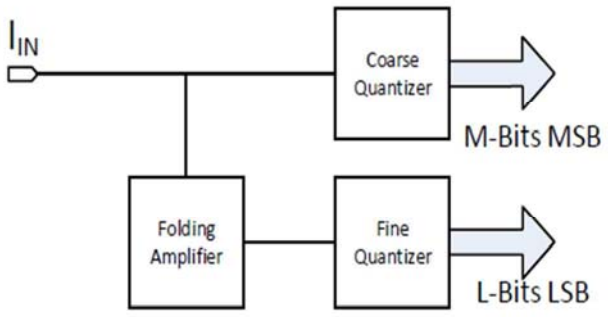


Figure1. Folding amplifier concept

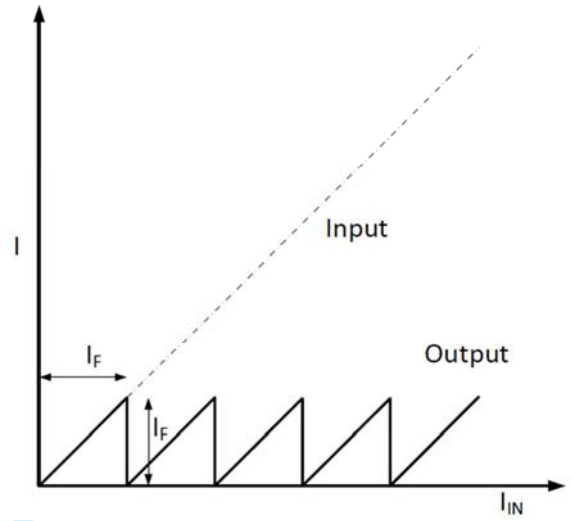


Figure2. Input output characteristic of the amplifier

The work presented in this paper is an extension of the work proposed in [14]. The block diagram of the circuit proposed in [14] is reproduced here and is shown in Fig. 3. It is a straight forward implementation of the modulo division concept described in the previous paragraph. The amplifier has two inputs: the input current signal I_{IN} and the reference current I_{REF}. The fold size in this case is $I_F = I_{REF}/N$. The two currents are fed to two mirroring and scaling circuits, the current copier and the reference scaler. The current copier produces N outputs: $N-1$ copies are shown as I_{CP} in Fig. 3 and one copy as I_X which goes directly to the output. The current scaler produces $2(N-1)$ outputs. $(N-1)$ outputs are scaled as I_{REF}/N, $2I_{REF}/N,\ldots,(N-1)I_{REF}/N$, which are shown as I_{SC} in Fig. 3. The other $(N-1)$ outputs are all I_{REF}/N and are shown as I_Y in Fig. 3. I_{SC} and I_{CP} are subtracted from each other at the entrance of the comparators which decides whether the resulting currents are greater or less than zero, effectively giving $B[i]$ = logic 1, for $I_{CP}[i] < I_{SC}[i]$ for $i = 1,2,\ldots,N-1$. The binary signal $B[i]$ is used to switch on/off the i^{th} transmission gate (shown as TGate) which subtracts a current $I_F = I_{REF}/N$ from the output, hence realizing folding. Notice that only one current mirror separates the input signal from the output. Thus, the minimum number of current mirrors is used in the path between the input and the output of the proposed structure.

The circuits used to realize the blocks of Fig. 3 are shown in Fig. 4. Instead of using large channel length transistors in the current mirrors as in [13] a folded cascode mirror is used for all the current mirrors [16]. This allows the use of smaller channel length transistors (300nm for all mirroring transistors) while not sacrificing the accuracy (simulation results show that all mirrors give less than 2% error for currents in the range $1 - 32\mu A$). For the current scaler the IY output terminals are not shown as they are similar to those used in the current copier. The cascode transistors are biased by a transistor which is half the width of the main transistor and biased by ICAS = 35μA.

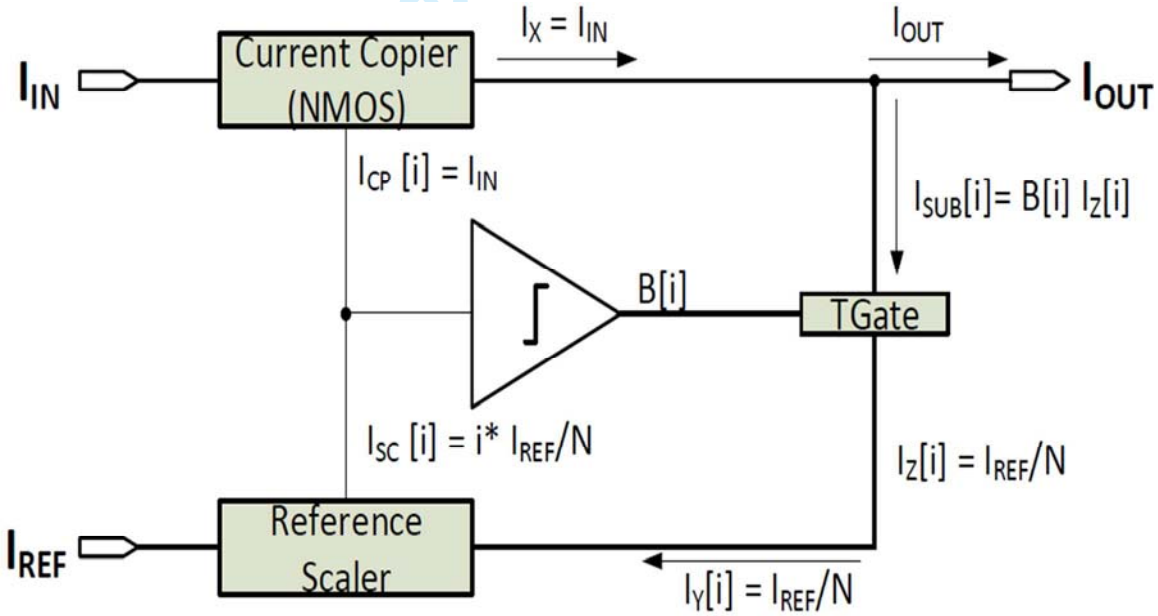


Figure3. Block diagram of the proposed design

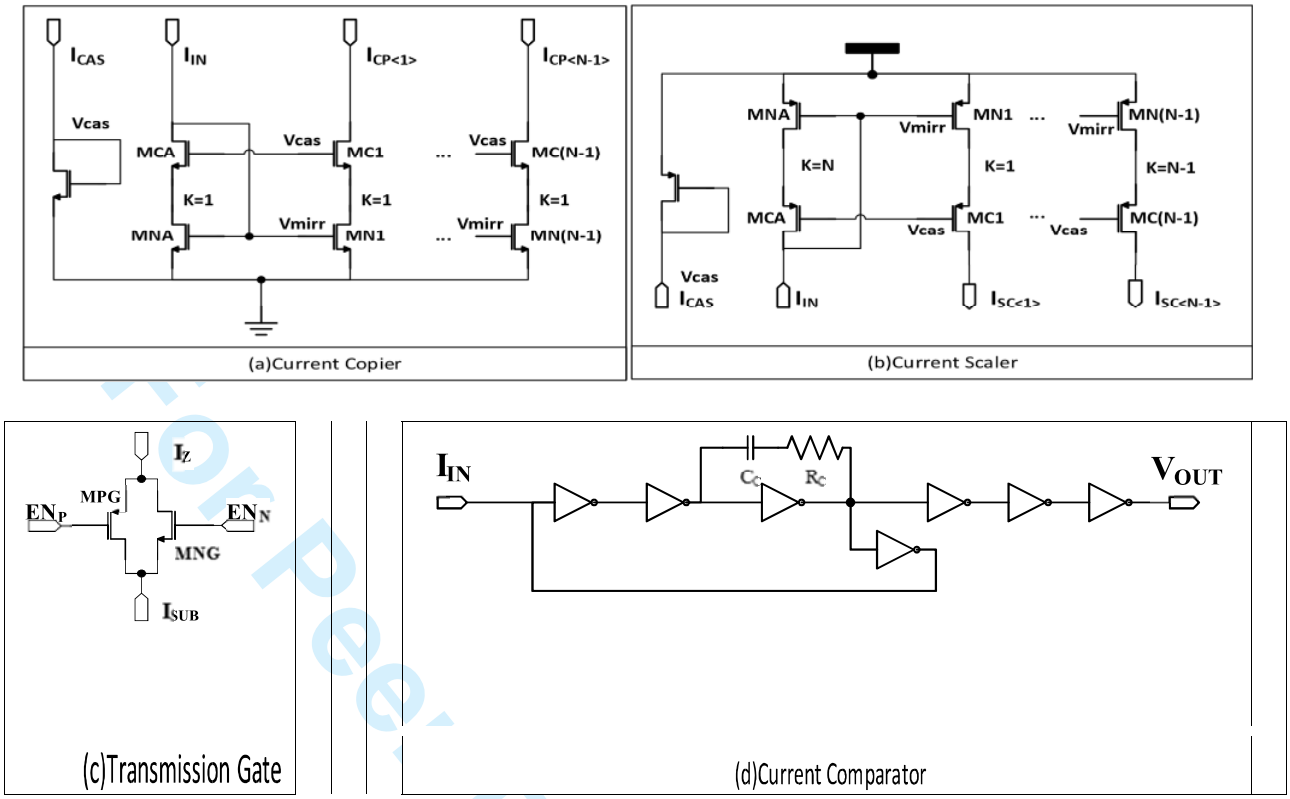


Figure4. Circuit level implementation of the folding amplifier blocks: (a) Current copier (b) Reference scaler (c) Transmission gate (d) Current comparator

Simulation Results

The proposed 8-folds folding amplifier was simulated in LFoundry 150*nm* process with a supply voltage of $V_{DD} = 1.8V$. To compare with the results reported in [13], a folding amplifier with $N = 4$ was also designed, with a fold size of $4\mu A$ and with a load resistance of $10K\Omega$ connected to mid-supply ($V_{DD}/2 = 0.9V$). The simulated input-output relationship is shown in Fig. 5. This was obtained by performing a DC sweep of the input current from $0 - 20\mu A$ at a step of $50nA$. The error between the ideal and the simulated characteristics is shown in Fig. 6. The spikes are the misalignment of transition points from the ideal values of $4,8,...,20\mu A$. Ignoring the misalignment of the switching points from the ideal values, the maximum error is less than $0.07\mu A$ at an input current of $20\mu A$.

To test and compare the response time of the 4-folds folding amplifier, rising full-scale pulse signal (from $0\mu A$ to $20\mu A$) and falling full-scale pulse signal from ($20\mu A$ to $0\mu A$) were applied. These are shown in Fig. 7(a) and Fig. 8(a) respectively. The comparator outputs are shown in Fig. 7(b) and Fig. 8(b) respectively. Inspection of Figs. 7(a) and 8(a) shows that the falling pulse settled much faster than the rising one. Also in Fig. 7(a) one can very clearly notice the sudden jumps due to mirrors being switched on, which correspond to the switching instances in Fig. 7(b). The 2% settling time was found to be $5.9ns$ for the rising pulse and $2.3ns$ for the falling pulse. Using the full scale delay there is a fourfold improvement of speed over [13]. All the comparators settled in at most 2ns while the main current mirror took about 4ns after the last comparator to settle.

Transistor	Size
Current Copier	
Cascode Bias	500nm/320nm
MCA, MNA	1000nm/320nm
Current Scalar	
Cascode Biasing	500nm/300nm
MCA, MNA	8000nm/300nm
MC1, MN1	1000nm/300nm
MC2, MN2	2000nm/300nm

Transmission Gate	
MPG	500nm/150nm
MNG	320nm/150nm
Current Comparator	
Inverter NMOS	1000nm/150nm
Inverter PMOS	3000nm/150nm
CC	100fF
RC	1.6KOhm

Table1. Transistor Sizes

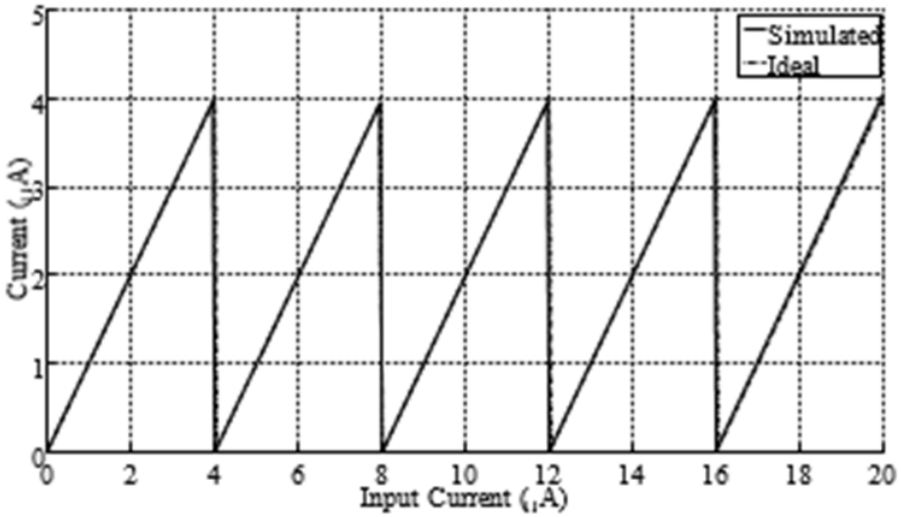


Figure5. Input /output characteristics of the folding amplifier.

These results confirm that an improvement in the current mirror design in addition to reducing the number of current mirrors in the path of the signal can substantially improve the performance of folding amplifiers.

In order to test the performance of the 4-folds current-mode folding amplifier under practical working conditions, a sinusoidal input signal of frequency = 5MHz was applied to the folding amplifier and its output was monitored. The results obtained from the transient response of the proposed folding amplifier are shown in Fig. 9. These results show that the switching events follow the ideal switch instances within the delays predicted by the pulse test. Moreover, the proposed circuit was also tested with a triangular input current and the output current was monitored. The transient response for the triangular input is shown in Figure 10. Inspection of Fig. 10 shows that the proposed current-mode folding amplifier is functioning properly.

Furthermore, the number of folds of the folding amplifier was increased to 8 to provide an 8-folds amplifier. With N = 8, using the same fold size ($I_F = 4\mu A$), the full scale value of the current is now $32\mu A$. The new developed 8-folds folding amplifier circuit was simulated using the same building blocks shown in Fig. 4 and the settling times for the rising and falling pulses were monitored. As expected the current mirrors became slower as the number of output branches increases and the settling time for the full scale rising and falling pulses increased to $8.4ns$ and $3.5ns$ respectively.

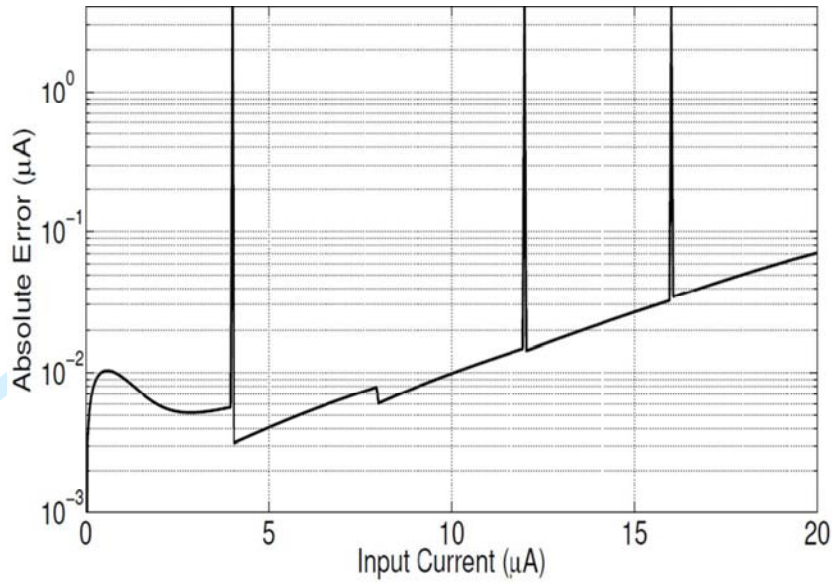
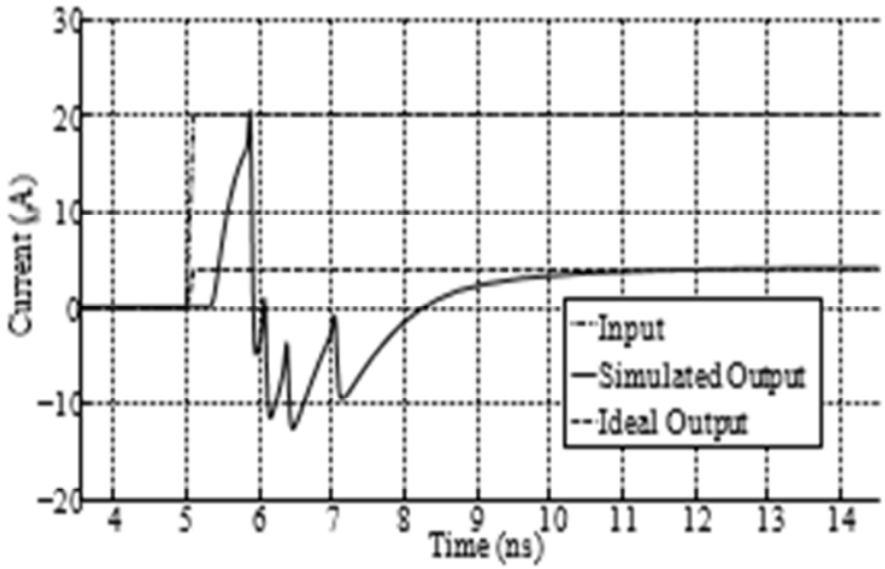
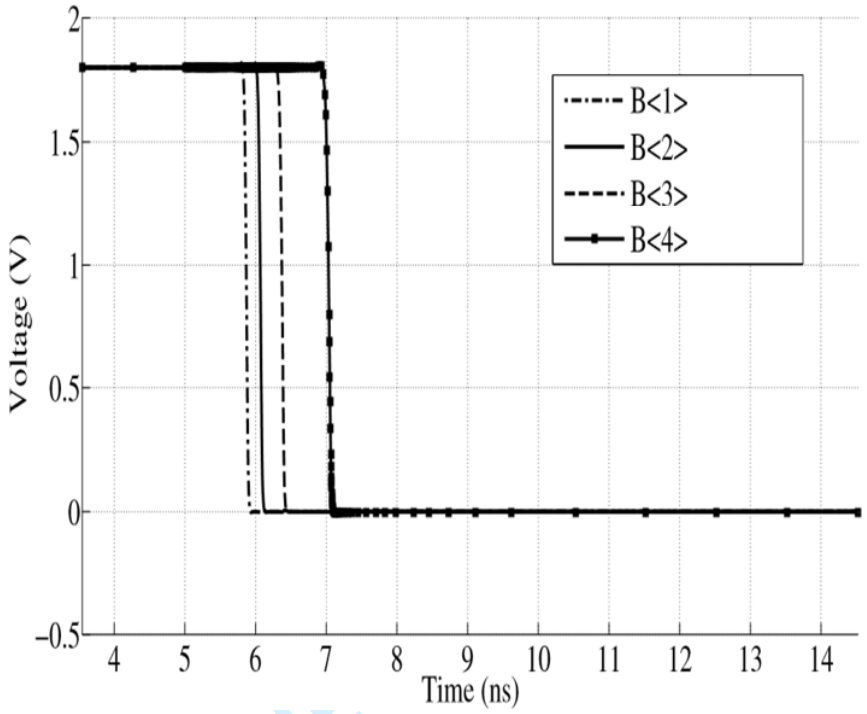


Figure6. Absolute difference (Error) between simulated characteristics and ideal characteristics.

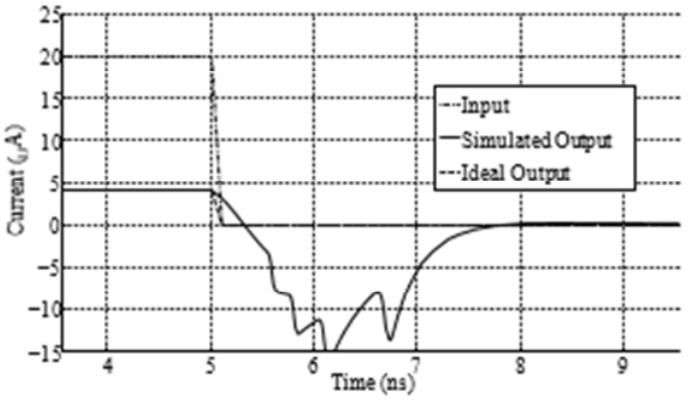


(a)

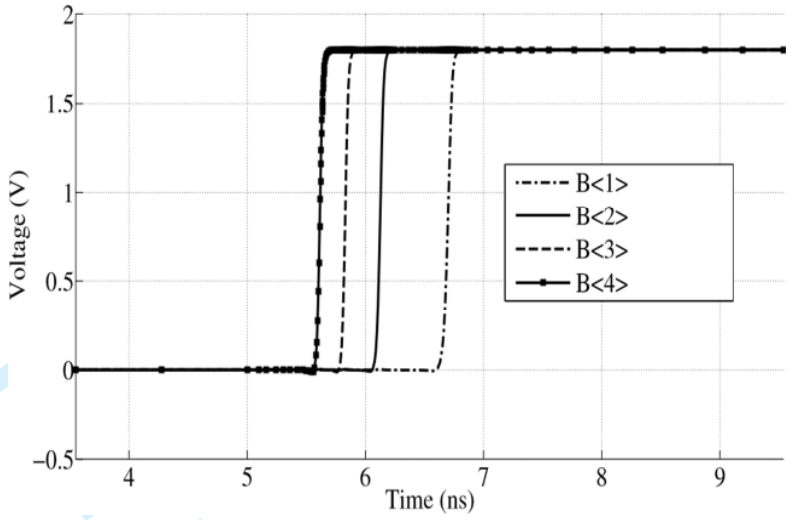


(b)

Figure7. Transient response for a full scale rising pulse



(a)



(b)

Figure8 .Transient response for a full scale falling pulse

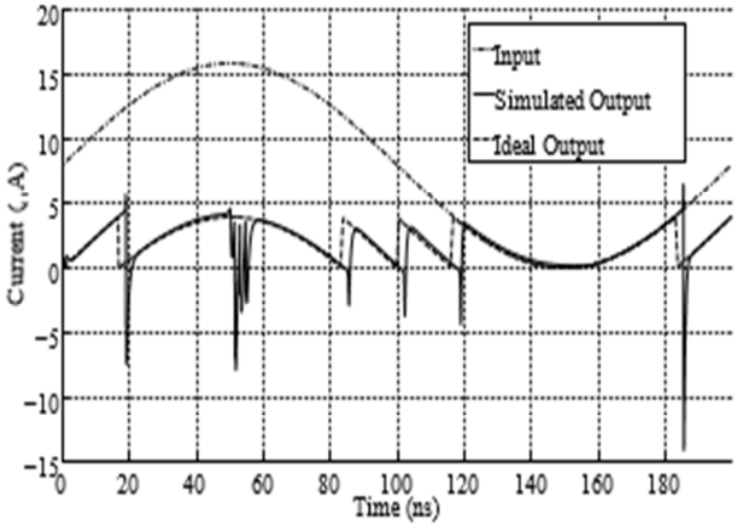


Figure9. Response to a sinusoidal signal of frequency 5MHz

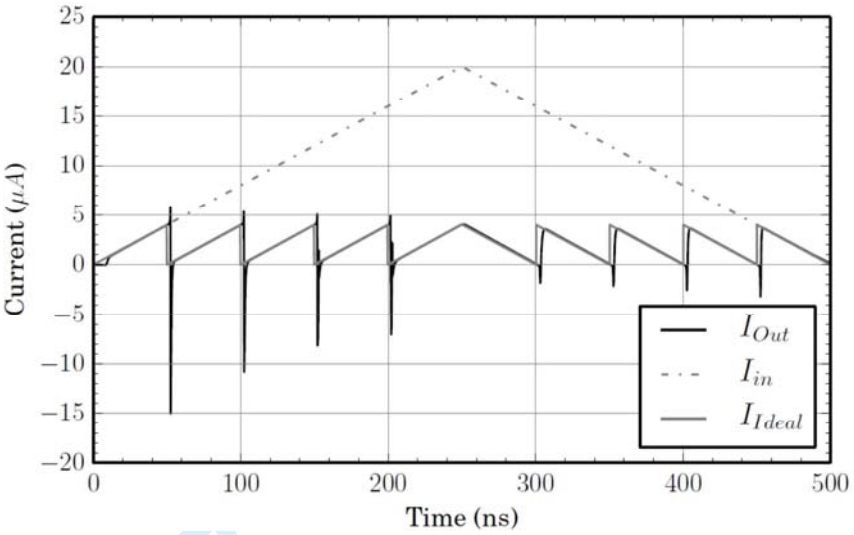


Figure10. Transient response to a triangular input signal

Finally, the performance of the proposed folding amplifier was tested under temperature variations. The circuit was simulated for temperature variations and the temperature was swept from -20° to 125° . Figure 11 shows a plot of the difference in the output current between the two extremes (125° and -25°). Inspection of Fig. 11 clearly shows that the performance of the proposed current-mode folding amplifier is highly insensitive to temperature variations.

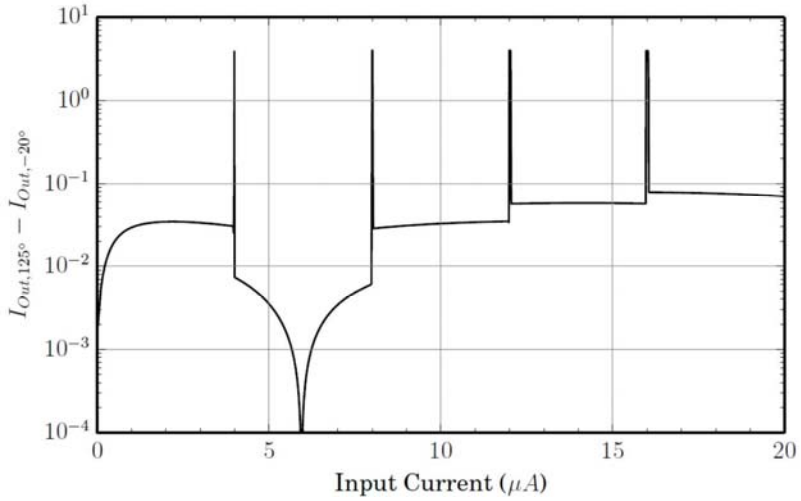


Figure11. Plot of the difference in the output current due to the temperature variation.

CONCLUSION

In this paper, a new 8-folds current-mode folding amplifier with minimal current mirrors count was presented. Only one current mirror is used in the path between the input and the output. Comparators were used to decide the switching points of the amplifier. The proposed folding amplifier was tested for a number of folds N=4. Simulation results show that the proposed folding amplifier can provide a four times faster full-scale response. The functionality of the proposed circuit was also tested using sinusoidal and triangular input currents. In both cases the circuit proved to be functioning as expected. Moreover, the scalability of the proposed circuit was tested and a folding amplifier with N=8 was designed and tested using the same building blocks. The results show that the proposed circuit is scalable with a slight change in the full scale time delay. This paves the way to develop folding amplifiers with number of folds N > 8 if a slight increase in the time delay can be tolerated. Simulation results also show that the performance of the proposed folding amplifier circuit is temperature insensitive over a wide range of temperature. Compared to previously published works, such folding amplifier can be a very useful building block for small area on the chip and high speed accurate ADCs. It is expected that further improvement in the current mirror settling time can substantially improve the performance of the proposed current mode folding amplifier

Acknowledgment

This work is a partial result of the project number ELE2146-04 supported by KACST under the National Science, Technology & Innovation Plan (NSTIP). The authors would like to thank KFUPM for support of this research.

References

[1] Oza, S., Devashrayee, N. Low voltage, low power folding amplifier for folding & interpolating ADC. In International Conference on Advances in Recent Technologies in Communication and *Computing,* Kottayam, Kerala, India, 2009, p. 178–182.

[2] Verbruggen, B. , Craninckx, J. , Kuijk, M. , Wambacq, P., Van derPlas G. A 2.2 mW 1.75 GS/s 5 bit folding flash ADC in 90 nm digital CMOS. *IEEE Journal of Solid-State Circuits*, 2009, vol. 44, no. 3, p. 874– 882.

[3] Jiang, F., Wu, D., Zhou, L., Wu, J., Jin, Z., Liu, X. An 8-bit 1 GS/s folding and interpolating ADC with a base-4 architecture. *Analog Integrated Circuits and Signal Processing*, 2013,vol. 76, no. 1, p. 139–146.

[4] Martinez, L. , Flores-Verdad, G. 7-bit 2.56 GS/s folding ADC with nanometric compatible architecture by using a high dynamic i/o folding amplifier. In *IEEE Fourth Latin American Symposium on Circuits and Systems (LASCAS)*, 2013, p. 1–4.

[5] Limotyrakis, S. , Nam, K., Wooley, B. Analysis and simulation of distortion in folding and interpolating a/d converters. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 2002, vol. 49, no. 3, p. 161–169.

[6] Leccese, F. A simplified 3–bits discrete pure linear analog preprocessing folding ADC architecture. In *Proceedings of 13th Workshop on ADC Modeling and Testing,* Florence, Italy, 2008, p. 22–24.

[7] Leccese, F. A 3 bits discrete pure linear analog preprocessing folding ADC architecture based on cascade controlled channels. In *XIX IMEKO World Congress on Fundamental and Applied Metrology*, Lispon, Portugal 2009, p.554-557

[8] Toumazou, C., Lidgey, F. , Haigh, D. *Analogue IC Design: The Current-mode Approach*. IET, Technology & Engineering. 1992.

[9] Li, Y., Sanchez-Sinencio, E. Current mirror based folding amplifier. In Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems, Lanseing M1, 2000, p. 60–63.

[10] Weng, R., Chao, C. A 1.5 v high folding rate current-mode folding amplifier for folding and interpolating ADC. In *IEEE International Symposium on Circuits and Systems, 2006.*

[11] Guo,W., Huber, R., Smith, K. A current steering CMOS folding amplifier. In *IEEE International Symposium on Circuits and Systems,* p. 141–144.

[12] Al Absi, M., Abuelma'atti, M., Mahemood, S. A new CMOS current-mode folding amplifier, *RADIOENGINEERING, JOURNAL*, 2013, vol. 22, no. 3, p. 892–898.

[13] Al Absi, M., Dhar, S., Abuelma'atti, M. , Elhassan, M. A new CMOS current mode fast folding amplifier. In *IEEE International Conference on Electronics Circuits & Systems*, 2014, p. 183–186.

[14] Mohanad A. M. Elhassan, Sagar K. Dhar, Munir A. AL-Absi and Muhammad T. Abuelma'atti. A New Fast and Accurate Current-Mode Folding Amplifier. In ELECO 2015, Bursa Turkey, p. 71-75.

[15] Flynn, M., Sheahan, B. A 400- msample/s, 6-b CMOS folding and interpolating ADC. IEEE Journal of Solid-State Circuits, 1998, vol. 33, no. 12, p. 1932–1938.

[16] Razavi, B. Design of Analog CMOS Integrated Circuits. Tata McGrawHill, Oct. 2002.

[17] Traff, H. Novel approach to high speed CMOS current comparators. *Electronics Letters*,1992, vol. 28, no. 3, p. 310–312.

[18] Moolpho, K., Ngarmnil, J. Sitjongsataporn, S. A high speed low input current low voltage CMOS current comparator. In Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS, p. 433-436–436.