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A new compact CMOS C-multiplier

Munir Ahmad Al-Absi[1] · **Eyas Saleh Al-Suhaibani**[1] · **Muhammad Taher Abuelma'atti**[1]

Abstract This paper presents a new compact CMOS capacitance multiplier. The multiplier is based on using the translinear principle with MOSFETs operating in sub-threshold region. The multiplication factor is controllable to meet the designer requirements. Tanner TSPICE simulator was used to confirm the functionality of the design in 0.18 μm CMOS Technology. The circuit operates from ±0.75 supply voltage. Simulation results indicate that the multiplication factor can be varied from 10 to 300. The functionality of the proposed capacitance multiplier was demonstrated by using it in designing a low pass filter and a relaxation oscillator.

Keywords Capacitance multiplier · Translinear loop · Low frequency filters · Biomedical circuits · Oscillators

1 Introduction

Integrated circuits are playing an increasing role in implantable biomedical systems. Such circuits must be designed to meet rigorous specifications especially area-on-the chip and power consumption. The signals generated by the human body have relatively very low frequencies, ranging from 1 Hz to less than 1 kHz. To process such signals using integrated circuit filters, there is always a need to realize large time constants in small area on the chip [16]. In order to implement such time constant, a large capacitance and/or a large resistance are needed. This would require large areas on the chip. But systems on-chip structures demand reduced silicon area as well as low voltage and low power consumption. Therefore, recourse to the well known capacitance multiplication technique is necessary to satisfy these requirements.

Over the years researchers developed several techniques to implement on-the-chip capacitance and impedance multipliers. In [4], a tunable C-multiplier is presented using an operational amplifier (OA) and two operational transconductance amplifiers (OTAs). Such implementation requires large area on the chip. An impedance scalar is presented in [12] using MOSFETs. This would require a small area on the chip. However, the scaling factor is decided by the aspect ratios of the transistors used. Thus, once fabricated it cannot be controlled. In [1], a current-conveyor based capacitance multiplier is presented. This approach requires a passive resistor and a relatively large area on the chip. In [15], a current- mirror based impedance scalar is reported. In this approach, the scaling factor depends on the aspect ratio of the mirror and hence limits the controllability of the impedance scalar. An immittance function simulator is reported in [6]. This approach uses at least three passive resistors. A current-conveyor based C-multiplier is presented in [10]. Again this design requires the use of passive resistors. In [11] and [14], an OTA-based C-multiplier and a dual differential amplifier C-multiplier are presented. Another complex design using the Sinh function is reported in [8]. This design uses log and anti-log circuits in addition to two nonlinear transconductors. In [13] a dual-X second-generation current-conveyor (DXCCII) based grounded capacitance multiplier is presented. The proposed design uses excessive number of transistors, two of them operated in the linear region, to implement the commercially unavailable DXCCII. A voltage-difference current-conveyor (VDCC)-based floating capacitor multiplier is presented in [9]. The circuit

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proposed in [7] is built around a current-controlled transconductance-amplifier (CCTA). Because of the use of resistors and/or integrated circuits the proposed implementations in [6–13] require relatively large area on the chip. Moreover, the scaling factor in the circuits proposed in [6–10] is fixed and cannot be controlled. In [2] a tow OTA based C-multiplier is presented, the multiplication factor is controlled by the bias current of the OTAs. A novel capacitance multiplier is presented in [5]. The design is based on current mirror. The problem of this design is that it works for small range of frequency namely 1–100 Hz.

In [3] a three novel C-multipliers are proposed and all the designs are based on current conveyor, improved current mirror and an OTA. The maximum scaling factor in these designs is 13.8.

It appears, therefore, that there is still a need for a new simple C-multiplier that occupies a relatively small area on the chip, consumes a relatively small power and enjoys controllability of the scaling (multiplication) factor. This paper presents a new MOS only C-multiplier based on the translinear principle using MOSFETs operating in the subthreshold region. Hence, low power consumption and small area on the chip are guaranteed. The proposed design also enjoys the attractive feature of controllable scaling factor.

2 Proposed C-multiplier

The circuit diagram of the proposed C-multiplier is shown in Fig. 1. The core circuit consists of four identical MOSFET transistors forming a translinear loop. Transistors M1 and M2 forms a regulated cascode topology which makes the node at the drain of M1 at low impedance and can sense the current from the capacitor. Also, it increases the high frequency corner. On the other hand, the subthreshold operation gives an advantage of a large output resistance which enhances the lower frequency corner of the operational range. With reference to Fig. 1, applying

Fig. 1 The proposed C-Multiplier

KVL to the translinear loop formed of transistors M1–M4 yields

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \tag{1}$$

The drain current of an NMOS operating in subthreshold forward saturation is given by:

$$I_D = \frac{W}{L} I_{DO} e^{\left(\frac{V_{GS} - V_{TH}}{nV_T} \right)} \tag{2}$$

In Eq. (2), I_{DO} is the saturation current, n is the slope factor and V_T is the thermal voltage.

To keep the MOSFETs operating in subthreshold forward saturation, the following conditions must be satisfied:

$$\frac{I_{DO}}{I_D} << 1 \text{ and } V_{DS} > 4V_T$$

Using Eq. (2) the gate-to-source voltage can be expressed as:

$$V_{GS} = nV_T \ln \left(\frac{I_D}{I_{DO}} \frac{L}{W} \right) + V_{TH} \tag{3}$$

Combining Eqs. (1) and (3) yields

$$I_{D1} I_{D2} = I_{D3} I_{D4} \tag{4}$$

In Eq. (4) $I_{Di}, i = 1, 2, 3, 4$ is the drain current of the transistor M_i.

To find the equivalent impedance Z_{eq} seen by the source V_x of Fig. 1, the current i_x must be calculated. With reference to Fig. 1, Eq. (4) can be rewritten as:

$$(i_o + I_4) \times I_3 = I_2 \times (I_1 + i_1) \tag{5}$$

or

$$(i_o + I_4) = G \times (I_1 + i_1) \tag{6}$$

where $G = \frac{I_2}{I_3}$.

From Eq. (6), if the current $I_4 = G \times I_1$ then $i_o = G \times i_1$.

With reference to Fig. 1, the impedance Z_{eq} is given by:

$$Z_{eq} = \frac{V_X}{i_X} = \frac{V_X}{i_1 + i_o} = \frac{Vx}{i_1 + Gi_1} = \frac{V_X}{i_1} \frac{1}{(G + 1)} \tag{7}$$

Assuming Z>> the impedance at the node of M1 because it is a regulated cascode then

$\frac{V_X}{i_X} = Z$ and Eq. (7) can be written as

$$Z_{eq} = \frac{Z}{(G + 1)} \tag{8}$$

It is clear from Eq. (8) that if Z is replaced by a capacitance then a capacitance multiplier can be achieved with a multiplication factor = G + 1. Thus, the capacitance multiplication factor can be controlled by adjusting the controlling variable $G = \frac{I_2}{I_3}$. This feature will allow scaling the capacitance up and down by adjusting the bias currents I_2 and/or I_3. However, this implies that the bias

currents I_1 and/or I_4 must be changed accordingly so as to keep $I_4 = GI_1$. This can be easily achieved if the relevant currents are mirrored from the same current source.

3 Simulation results

To test its functionality, the proposed circuit was simulated using Tanner TSPICE in 0.18 μm CMOS process with BSIM3V3 MOS model. The aspect ratio of all transistors was set to 7/2 μm and the circuit was powered using ±0.75 V. The currents I_1 and I_3 were set to 10 nA, the current I_4 was monitored to keep $I_4 = GI_1$ and the capacitor to be multiplied was set to 3 pF. The current I_2 was swept from 10 nA to 3 μA corresponding to a multiplication factor from 1 to 300 times.

To find the value of the effective capacitance, the proposed circuit was used in designing a low pass filter using 1 MΩ resistance in series with the C-multiplier. Then, by measuring the −3 dB frequency of the filter for each value of I_2, the value of the effective capacitance was calculated and plotted against the expected capacitance multiplication factor. The simulation results shown in Fig. 2 indicate that the proposed circuit is functioning properly with some deviations from the theoretical results.

It can be seen from Fig. 2, that there is a deviation between the calculated and simulated results especially for large values of the multiplication factor. This may be attributed to the non-ideal behavior of the current mirrors involved in providing the bias currents and/or the effect of the parasitic capacitances associated with the drain terminal of transistor M1. Moreover, the output resistance of the transistor M4 will vary with the bias current and it may contribute to the error as well.
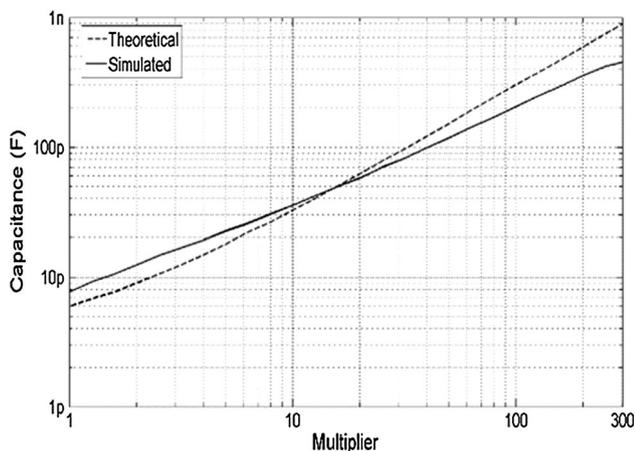
The proposed C-multiplier circuit was simulated for temperature variations with a capacitance multiplication factor G = 100. This capacitor was used in a low pass filter with the 1 MΩ resistor connected in series. The temperature was varied from 0 to 100°C and the value of the simulated capacitance was monitored. The simulation results shown in Fig. 3 indicate that the transfer characteristic of the resulting low pass filter is almost insensitive to temperature variations.

To study the effect of transistors mismatch on the performance of the proposed C-multiplier, Monte Carlo analysis was carried out when the multiplication factor set to 100 for 100 iterations using the statistical model of 0.18 μm CMOS technology. The simulation results shown in Fig. 4 indicate that the proposed design is insensitive to mismatch in transistor aspect ratios. It is worth mentioning here that the circuit works properly for a maximum input signal of 0.5 V. This range can be extended by increasing the aspect ratios of the MOSFETs to assure subthreshold mode of operation.

The performance of the proposed C-multiplier was compared with previously published similar circuits. The results are shown in Table 1. Inspection of Table 1 clearly shows that the proposed C-multiplier is superior to all previously published circuits.

The variation of the reactance of the C-multiplier with frequency was checked and the results are shown in Fig. 6. Inspection of Fig. 5 clearly shows that the reactance of the capacitance is decreasing with the increase in frequency and the phase angle is 90 degrees in the frequency range from 100 Hz to 1MHZ. Thus, the proposed C-multiplier works properly in the frequency range from 100 Hz to 900 kHz.

The proposed circuit was simulated for time domain analysis in which the capacitor was used in the design of a
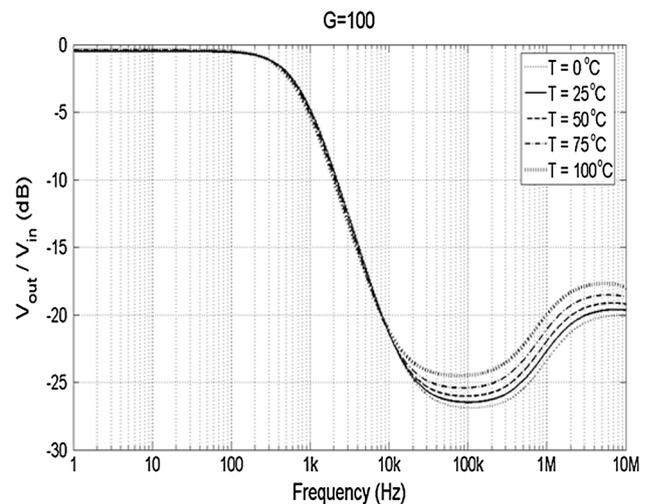

Fig. 2 Variation of the simulated and calculated capacitance with the multiplication factor

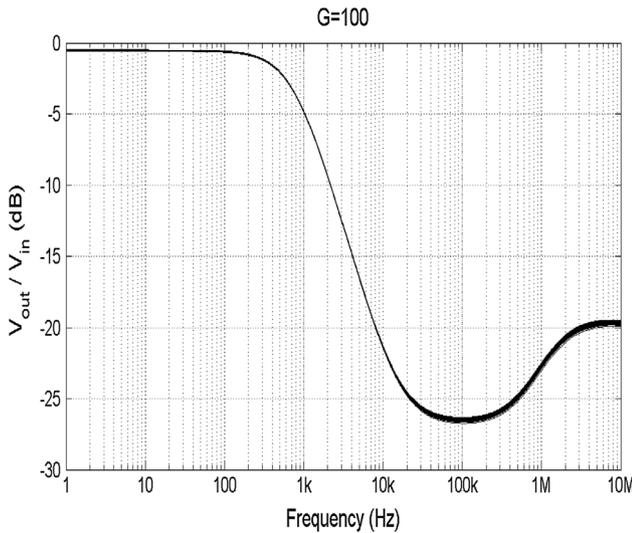Fig. 3 Simulation result for temperature analysis

Fig. 4 Monte Carlo simulation results for transistors mismatch

Table 1 Performance comparison

	Max. scaling factor	Power consumption	Area mm^2
Ref. [12].	Fixed 10	10.8 mW	0.0297
Ref. [11].	Fixed 10	0.5 µW	–
Ref. [8].	Fixed 28	6.77 mW	0.0171
This work	Variable 10 to 300	15.41 µW (G = 300)	0.0014
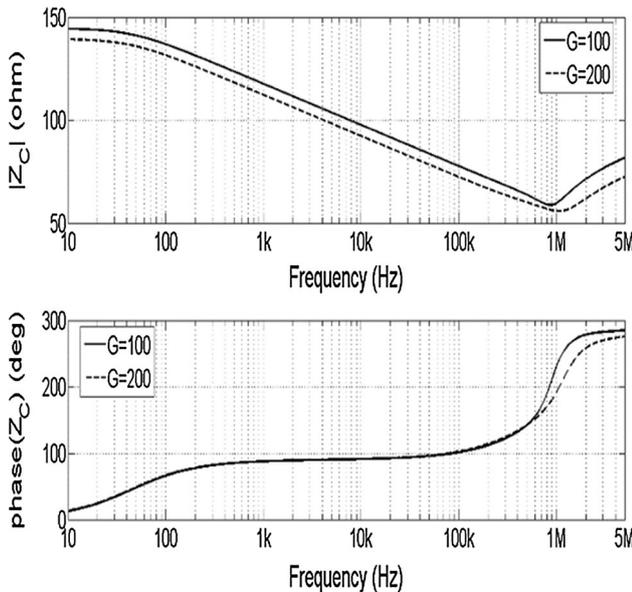
Fig. 5 Variation of the reactance and phase shift of the C-multiplier with frequency

Fig. 6 Simulation results for time domain analysis
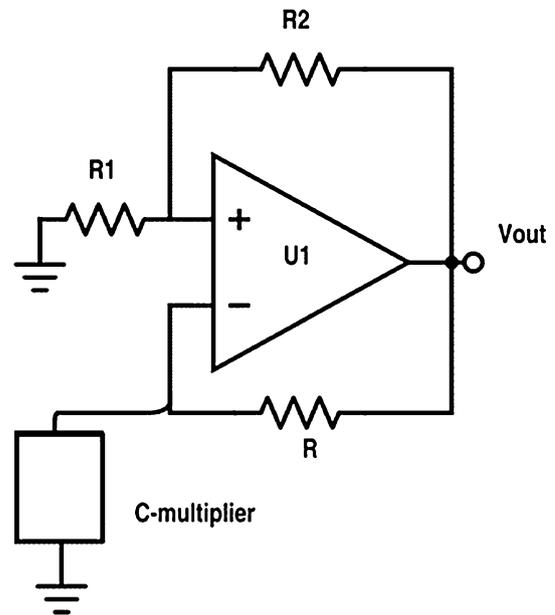
Fig. 7 Relaxation oscillator using C-multiplier

low pass filter. The low pass filter was excited by a sinusoidal input and the output was monitored. The simulation results obtained are shown in Fig. 6 along with the ideal RC filter output. Simulation results shown in Fig. 6 confirms that functionality of the design.

Finally, the proposed C-multiplier was used in the design of the tunable relaxation oscillator circuit shown in Fig. 7. A single stage Op-Amp powered by ±1.5 V was used $R_2 = R = 1$ MΩ and R1 = 100 KΩ. The capacitance to be multiplied is set to 10pF and the multiplication factor G was varied from 100 to 300 in step of 50. The simulation results shown in Fig. 8 confirms the functionality of the proposed C-multiplier in designing a tunable relaxation oscillator.
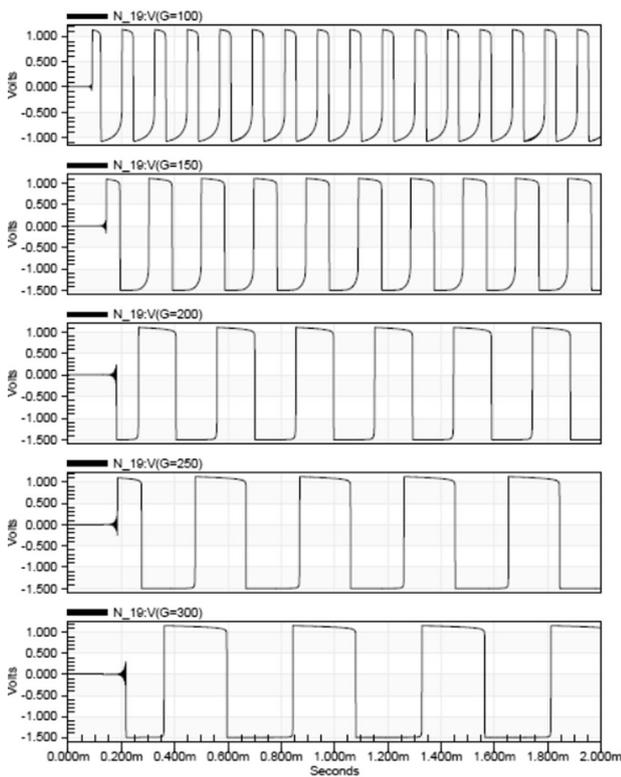
Fig. 8 Simulation results of the tuned relaxation oscillator
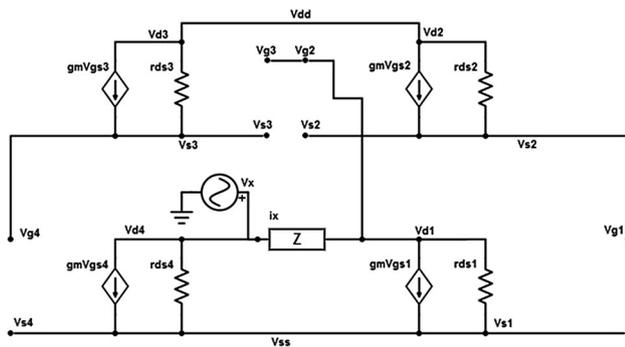
Fig. 9 Circuit used to find the equivalent input impedance

4 Non-ideal analysis

The small signal equivalent circuit of the proposed C-multiplier including the drain-to-source resistances of the transistors is shown in Fig. 9. Routine analysis shows that the equivalent input impedance of Fig. 9 can be expressed as

$$Z_{eq} = \frac{Z}{1 + g_{ds4}Z + \frac{\frac{g_{m3}g_{m4}Z}{g_{m3}+g_{ds3}}-1}{g_{ds1}Z+\frac{g_{m1}g_{m2}Z}{g_{m2}+g_{ds2}}+1}} \tag{9}$$

In Eq. (9) $g_{dsi} = \lambda I_{Di}, g_{mi} = \frac{I_{Di}}{nV_T}$, $i = 1, 2, 3, 4$.
Since $g_{mi} >> g_{dsi}$, Eq. (9) can be reduced to

$$Z_{eq} = \frac{Zg_{m1}+1}{g_{m1}\left(1+\frac{g_{m4}}{g_{m1}}\right)} = \frac{Z}{1+G} + \frac{1/g_{m1}}{(1+G)} \tag{10}$$

Comparing Eqs. (8) and (10) it is clear that the term $\frac{1/g_{m1}}{1+G}$ is the source of the error. This implies that the realized capacitance will be lossy a with series connected resistance $= \frac{1/g_{m1}}{1+G}$. Thus, by proper selection of the bias current I_1, the effect of non-idealities can be minimized.

5 Conclusion

In this paper, a new C-multiplier has been presented. The proposed design uses four MOSFETs and four DC current sources. The multiplication factor can be easily controlled by adjusting the DC current sources. The functionality of the C-multiplier was confirmed using Tanner TSPICE simulation tools in 0.18 μm CMOS technology. The design is compact, consumes a relatively small area on the chip and provides a large multiplication factor for capacitance and is insensitive to temperature variations. The design is also insensitive to mismatch in device dimensions. The proposed design can be used in integrated circuit design where large time constant is required, for example in designing very low frequency active filters for biomedical applications and tunable oscillator.

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