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A new CMOS current-mode controllable-gain square rooting circuit using MOSFET in subthreshold

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Abstract A new controllable-gain square rooting circuit using MOS transistors working in weak inversion is proposed. The proposed circuit can be configured to compute the geometric mean between two signals and the square root of the inverse of a signal. Tanner tool is used to confirm the functionality of the circuit in 0.18 μm CMOS TSMC process technology. Simulation results show a 3 dB bandwidth of 2 MHz and a relative error of about 2.4 %. The maximum power consumption is 1.73 μW. The proposed circuit is attractive for low power and low current applications.

Keywords Translinear principle · Current mode · Square-root

1 Introduction

Square rooting circuit is one of the most important building blocks used in instrumentation and analog signal processing. It can be used to linearize the output from a flow meter or differential pressure sensors. It also can be used to find the geometric mean of two signals. There are many square rooting circuit reported in the literature. One approach uses devices such as OTA, Op-Amps, current conveyers, and different devices such as the circuits reported in [1–4]. The problem with this approach is that the circuit will consume relatively more power than using CMOS transistors. Many of the CMOS-transistor based square rooting circuits use MOSFETs operating in strong inversion as in [5, 6] and the references cited therein. In [7] square rooting circuit based on MOS transistor operating in weak inversion is presented. The drawback of this design is the use of the back gate of a MOSFET. This approach suffers from the error associated with body effect. Moreover, it uses a capacitor that will occupy relatively large area on the chip. Also, its gain can only be controlled by a reference current source which makes the gain controlling feature very limited.

In this paper, a new current-mode controllable-gain square rooting circuit based on MOS transistors operating in weak inversion is proposed. The rest of the paper is organized as follows: The prosed circuit is presented in Sect. 2. Section 3 presents the simulation results and discussion. The paper conclusion is presented in Sect. 4.

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2 Proposed circuit

The proposed square-rooting circuit is shown in Fig. 1. It consists of six-matched transistors M_1 to M_6 forming a translinear loop. Transistors M_7, M_a and M_b are used to produce the output current. All of these transistors are working in subthreshold region. The current I_1 is the input where I_2, I_3 and I_5 are used for biasing and gain control.

Appling KVL to the translinear loop yields the following:

$$V_{GS1} + V_{GS2} + V_{GS3} = V_{GS4} + V_{GS5} + V_{GS6} \quad (1)$$

The drain current of a transistor working in subthreshold forward saturation is given by:

$$I_D = \frac{W}{L} I_{D0} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)} \quad (2)$$

where, W and L are the channel width and length respectively, V_T is thermal voltage, n is the subthreshold slope

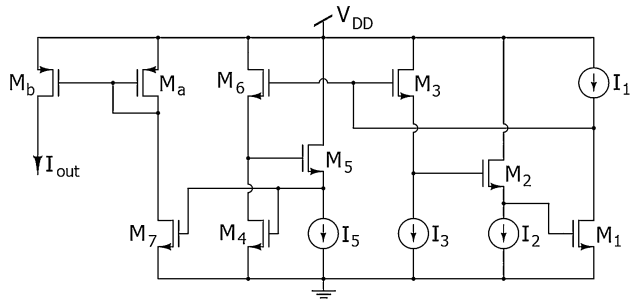

Fig. 1 The circuit diagram of the proposed square rooting circuit

factor, V_{Th} is the threshold voltage and I_{D0} is a device dependent parameter.

Assume all the transistors forming the translinear loops are matched, it is easy to show that

$$I_1 I_2 I_3 = I_4 I_5 I_6 \tag{3}$$

where, I_i is the drain current for the transistor M_i.

With reference to Fig. 1, $I_4 = I_6$, (3) can be rewritten as:

$$(I_4)^2 = \frac{I_1 I_2 I_3}{I_5} \tag{4}$$

$$Or I_4 = \sqrt{\frac{I_1 I_2 I_3}{I_5}} \tag{5}$$

The current I_4, is mirrored by transistor M_7. The current I_7 is considered to be the output current and it is mirrored by M_b and M_a to the load. The purpose of current mirror in the output is to provide large output impedance. Thus,

$$I_{out} = \sqrt{\frac{I_1 I_2 I_3}{I_5}} = K\sqrt{I_1} \tag{6}$$

where $K = \sqrt{\frac{I_2 I_3}{I_5}}$

It is clear that (6) implements the square root function for the input signal represented by the current I_1 and the gain can be controlled by K. This gain controllability is the main advantage of the proposed circuit over most of square rooting circuits reported in the literature. Moreover, the circuit has multiple inputs which make it useful to perform other functions. The proposed circuit can be used to compute the geometric mean between two signals (where the inputs are I_1 and I_2) with controllable gain using I_3 and I_5. Also, it can be used to compute the square root of an inversed signal where the input in this case is I_5. It also can be used as a controllable gain amplifier if the input current is fed to both I_1 and I_2 where I_3 and I_5 control the gain.

3 Simulation results and discussion

The proposed circuit was simulated using Tanner with Bsim3v3 model in 0.18 µm CMOS process technology. The power supply voltage (V_{DD}) is equal to 1 V. The current $I_2 = I_3 = I_5 = 30$ nA and the input current I_1 was swept from 0 to 500 nA. The transistors sizes used for simulation are shown in Table 1.

Simulated and calculated results for the DC characteristics of the controllable gain square rooting circuit are shown in Fig. 2. Figure 3 shows the DC characteristics of the controllable gain square rooting circuit for three different values of I_2($I_2 = 30$, 90 and 150 nA). This proves the gain controllability of the proposed circuit. The proposed circuit has a relatively wide dynamic range and relative error of about 2.4 % over the entire input current range. The maximum power consumption was found to be around 1.73 µW.

Simulation for AC analysis was carried out. Figure 4 shows the frequency response of the proposed circuit. The proposed circuit has a bandwidth of 2 MHz.

Transient analysis also carried out. Figure 5 shows the output current when the input is a triangular signal with frequency of 20 kHz where all inputs are set to 30 nA.

Table 1 Transistors aspect ratios of the proposed circuit

	M_a and M_b	M_1–M_7
W/L (µm/µm)	1.5/6	15/0.5

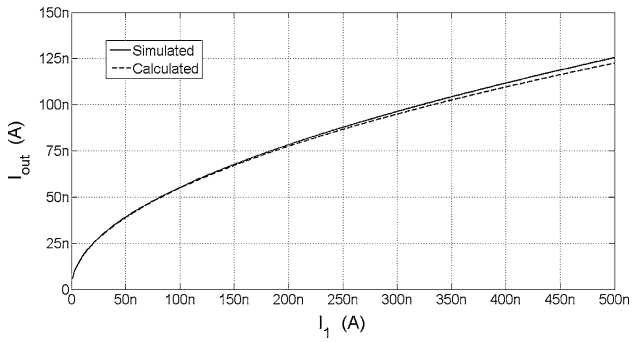

Fig. 2 DC characteristic for simulated and calculated output current

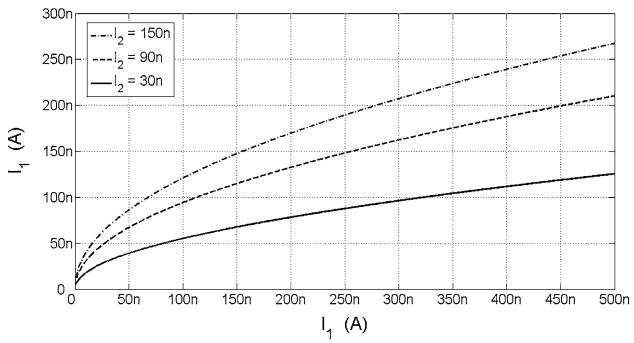

Fig. 3 DC characteristic for with different gains

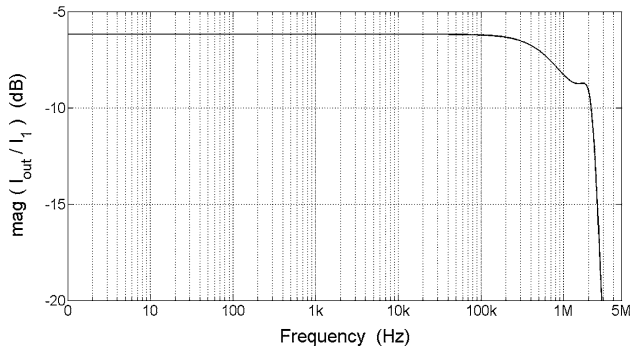

Fig. 4 Frequency response of the proposed circuit

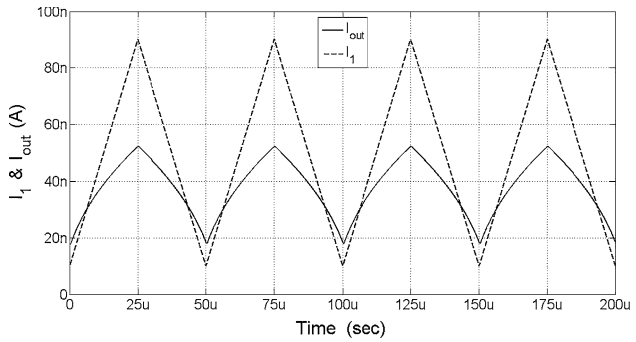

Fig. 5 Transient response of the proposed circuit

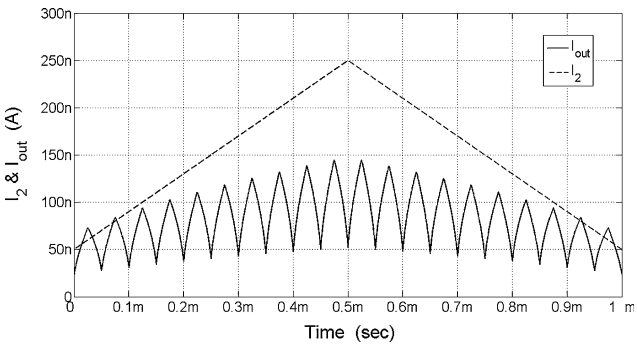

Fig. 6 Transient response of the proposed circuit as the gain changes

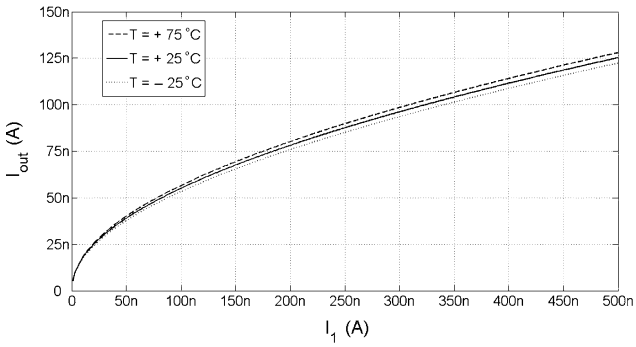

Fig. 7 DC characteristic under different operating temperature

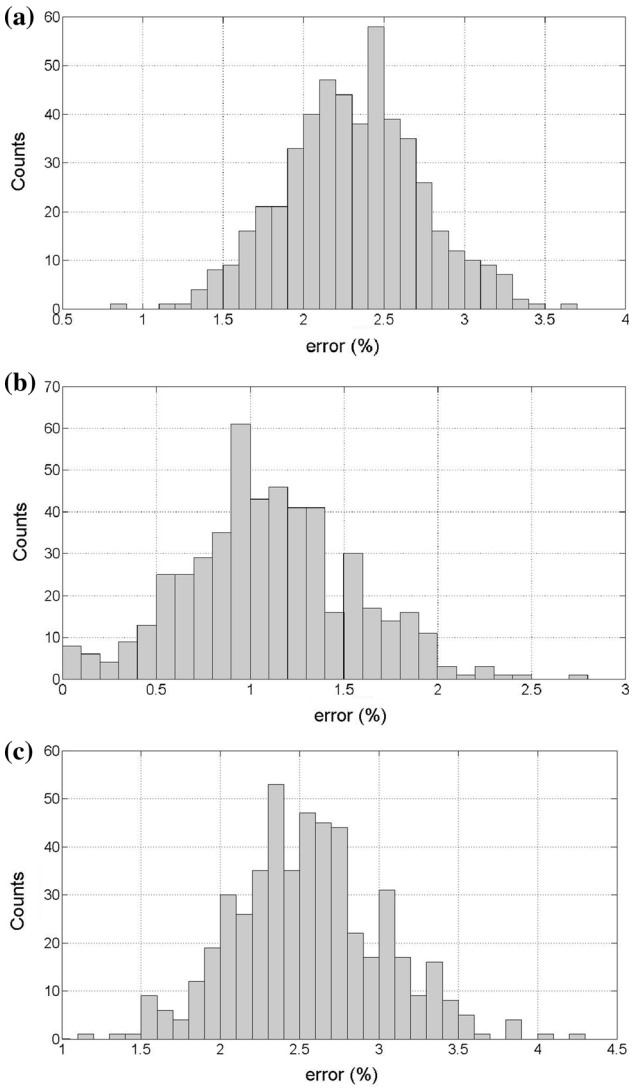

Fig. 8 Relative error distribution when running Monte Carlo analysis for 500 iterations under three different gain values. **a** $I_2 = 30$ nA. **b** $I_2 = 90$ nA. **c** $I_2 = 150$ A

Table 2 Summary of Monte Carlo analysis results

	Figure 8(a)	Figure 8(b)	Figure 8(c)
Average (%)	2.3091	1.1042	2.5558
Standard deviation (%)	0.428	0.450	0.469
Variance	0.183	0.203	0.220

Figure 6 clarifies the gain controllability of the proposed circuit. The input (I_1) is a triangular signal with a frequency of 20 kHz. Then, I_2 is used to change the gain by changing its value from 50 to 250 nA and then back to 50 nA. It is clear from the figure that as I_2 changes, the amplitude of the output current changes accordingly.

Simulation of the circuit for temperature analysis was carried out. The temperature was varied from −25 to

75 °C. The simulation result of the DC characteristic for different temperature is shown in Fig. 7. It is clear from the figure that the variation in the output current is relatively small. It is also clear that the error due to temperature variation is gain error and because of the gain controllability feature of this circuit, this error can be easily minimized.

To study the effect of mismatch in transistors, Monte Carlo analysis was carried out using the statistical model for 0.18 μm CMOS technology. The analysis was done on three different gain values (namely, when $I_2 = 30$, 90, and 150 nA). In each case, the analysis was done for 500 iterations and the relative error was measured in every iteration. Figure 8 shows the error distribution in each case. Table 2 summarizes the results for each case. As it is clear from the results, the average relative error is 2.6 % with standard deviation of around 0.5 %. Thus, the circuit error is reasonably small with very small variation from average relative error.

4 Conclusion

A new current-mode square rooting circuit with controllable gain is developed. The proposed circuit use MOSFETs working in subthreshold region which makes it attractive for low power and low current applications. The circuit's bandwidth is relatively large and it consumes low power. The circuit is useful block in many signal processing applications like biomedical and in instrumentation.

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