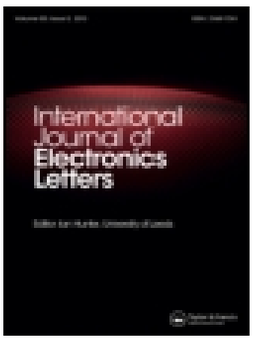

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A new 8-fold CMOS current-mode sawtooth folding amplifier

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ABSTRACT

This paper presents a new 8-fold current-mode sawtooth folding amplifier. In the proposed circuit the number of current mirrors in the signal path between the input and the output is minimised. This results in minimising the delay in the signal path of the 8-fold current-mode sawtooth folding amplifier. Thus, the speed of the proposed amplifier is improved while enjoying a compact design and consuming less DC power. The functionality of the proposed circuit was tested and confirmed using LFoundry 150 nm process in Cadence simulation tools. Simulation results show that 8.4 ns settling time for the full-scale rising edge and 3.5 ns for the full-scale falling edge can be achieved. For comparison with already existing folding amplifiers, the proposed circuit was scaled down to provide four folds. Simulation results obtained from the 4-fold amplifier show that a full-scale delay of 5.9 ns can be achieved. This is more than four times faster than already existing designs in the open literature. Furthermore, the simulation results obtained from a sinusoidal and a triangular input current confirm the workability of both the 4-fold and the 8-fold amplifiers. The simulation results also show that the circuit is temperature insensitive and is functioning as expected in the temperature range −25°C to 125°C.

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Folding amplifier; current mode; analogue-to-digital converter; folding flash; saw tooth

Introduction

Analogue-to-digital converters (ADC) are basic building blocks in modern mixed-mode analogue and digital signal processing. This justifies the quest for designing low-voltage, low-power, high-speed and compact ADCs. Over the years different architectures of ADCs have been developed. Among the available ADC designs it is well known that the full-flash ADC is the fastest. Unfortunately, an N-bits full-flash ADC requires $2^N - 1$ comparators and 2^N equal-value resistors. This would require large area on the chip and consume relatively large powers. The full-flash ADC is, therefore, considered to practical only for relatively small number of bits. Fortunately, using the concept of folding ADC can reduce the number of active and passive components of flash ADC with a reasonable cost in terms of reducing the conversion speed of the ADC. In a folding ADC a folding amplifier must be used. In order to avoid the use of correcting

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circuits to reduce the errors resulting from the folding process, it is preferable to use a folding amplifier with sawtooth input–output characteristics.

Conventional voltage-mode folding amplifiers have been reported in the literature (Jiang, Wu, Zhou, Wu, Jin and Liu, 2013; Leccese, 2008, 2009; Limotyrakis, Nam, & Wooley, 2002; Martinez & Flores-Verdad, 2013; Oza & Devashrayee, 2009; Verbrugegen, Craninckx, Kujik, Wambacq and Van der Pals, 2009). The ADCs reported in Jiang et al. (2013), Martinez and Flores-Verdad (2013), Oza and Devashrayee (2009) and Verbruggen et al. (2009) use voltage-mode folding amplifiers. Unfortunately, the transfer characteristics of these folding amplifiers are either sinusoidal or triangular. Folding ADCs exhibiting such nonlinear sinusoidal or triangular transfer characteristics cause error in digitisation (Limotyrakis et al., 2002). Thus, additional circuits would be required for error correction/compensation. Obviously this would increase the power consumption and the area on the chip and may add additional time delay. Moreover, the nonlinearity of the differential amplifier used would limit the operation of the folding amplifier to relatively large voltages, and the circuits proposed in Jiang et al. (2013), Martinez and Flores-Verdad (2013), Oza and Devashrayee (2009) and Verbruggen et al. (2009) would not be suitable for low-voltage applications. In Leccese (2008, 2009) the proposed voltage-mode folding amplifiers offer sawtooth transfer characteristics. However, the proposed circuit requires exact generation of voltages which require additional power management circuitry.

Recently the current-mode approach has attracted the attention of many designers. This is attributed to the simple circuitry, faster response and low-voltage operation of current-mode circuits compared to the voltage-mode counterparts (Toumazou, Lidgey, & Haigh, 1992). It is, therefore, anticipated that current-mode folding amplifiers exhibiting sawtooth transfer characteristics would be faster, more compact and consumes less DC power. However, despite these obvious advantages that make such amplifiers excellent candidates for the design of improved flash-folding ADCs, only very few current-mode folding amplifiers are reported in the open literature (Elhassan, Dhar, Al-Absi and Abuelma'atti, 2015; AlAbsi, Abuelma'atti and Mahemood, 2013; AlAbsi, Dhar, Abuelma'atti and Elhassan, 2014; Guo, Huber, & Smith, 2002; Li & Sanchez-Sinencio, 2000; Weng & Chao, 2006).

In Li and Sanchez-Sinencio (2000) and Weng and Chao (2006), the authors present current mirror-based folding amplifiers exhibiting triangular transfer characteristics. This may result in conversion error in the ADC applications and would require further correction circuits, more power consumption and area on the chip in addition to possible delays. The current-mode folding amplifier reported in Guo et al. (2002) uses the current steering technique and exhibits a sinusoidal transfer characteristics. Again, this would lead to errors in ADC applications and would require further correction circuits with possible delays, additional area on the chip and increased power consumption. In Al Absi et al. (2013) a current-mode folding amplifier with sawtooth transfer characteristics was reported. The proposed folding amplifier uses two building blocks. The first block produces the linear portion of the sawtooth characteristics. The second block produces the sharp transition of the sawtooth characteristics. However, obtaining this sharp transition requires current mirrors with large current ratios. This would require large-size transistors and would result in slower response of the overall folding amplifier. A regeneration of the folding amplifier reported in Al Absi et al. (2013) shows a response

time of about 235 ns when the circuit is simulated using 0.35 μm technology. This is a relatively large delay which will be a major drawback for the realisation of a high-speed folding ADC.

A new design for a 4-fold current-mode folding amplifier with sawtooth transfer characteristic was presented in Al Absi et al. (2014). The response time of this design was found to be 25 ns. In terms of speed and accuracy it was also observed that, in the design of current-mode folding amplifier with sawtooth transfer characteristics, the major bottleneck is the number of current mirrors required in the path between input and output. This is attributed to the relatively long time required to charge (or discharge) the relatively large pair of gate-to-source capacitances ($2C_{GS}$) especially when switching OFF or ON. As such it is desirable to reduce the number of current mirrors in the signal path between input and output.

In Elhassan, Dhar, Al-Absi and Abuelma'atti (2015), a further improvement of the 4-fold folding amplifier has been presented. The proposed circuit, using the minimum number of current mirrors in the signal path, was simulated using LFoundary 150 nm technology in Cadence Tools. Simulation results shows a 5.9 ns full-scale delay time from input to output. This is far better than the results reported using the circuits presented in Al Absi et al. (2013, 2014).

The major intention of this paper is to build upon the results obtained in Elhassan, Dhar, Al-Absi and Abuelma'atti (2015) and to present an 8-fold current-mode folding amplifier. For further investigation of the folding amplifier performance, the paper will also present results obtained from the transient analysis of the folding amplifier excited by a triangular input current, a sinusoidal input current and the effect of temperature variations on the performance of the amplifier.

Proposed current-mode folding amplifier

Figure 1 shows the block diagram of an ADC based on the folding amplifier concept. The folding amplifier is characterised by (a) its number of folds, N, and (b) the fold size I_F. The function of the folding amplifier is simply to map the input into the output in a modulo division fashion (Flynn & Sheahan, 1998; Guo et al., 2002). This can be explained as follows: As long as the signal current is larger than the fold size, the current I_F is repeatedly subtracted from signal current until the signal current becomes smaller

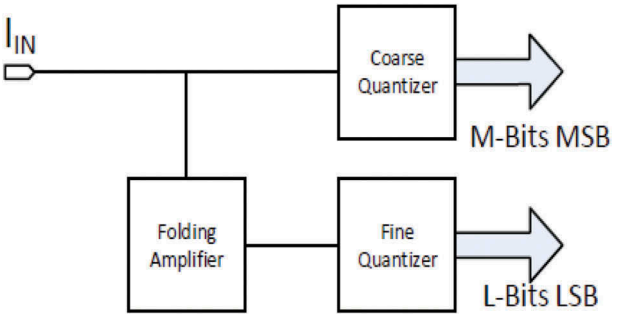

Figure 1. The concept of current-mode folding-amplifier-based ADC.

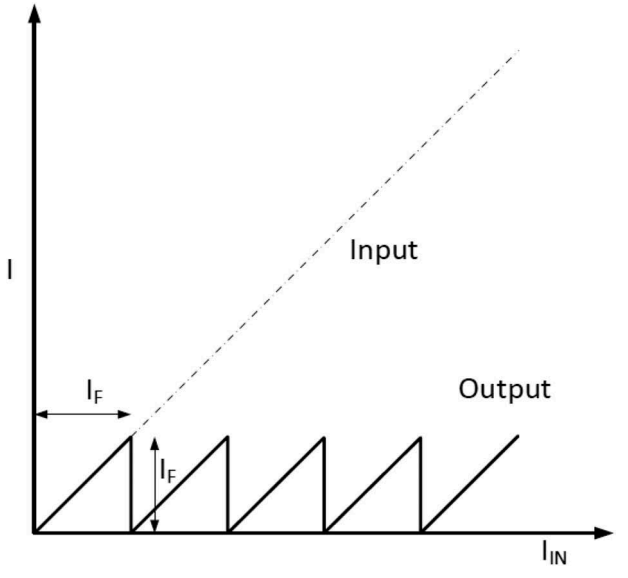

Figure 2. The sawtooth input–output characteristic of the current-mode folding amplifier.

than the fold size I_F. The result is a sawtooth transfer characteristic as shown in Figure 2. The transfer characteristic of Figure 2 can be realised as follows. First, the input current is mirrored to the output via a current copier. Second, once the value of the input current is beyond certain points, the value of the fold size I_F is successively subtracted from the output current. Obviously, these points are: I_F, $2I_F$, $3I_F$,…,$(N-1)I_F$ for an N-fold amplifier.

The work presented in this paper is an extension of the work proposed in Elhassan, Dhar, Al-Absi and Abuelma'atti (2015). The block diagram of the circuit proposed in Elhassan, Dhar, Al-Absi and Abuelma'atti (2015) is reproduced here and is shown in Figure 3. The block diagram shown in Figure 3 shows a possible implementation of the modulo division concept previously described. As shown in Figure 3 the proposed

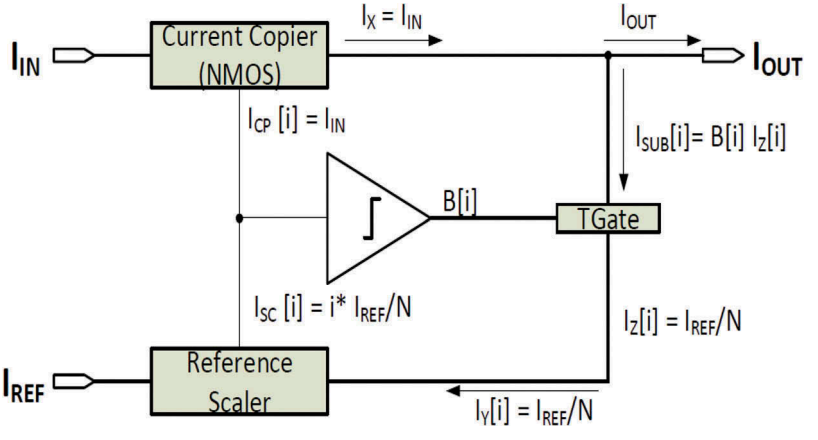

Figure 3. Block diagram of the proposed design of current-mode folding amplifier with sawtooth transfer characteristics.

current-mode amplifier with sawtooth input–output characteristic has two inputs: namely the input current signal I_{IN} and a reference current I_{REF}. The fold size in this case is $I_F = I_{REF}/N$ where N is the number of folds. The current I_{IN} is fed to the current copier. The output of the current copier is formed of N currents; $N - 1$ outputs are shown as I_{CP} in Figure 3 and one copy is shown as I_X in Figure 3. The current I_{REF} is fed to the reference scaler. The output of the reference scaler is formed of $2(N - 1)$ output currents. Of these currents $(N - 1)$ output currents are scaled as I_{REF}/N, $2I_{REF}/N$,. . .,$(N - 1)$ I_{REF}/N and are shown as I_{SC} in Figure 3. The other $(N - 1)$ output currents are all equal to I_{REF}/N and are shown as I_Y in Figure 3. The currents I_{SC} and I_{CP} are subtracted and fed to the current comparator which will provide output voltage $B[i]$ = logic 1, for $I_{CP}[i] < I_{SC}[i]$ for i = 1,2,. . .,$N - 1$. The binary voltage signal $B[i]$ is then used to switch on/off the ith transmission gate (shown as TGate) which subtracts a current $I_F = I_{REF}/N$ from the output. This will realise the folding. It is worth mentioning here that the input current and the output current are separated by only one current mirror. Thus, the minimum number of current mirrors is used in the path between the input current and the output current of the proposed structure.

Figure 4 shows the circuits used to implement the blocks shown in Figure 3. Instead of using large channel length transistors in the current mirrors as in Al Absi et al. (2014) a folded cascode mirror is used for all the current mirrors (Razavi, 2002). This allows the use of smaller channel length transistors (300 nm for all mirroring transistors) while not sacrificing the accuracy (simulation results show that all mirrors give less than 2% error for currents in the range 1 – 32 μA). In Figure 4(b), the IY output terminals of the current scaler are not shown as they are similar to those used in the current copier of Figure 4(a). The cascode transistors used in Figure 4(a,b) are biased by a diode-

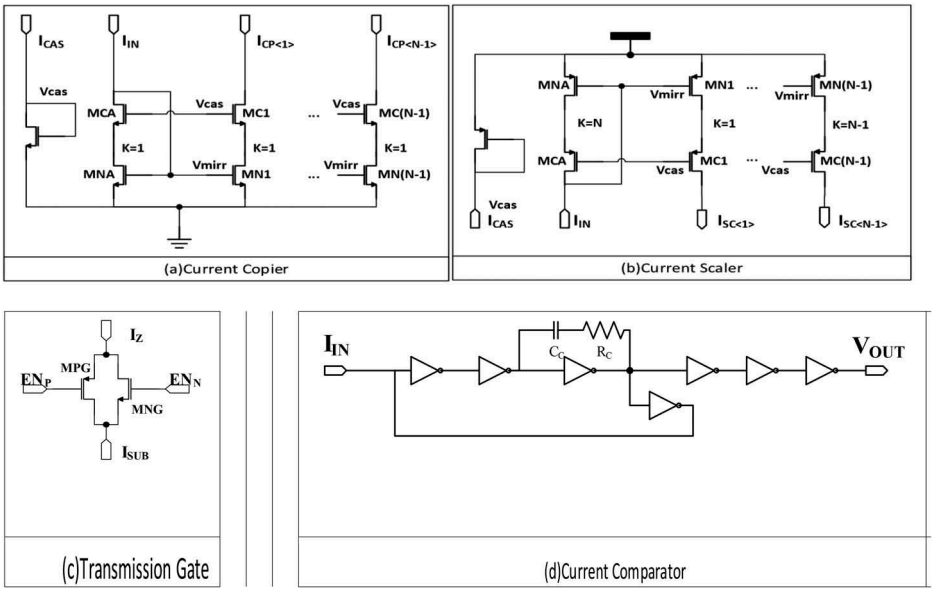

Figure 4. Circuit diagrams of the blocks used for the implementation of the proposed current-mode folding amplifier: (a) current copier; (b) reference current scaler; (c) transmission gate; and (d) current comparator with input current and output binary voltage.

configured transistor which is half the width of the main transistor and biased by *I*CAS = 35 µA.

Simulation results

The proposed 8-fold current-mode folding amplifier was simulated in LFoundry 150 nm process with a supply voltage of V_{DD} = 1.8 V. The sizes of all transistors used are shown in Table 1. To compare with the results reported in Al Absi et al. (2014), a 4-fold current-mode folding amplifier was also designed. In both cases the fold size was 4 µA and the load resistance of 10 KΩ was connected to mid-supply (V_{DD}/2 = 0.9 V). The simulated variations of the input current with the output current are shown in Figure 5. The results shown in Figure 5 were obtained using a DC sweep of the input current from 0 – 20 µA at a step of 50 nA. Figure 6 shows the error between the ideal and the simulated characteristics of the proposed sawtooth current-mode folding amplifier. The spikes appearing in Figure 6 can be attributed to misalignment of transition points from the ideal values of 4,8,. . .,20 µA. Ignoring these misalignment of the switching points from

Table 1. Sizes of transistors used in simulation.

Current copier	
Cascode biasing transistor	0.5 µm/0.3 µm
MCA, MNA 1 µm /0.3 µm	1 µm /0.3 µm
Current scalar	
Cascode biasing transistor	0.5 µm/0.3 µm
MCA,MNA	0.8 µm/0.3 µm
MC1, MN1	1 µm/0.3 µm
MC2, MN2	2 µm/0.3 µm
Transmission gate	
MPG	0.5 µm/0.15 µm
MNG	0.32 µm/0.15 µm
Current comparator	
Inverter NMOS	1 µm/0.15 µm
PMOS inverter	3 µm/0.15 µm
CC 100fF	

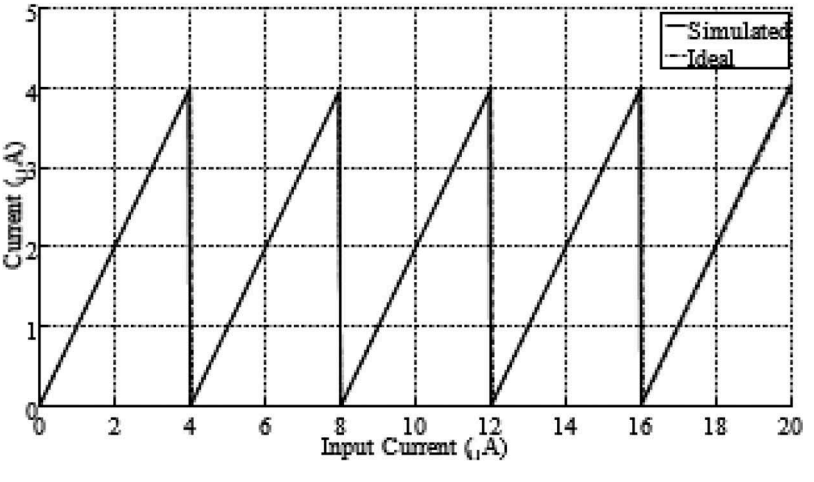

Figure 5. The input–output characteristic of the proposed folding amplifier.

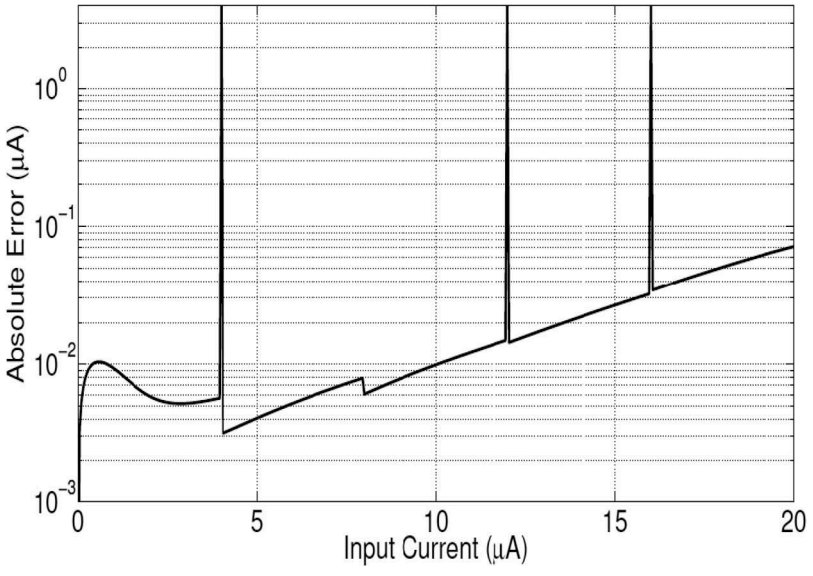

Figure 6. Absolute error between simulated and ideal characteristics of the proposed current-mode folding amplifier.

the ideal values, the maximum error shown in Figure 6 is less than 0.07 μA at an input current of 20 μA.

The response time of the 4-fold sawtooth current-mode folding amplifier was tested using a rising full-scale pulse signal (from 0 to 20 μA), shown in Figure 7(a), and a falling full-scale pulse signal (from 20 to 0 μA), shown in Figure 8(a). These two signals were applied to the input of the proposed current-mode folding amplifier. The output voltages of the comparators in the two cases are shown in Figure 7(b) and Figure 8(b), respectively. Inspection of Figures 7(a) and 8(a) shows that the rising pulse settled much slower than the falling one. Moreover, Figure 7(a) clearly shows the sudden jumps resulting from the switching-on of the mirrors. These correspond to the switching instances in Figure 7(b). Furthermore, Figure 7(a) shows that for the rising pulse the 2% settling time is 5.9 ns, while Figure 8(a) shows that the 2% settling time is 2.3 ns for the falling pulse. One can, therefore, conclude that using the full-scale delay there is a 4-fold improvement of speed over the performance of the sawtooth current-mode folding amplifier reported in Al Absi et al. (2014). It is worth mentioning here that the main current mirror took about 4 ns to settle after the last comparator, while all the comparators settled in at most 2 ns.

These results confirm that substantial improvement in the performance of the folding amplifier can be achieved by reducing the number of current mirrors in the path of the signal and by improving the current mirror design.

The performance of the 4-fold current-mode sawtooth folding amplifier was also tested under practical working conditions using a sinusoidal input signal current of frequency = 5 MHz. This signal was applied to the input of the folding amplifier and its output current was monitored. The results obtained from the transient response of the proposed current-mode folding amplifier are shown in Figure 9. These results

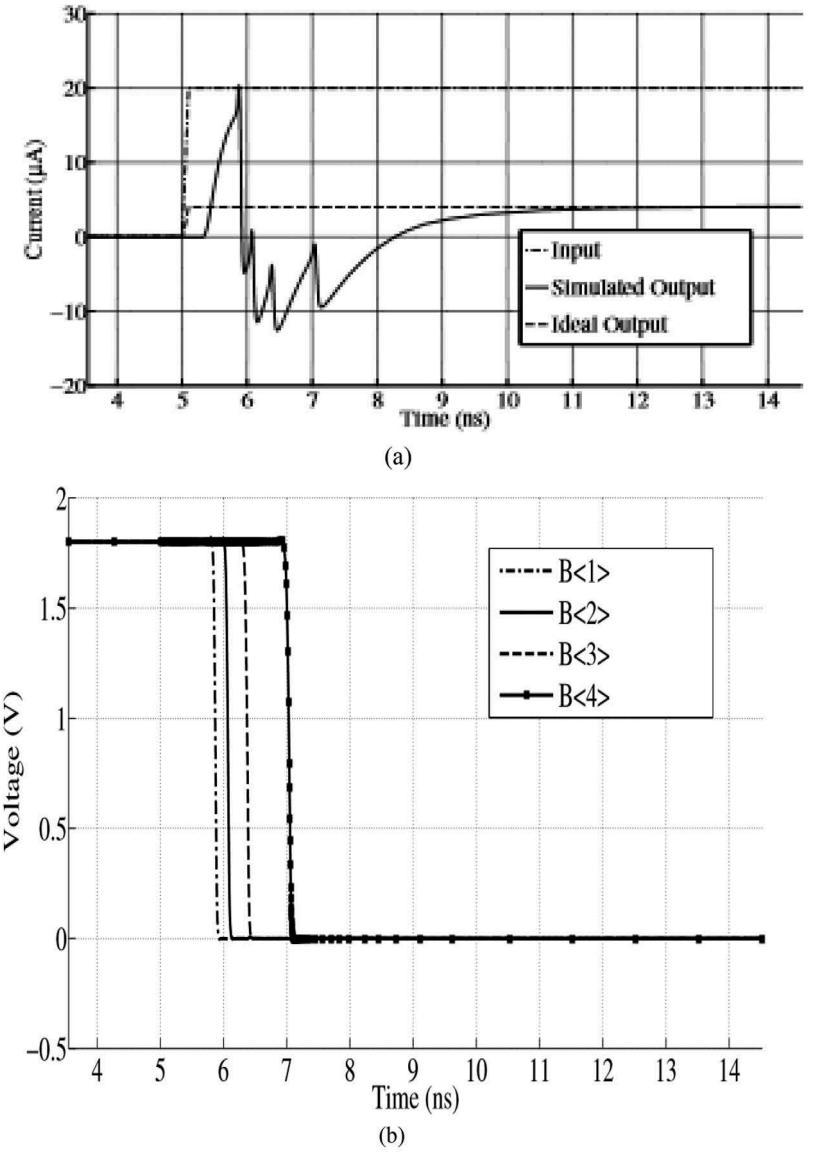

Figure 7. (a) Transient response of the proposed current-mode folding amplifier for a full-scale rising pulse and (b) comparator output for the rising pulse.

show that the switching events are almost following the ideal switch instances within the delays predicted by the pulse test. Moreover, the proposed circuit was also tested with a triangular input current and the output current was monitored. The transient response for the triangular input is shown in Figure 10. Inspection of Figure 10 shows that the proposed current-mode folding amplifier is functioning properly.

Furthermore, the number of folds of the folding amplifier was increased to 8 to provide an 8-fold amplifier. With $N = 8$, using the same fold size ($I_F = 4$ μA), the full-scale

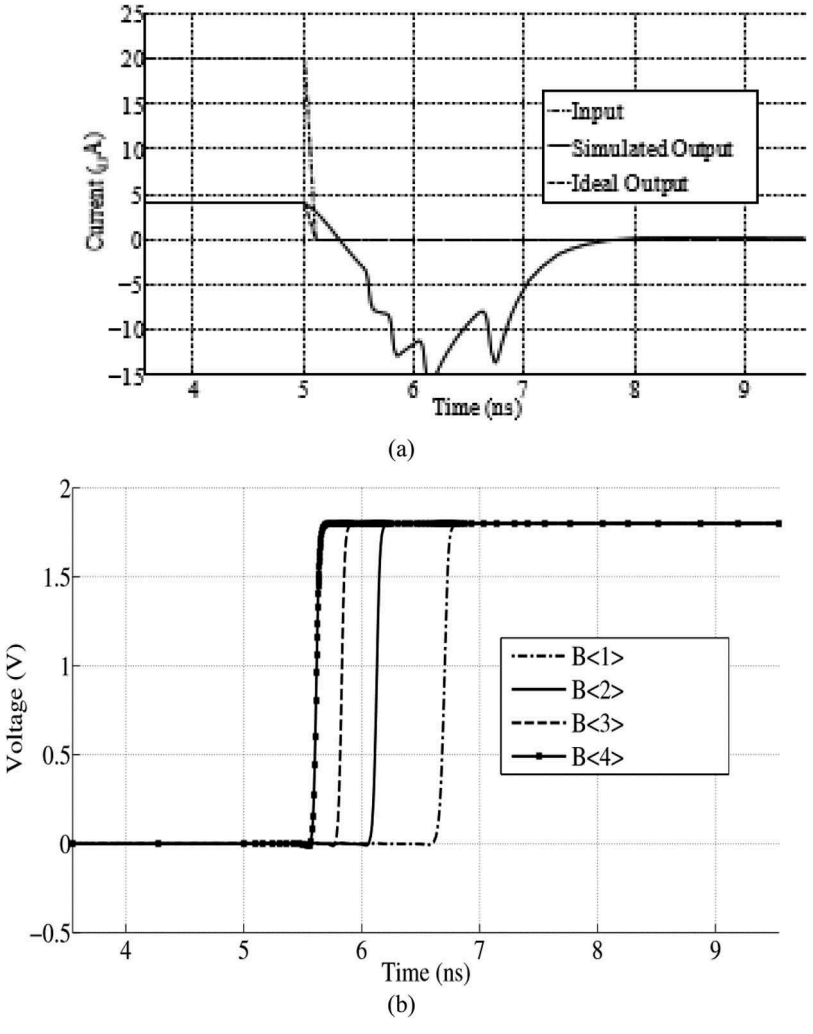

Figure 8. (a) Transient response of the current-mode folding amplifier for a full-scale falling pulse and (b) comparator output for the falling pulse.

value of the current is now 32 μA. The new developed 8-fold folding amplifier circuit was simulated using the same building blocks shown in Figure 4 and the settling times for the rising and falling pulses were monitored. As expected, increasing the number of output branches results in slower current mirrors and the settling time for the full-scale falling and rising pulses increased to 3.5 ns and 8.4 ns, respectively.

Finally, the effect of temperature variations on the performance of the proposed current-mode folding amplifier was tested. The circuit was simulated for temperature variations and the temperature was swept from −20°C to 125°C. Figure 11 shows a plot of the difference in the output current between the two extremes (125°C and −25°C). Inspection of Figure 11 clearly shows that the performance of the proposed current-mode folding amplifier is highly insensitive to temperature variations.

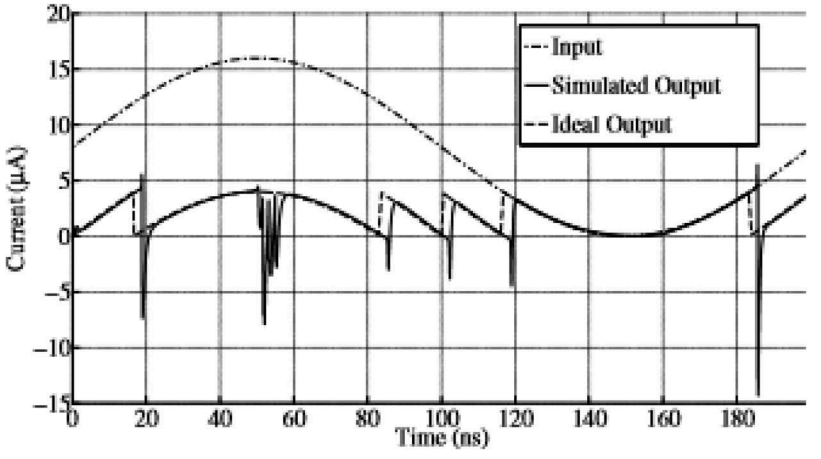

Figure 9. Response of the proposed current-mode folding amplifier to a sinusoidal signal of frequency 5 MHz.

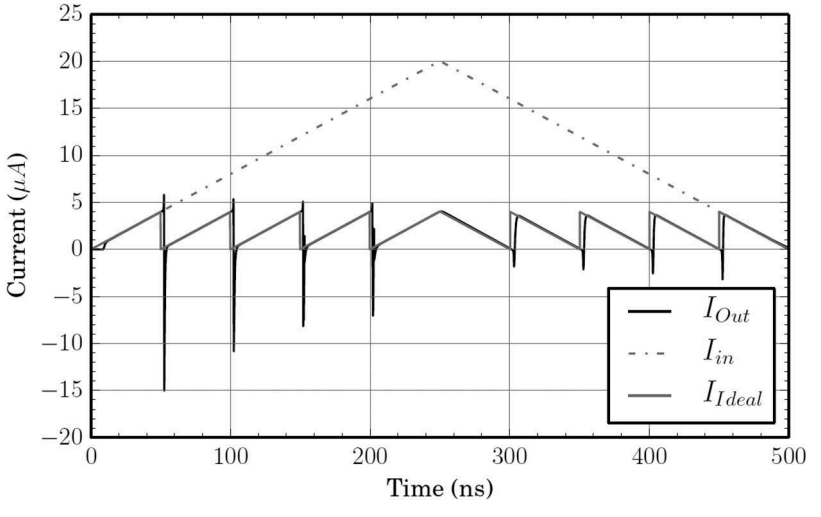

Figure 10. Transient response of the proposed current-mode folding amplifier to a triangular input signal.

Conclusion

In this paper, a new 8-fold current-mode folding amplifier with sawtooth transfer characteristics has been presented. The new design uses the minimum number of current mirrors with only one current mirror used in the path between the input and the output. Comparators were used to decide the switching points of the amplifier. The proposed current-mode folding amplifier was tested for a number of folds $N = 4$. Simulation results show that the proposed current-mode folding amplifier can provide a four times faster full-scale response. The functionality of the proposed circuit was also tested using sinusoidal and triangular input currents. In both cases the circuit proved to be functioning as expected. Moreover, the scalability of the proposed circuit was tested and a current-mode folding

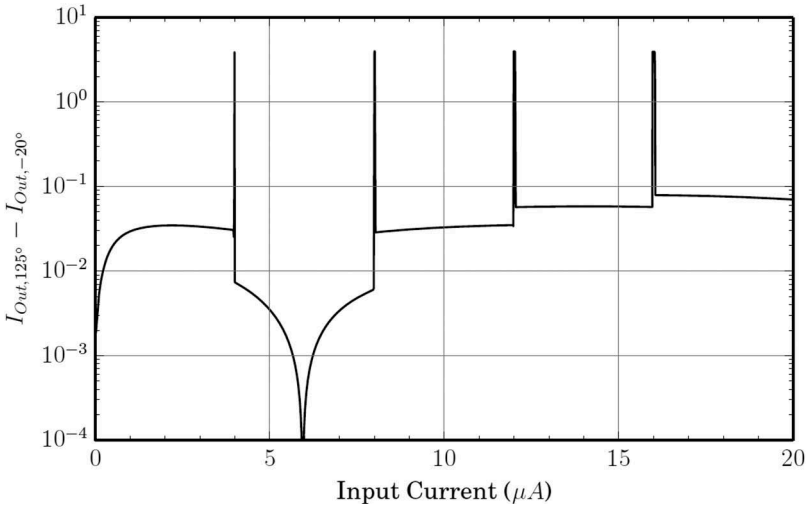

Figure 11. Plot of the difference in the output current due to the temperature variation.

amplifier with $N = 8$ was designed and tested using the same building blocks. The results show that the proposed circuit is scalable with a slight change in the full-scale time delay. This paves the way to develop current-mode folding amplifiers with number of folds $N > 8$ if a slight increase in the time delay can be tolerated. Simulation results also show that the performance of the proposed current-mode folding amplifier circuit is temperature insensitive over a wide range of temperature. Compared to previously published works, the proposed current-mode folding amplifier with sawtooth transfer characteristics would be a useful building block for small area on the chip and high-speed accurate ADCs. Finally, it is expected that substantial improvements in the performance of the proposed current-mode folding amplifier can be achieved by improving the settling time of the current mirror used.

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Disclosure statement

No potential conflict of interest was reported by the authors.

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