KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

ELECTRICAL ENGINEERING DEPARTMENT

EE-520 Project

Semester (131)

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Part I: Load-Flow Studies

The line-data and bus-data of the IEEE 30-bus system are given below on a 100 MVA base. The minimum and maximum limits of voltage magnitude and phase angle are considered to be 0.95p.u. to 1.05p.u. and -45^o to +45^o respectively.

Line Data of IEEE 30-Bus System (1/2)

Line number	From bus	To bus	Line impedance ($p.u.$)		Half line charging susceptance ($p.u.$)	MVA rating
			Resistance	Reactance		
1	1	2	0.02	0.06	0.03	130
2	1	3	0.05	0.20	0.02	130
3	2	4	0.06	0.18	0.02	65
4	2	5	0.05	0.02	0	130
5	2	6	0.06	0.18	0.02	65
6	3	4	0.01	0.04	0	130
7	4	6	0.01	0.04	0	90
8	4	12	0	0.23	0	65
9	5	7	0.05	0.12	0.01	70
10	6	7	0.03	0.08	0	130
11	6	8	0.01	0.09	0	32
12	6	9	0	0.21	0	65
13	6	10	0	0.56	0	32
14	6	28	0.07	0.06	0.01	32
15	8	28	0.06	0.20	0.02	32
16	9	11	0	0.21	0	65
17	9	10	0	0.11	0	65
18	10	20	0.09	0.21	0	32
19	10	17	0.03	0.09	0	32
20	10	21	0.03	0.08	0	32
21	10	22	0.07	0.15	0	32

Line Data of IEEE 30-Bus System (2/2)

Line number	From bus	To bus	Line impedance ($p.u.$)		Half line charging	*MVA*
			Resistance	Reactance	susceptance ($p.u.$)	rating
22	12	13	0	0.14	0	65
23	12	14	0.12	0.26	0	32
24	12	15	0.07	0.13	0	32
25	12	16	0.01	0.12	0	32
26	14	15	0.22	0.12	0	16
27	15	18	0.11	0.22	0	16
28	15	23	0.10	0.21	0	16
29	16	17	0.08	0.19	0	16
30	18	19	0.06	0.13	0	16
31	19	20	0.03	0.07	0	32
32	21	22	0.01	0.22	0	32
33	22	24	0.11	0.18	0	16
34	23	24	0.13	0.27	0	16
35	24	25	0.19	0.33	0	16
36	25	26	0.25	0.38	0	16
37	25	27	0.11	0.21	0	16
38	27	29	0.22	0.4	0	16
39	27	30	0.32	0.60	0	16
40	28	27	0	0.4	0	65
41	29	30	0.24	0.45	0	16

Transformer Tap Setting Data of IEEE 30-Bus System

From bus	To bus	Tap setting value ($p.u.$)
6	9	1.0155
6	10	0.9629
4	12	1.0129
28	27	0.9581

Bus Data of IEEE 30-Bus System (1/2)

Bus number	Bus voltage		Generation		Load		Reactive power limits	
	Magnitude ($p.u.$)	Phase angle (degree)	Real power (MW)	Reactive power ($MVAR$)	Real power (MW)	Reactive power ($MVAR$)	$Q_{\min}$ ($MVAR$)	$Q_{\max}$ ($MVAR$)
1	1	0	0	0	24.963	-4.638	-20	150
2	1	0	21.7	12.7	60.97	27.677	-20	60
3	1	0	2.4	1.2	0	0	0	0
4	1	0	7.6	1.6	0	0	0	0
5	1	0	0	0	0	0	0	0
6	1	0	0	0	0	0	0	0
7	1	0	22.8	10.9	0	0	0	0
8	1	0	30	30	0	0	0	0
9	1	0	0	0	0	0	0	0
10	1	0	5.919	2	0	0	0	0
11	1	0	0	0	0	0	0	0
12	1	0	11.2	7.5	0	0	0	0
13	1	0	0	0	37	13.949	-15	44.7
14	1	0	6.2	1.6	0	0	0	0
15	1	0	8.2	2.5	0	0	0	0
16	1	0	3.5	1.8	0	0	0	0
17	1	0	9	5.8	0	0	0	0
18	1	0	3.2	0.9	0	0	0	0
19	1	0	9.5	3.4	0	0	0	0

Bus Data of IEEE 30-Bus System (2/2)

Bus number	Bus voltage		Generation		Load		Reactive power limits	
	Magnitude ($p.u.$)	Phase angle (degree)	Real power (MW)	Reactive power ($MVAR$)	Real power (MW)	Reactive power ($MVAR$)	$Q_{\min}$ ($MVAR$)	$Q_{\max}$ ($MVAR$)
20	1	0	2.2	0.7	0	0	0	0
21	1	0	19.669	11.20	0	0	0	0
22	1	0	0	0	31.59	40.34	-15	62.5
23	1	0	3.2	1.6	22.2	8.13	-10	40
24	1	0	15	6.70	0	0	0	0
25	1	0	1.00	0.00	0	0	0	0
26	1	0	3.50	2.30	0	0	0	0
27	1	0	0	0	28.91	10.97	-15	48.7
28	1	0	0	0	0	0	0	0
29	1	0	3.659	0.90	0	0	0	0
30	1	0	12.00	1.90	0	0	0	0

Shunt Capacitor Data of IEEE 30-Bus System

Bus Number	**Suseptance (p.u.)**
10	20 + Your two-digit serial number
24	5 + 0.Your two-digit serial number

1. Use the Power World Simulation Package to simulate the above IEEE 30-bus power system indicating the following:
   - The single line diagram of the system including the circuit breaker at both ends of every line.
   - The voltage (p.u.), generation (MW and MVAR), and load (MW and MVAR) for each bus.
   - The line-flows (MW and MVAR) at both ends of every line.
   - The line-flow pie chart on every line.

2. Perform the following tasks:
   - Run your **own case** for a simulation time of 2 hours (7200 seconds) and simulation speedup of 60 seconds.
   - Use the load variation graph to simulate a varying load increase from 100% (using the base case) to 130% during the simulation time (**This must be automated increase in the load**).
   - Show the animated flows on the single-line diagram.
   - Enforce the line overloads to check the line limits.
   - Detect and record any system's abnormality during the simulation time (e.g., bus voltages outside 5% range of the nominal values, overloaded lines, …etc.).

3. Introduce a solution for the problems detected earlier to ensure a normal operation of the system during the simulation time (the two-hours).

4. Write a formal typed-report showing the following items:
   - The single-line diagram of the original case.
   - Statement on the problems faced during the simulation time.
   - The single-line diagram of the modified case (showing all modifications made to resolve the problems of the original case).
   - Statements on the suggested solutions with clear explanation and justification for each solution.

Submission Format:

Submit a hard-copy as well as a softcopy (on a cd). Label the softcopy with your student ID for all files in the following format:

- S200xxxxx0-o.pwd for the original file with extension pwd.
- S200xxxxx0-o.pwp for the original file with extension pwp.
- S200xxxxx0-m.pwd for the modified file with extension pwd.
- S200xxxxx0-m.pwp for the modified file with extension pwp.
- S200xxxxx0.doc for the report file with extension doc.

Control Options:

You may use one of the following control options:

- Increase the number of circuit of lines (maximum one circuit).
- Add a new line (maximum two circuits).
- Add a new Generator to one of the existing busses (one generator of 100MW and 40MVAR).
- Add Capacitor banks (maximum at two locations; each with 40MVAR).
- Use Transformer taps (maximum +/- 25% of the nominal value).

Part II: Short-Circuit Studies

Consider the IEEE 30-bus system given in Part I of this project. Assume that each generator has a subtransient reactance of 12% on the 100MVA base. Conduct short circuit analysis before and after modifying your system for the following:

- Calculate the subtransient fault current seen by each circuit breaker due to a solid three-phase fault occur at all bus locations.
- Calculate the subtransient fault current seen by each circuit breaker due to a three-phase fault through an impedance of (0.1+ 0.your two digit serial number) occur at all bus locations.
- Calculate the subtransient fault current seen by each circuit breaker due to a solid SLG fault occur at all bus locations.
- Calculate the subtransient fault current seen by each circuit breaker due to a SLG fault through an impedance of (0.1+ 0.your two digit serial number) occur at all bus locations.
- Find out the proper capacity (in MVA) needed of each circuit breaker in these busses.

Due date: December 9th 2013

Good Luck in your project