Design and Analysis of Fractional-N Frequency Synthesizers For Wireless Communications

by

Alaa Hussein

A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Doctor of Philosophy
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2002

I hereby declare that I am the sole author of this thesis.

I authorize the University of Waterloo to lend this thesis to other institutions or individuals for the purpose of scholarly research.

Alaa Hussein

I further authorize the University of Waterloo to reproduce this thesis by photocopying or other means, in total or in part, at the request of other institutions or individuals for the purpose of scholarly research.

Alaa Hussein

The University of Waterloo requires the signatures of all persons using or photocopying this thesis. Please sign below, and give address and date.

Acknowledgements

After thanking God Almighty for giving me the strength and ability to complete this work, I would like to express my sincere thanks to my parents who have instilled in me the drive and encouragement to complete this work.

I would also like to express my appreciation and gratitude to my thesis supervisor, Professor M. I. Elmasry for his encouragement, guidance and support in my research. He gave me valuable insight and motivation for this work.

I would also like to acknowledge and thank all my colleagues in the VLSI Research Group, and my co-workers in Texas Instruments, and Research in Motion for their support and useful discussion.

This work is supported in part by research funding from NSERC, Canadian Microelectronics Corporation (CMC) and Micronet. Their contributions are greatly appreciated.

Abstract

Over the last few years, the wireless market has experienced an exponential growth. To sustain this growth, along with the increasing demands of new wireless standards, the cost, battery-lifetime, and performance of wireless devices must be enhanced.

With the advancement of radio frequency (RF) technology and the requirement for more integration, new RF wireless architectures are needed. One of the most critical blocks in a wireless transceiver is the frequency synthesizer. It significantly affects all three dimensions of a wireless transceiver design: cost, battery-lifetime, and performance. In this thesis, we present new RF synthesizer architectures with low-power consumption, high-performance, and low cost.

The common approach to frequency synthesis design for wireless communication is to design an analog-compensated fractional-N phase-locked loop (PLL). However, this technique suffers from lock time limitations, and inadequate fractional spur suppression, and falls short of third generation wireless standards. In this work, we propose three new delta-sigma PLL architectures to overcome the disadvantages of traditional PLLs. The first architecture addresses the spur reduction through the use of the sigma-delta modulator output as a dithering signal. The second architecture targets the speed and stability issue, as well as the power dissipation, by replacing the sigma-delta block with a pre-calculated ROM. The last architecture reduces both the power dissipation and the spur level through the implementation of a proposed tapering technique. The use of these architectures for closed-loop modulation is also examined.

The major advantages of these architectures include low-cost, low-power, and a fully monolithic solution. Throughout this work, low-power has been achieved by different architectural techniques that enable a tighter integration of the PLL's loop components on a single chip, as well as a faster lock time.

Another pivotal block in wireless transceiver is the data converter. Data converters provide the two required bridges between the analog and digital worlds; as a result, data converters pose interesting and challenging tradeoffs that are relative to integration, process technology, and performance parameters.

Another goal of this thesis is to find methods for improving the performance (such as reducing power and energy consumption) of the analog-to-digital converter for wireless applications. A new analog-to-digital converter (ADC) architecture is devised. This architecture is memory-based: the last sample is used to predict the current one, resulting in both low-power dissipation and energy reduction. The low-power dissipation is a vital factor when we consider the chip reliability and integrity. The low-energy consumption is a critical factor when we consider battery operated devices. Moreover, the proposed memory-based ADC may be used to extend the attainable flash converter resolution by pre-calculating the most significant bits.

Contents

List of Tables

List of Figures

List of Abbreviations

CMOS	Complementary Metal Oxide Semiconductor
ECL	Emitter Coupled Logic
IC	Integrated Circuit
CDMA	Code Division Multiple Access
TDMA	Time Division Multiple Access
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
DSM	Delta-Sigma Modulator
PLL	Phase-Locked Loop
OSR	Over Sampling Ratio
SNR	Signal to Noise Ratio
MASH	MultistAge noise SHaping
MLS	Minimum Length Sequence
PN	Pseudo Noise
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
FN	Fractional-N
LSB	Least Significant Bit
MSB	Most Significant Bit

Chapter 1

Introduction

1.1 Introduction

In the last decade, there has been an explosive growth in the wireless telecommunications market. Approximately $750 billion will have been spent in the rollout of third generation (3G) mobile networks with the highest levels of investment in the US, Japan, and western Europe. Worldwide revenue projections for all 3G services will mushroom from zero in 2001 to approximately $67.7 billion by 2005.

It is estimated that more that half of the homes in the United States now have cordless phones, and that approximately 20,000 Americans join the cellular phone market everyday. Now, more than 280 million people currently subscribe to cellular phones, whereas ten years ago, there were only 2 million subscribers. Revenues from all wireless voice and data services in the U.S. are expected to grow to $119 billion by 2005. Approximately, 30% of the computer market revenue comes from portable computers (laptops and notebooks) that require wireless access. Furthermore, with dedicated email wireless terminals now on the market, there will be 136 million of these devices on the networks.

The fantasy that anyone can communicate with anyone else anytime, anywhere and exchange any kind of information will soon be a reality. Today, voice, data, and video can be transmitted over a wireless channel from one portable unit to another. The key to the success of the wireless market is affordability due to advances in semiconductor technology. As transistor dimensions shrink in size, more components are moved from the board to the chip. This not only helps to

drastically reduce cost and area, but also to remove power consuming chip-to-chip communications. The present goal is to reduce both power consumption and the price of cellular phones by 30% each year. This cannot be achieved by relying on semiconductor technology alone. Circuit and architectural techniques must be investigated.

One pivotal block in the wireless radio terminal is the frequency synthesizer, which is responsible for generating the carrier frequencies for both the transmitter and receiver. A wireless radio may have a shared frequency synthesizer for both the transmitter and the receiver, or two dedicated frequency synthesizers. The performance of the frequency synthesizer directly affects the performance of the transceiver.

The amount of time required for the synthesizer to generate a certain frequency (called lock time) also affects performance and power consumption. In many wireless standards, time division multiple access (TDMA) is used, where each user is given a time slice to transmit his data. After this time slice is passed, the frequency synthesizer of the base station must tune to the transmission frequency of another user. If the frequency synthesizer lock time is reduced, the bandwidth allocated to each user can be increased. The frequency synthesizer is also the most active component in the wireless radio. Since the radio must periodically check for any incoming data, the synthesizer must be turned on for that amount of time. Moreover, power is wasted because the transceiver must be on while the synthesizer is locking to the desired channel.

Integrating the entire frequency synthesizer on a single chip is a challenging task. This is related to the stringent performance requirements of the synthesizer. The quality of the on-chip passive components used in the frequency synthesizer is usually much lower than that of discrete components. Also, interference between one of the frequency synthesizer's components on another may cause performance degradation. This leads to the need for more board space, which entails a higher cost, larger size, and more power dissipation.

One approach to integrate the entire frequency synthesizer on a single chip is to use a specialized technology, which is expensive and has not received widespread acceptance by the industry. An alternative solution is to use an inexpensive technology such as CMOS and try to achieve integration through architectural innovations. This technique requires the redesign of the frequency synthesizer architecture.

Frequency synthesizers for wireless communications are usually implemented as phase locked

loops (PLLs), which have both analog and digital components. In this study, we examine digital solutions for improving the performance, integration, power consumption, and lock time of PLLs.

1.2 Organization of the Thesis

Chapter 2 is an introduction to different transmitter architectures. The delta-sigma modulation technique and the concept of noise shaping are presented in Chapter 3. Noise shaping capabilities are also useful in frequency synthesis and modulation of the signal in the fractional-N frequency synthesizers, which are discussed in Chapter 4.

In Chapter 5, we implement a modified multistage noise shaping (MASH) frequency synthesizer. The MASH architecture is realized by cascading first and second order delta-sigma modulators. This architecture is known to provide a digital solution to eliminate the spurious noise produced by PLLs. Also, the MASH architecture offers a high frequency resolution which is essential for all second and third generation wireless communication standards. The modification was introduced to increase the flexibility of the MASH architecture.

To improve the performance of the MASH architecture, a novel architectures based on delta-sigma modulation are presented in Chapter 6 . It is demonstrated that these architectures are capable of better performance in terms of spur, speed, stability, and power dissipation compared to the architecture introduced in Chapter 5.

In Chapter 7, a new low-power memory-based analog-to-digital converter architecture is given. Finally, a discussion, conclusion, and future work proposal are presented in Chapter 8.

Chapter 2

Wireless Transmitters

2.1 Introduction

In today's mobile communication applications, cordless or wireless, researchers are focused on a one-chip solution within a single technology.

New architectures and new techniques such as delta-sigma modulation are being investigated for the transceiver at both the circuit level and system level to reduce cost and power consumption. The transceiver or RF-front end is composed of a receiver and a transmitter.

Several receiver architectures with delta-sigma modulation [4] have been described in several papers, for example, [5] and [6]. The tendency has been to move the digital stage close to the antenna either with a superheterodyne (two down-conversion stages) structure or a low-IF structure or a zero-IF structure. The separation between the in phase (I) and the quadrature phase (Q) of the complex signal is carried out in the digital domain after a baseband or low frequency analog to digital conversion. The conversion is performed with a bandpass delta-sigma analog to digital converter.

Regarding the transmitter component, little work has been published on architectures with delta-sigma modulation. In this work, we have chosen to concentrate on the modulator/frequency synthesizer block, and the issues related to delta-sigma modulation in the transmitter design.

In the existing transmitter designs, frequency up-conversion is either performed directly or with a single mixer stage to produce a single-sideband signal [7]. As we will discuss in Section 2.2, both structures are not ideal if we want to change the technology, or meet several standards within

a single implementation. Therefore, we will consider architectures with delta-sigma modulation in the two transmitter structures.

2.2 Transmitter Architectures

2.2.1 Heterodyne Architecture

In a heterodyne transmitter, the information signal is transmitted from baseband to radio frequency by one or two up-conversion stages, known as frequency mixers, as shown in Figure 2.1. The principle of frequency up-conversion is as follows: The input signal is multiplied by a local oscillator (LO). The output of the multiplier is band-pass filtered to conserve only one of the two resulting frequency components of the signal. For example, if we consider a baseband sinusoid f_1 multiplied by a sinusoid of frequency $f_2 > f_1$, the result of the product of these two input signals contains the frequency $f_2 - f_1$ and $f_1 + f_2$. When filtering the frequency component $f_2 - f_1$, we obtain a signal with a frequency component greater than f_2.

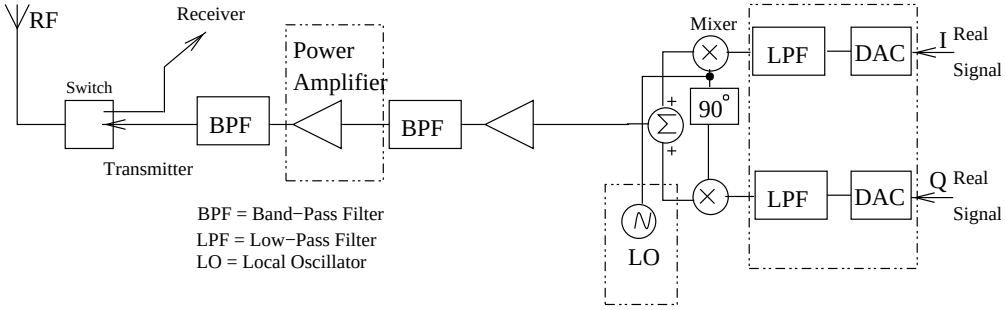


Figure 2.1: Mixer-based up-conversion transmitter

Frequency up-conversions that are based on mixers present several disadvantages. Often, the frequency components of the local oscillator are composed of not only a central frequency f_c, but also harmonics ($\pm nf_c$). Also, the mixer is a non-linear device which produces frequency components of $\pm mf_1 \pm nf_2$.

Due to the complex nature of the modulated signal, the I and Q channels, the two signals must be processed in an orthogonal manner; therefore, a precise 90° phase shifter is needed to generate the two components of the complex signal from the local oscillator.

The reliability of the implementation with one mixer depends on the high requirements of the

filter after the mixer, and the accuracy of the 90° phase shifter.

2.2.1.1 A Digital Quadrature Modulator in a Mixed-Signal Superheterodyne Transmitter

A digital quadrature modulator, illustrated in Figure 2.2, has been presented in [8]. The modulator is implemented in a $1\mu m$ CMOS process. The digital quadrature modulator is clocked at 80MHz for a carrier frequency of 20MHz for each of the modulator inputs.

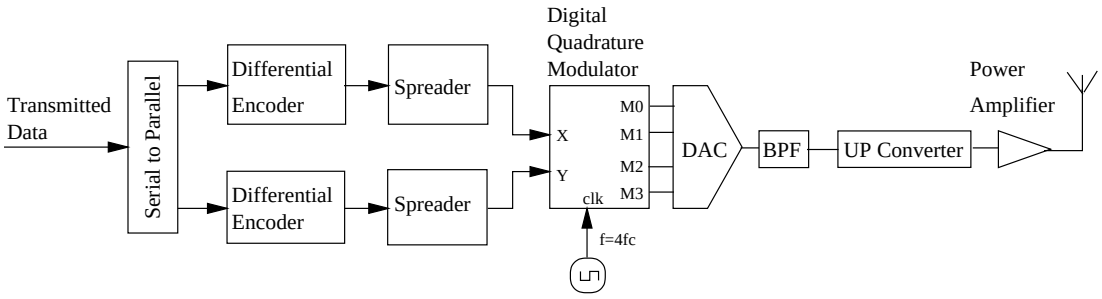


Figure 2.2: Quadrature modulator in a spread-spectrum transmitter

Such an architecture is based on two mixing stages; the first stage is fully digital, whereas the second stage remains analog.

In the first up-conversion stage, the transmitted data is separated in the I and Q channels. After some modifications (differential encoding and spreading with a pseudo-noise (PN) generator), the I and Q channels are fed into a digital quadrature modulator. The 4-bit output of the modulator is converted to an analog signal with a digital-to-analog converter (DAC). Then, the output is moved to higher frequency through a second up-conversion stage as in a classic heterodyne modulator. This structure eliminates the need for a precise analog-phase shifter and analog mixers for the first up-conversion stage. In addition, precise filtering is required for the analog up-conversion stage, which may limit the full integration of the transmitter with a single technology such as CMOS.

Even though a digital stage may alleviate the problem of phase accuracy required in the 90° phase shifter, a heterodyne-based transmitter generally requires sharp filtering to reject the non-linear components introduced by the frequency mixers. Sharp filters are difficult to integrate on CMOS, because only low quality factors for inductors and capacitors are available.

2.2.2 Direct Conversion with a PLL

An alternative implementation of the transmitter is based on a direct up-conversion from the baseband to RF. The loop of a phase-locked loop (PLL) is opened to introduce digital modulation. PLL parameters are calculated to cover the range of the frequency carriers required for each channel of the frequency bandwidth allocated to a given mobile communication standard. The direct-modulation scheme based on an integer-N PLL suffers from a large settling time, which is problematic for second and third generation wireless communication standards.

DECT or GSM specifications imply a high division ratio and a low reference frequency, if the division ratio N in the PLL feedback is chosen to be an integer. This results in a large settling time, but such a type of PLL does not require delta-sigma modulation.

To obtain a fast settling time, we can use a fractional-N PLL and introduce the information by other means into the loop, which will be discussed in the next section.

2.2.3 Architectures Using $\Delta\Sigma$ Modulation

Both heterodyne and direct conversion-based transmitters may limit the integration capabilities of the transmitter. Therefore, we have decided to investigate the benefits of a specific technique in the transmitter, known as delta-sigma modulation. The principle of delta-sigma modulation and related matters such as stability, and scaling factors are further developed in Chapter 3.

Several transmitter architectures can benefit from delta-sigma modulation, and we will consider the direct conversion with the PLL. In this case, the information is directly brought to the RF band with a fractional-N frequency divider. More work in fractional-N frequency synthesizers will be discussed and developed during this research work.

2.2.3.1 Direct Conversion with a PLL Using $\Delta\Sigma$ Modulation

Fractional-N frequency synthesizers have several advantages over integer division ratio architectures [9]. These advantages include improved phase noise and fast settling time without sacrificing frequency precision.

Figure 2.3 depicts a basic frequency synthesizer structure. In a frequency synthesizer such as the PLL, the frequency division ratio N determines the signal integrity. The phase noise of

the reference and the phase detector are degraded by $20.log(N)$. The output frequency, f_o of the PLL, is a multiple of the reference frequency f_R, as shown in

$$f_o = N.f_R \tag{2.1}$$

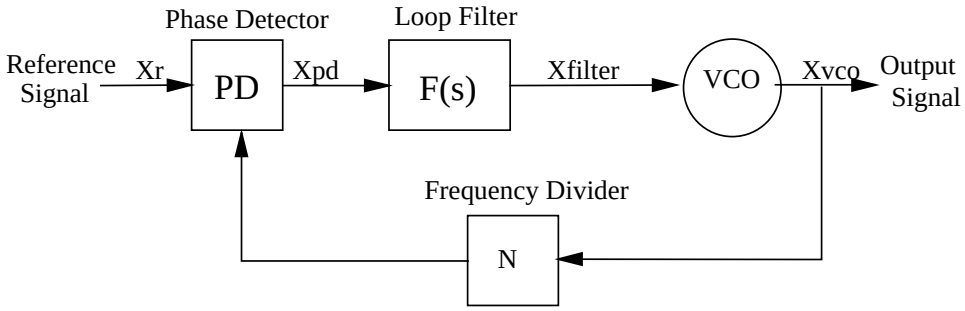


Figure 2.3: Basic frequency synthesizer

In fractional-N synthesis, the division ratio N of the frequency divider is not an integer. The fractional value is controlled by a delta-sigma modulator. The reference frequency f_R, is many times the frequency step time f_{step}, and the output frequency of the PLL, f_o is

$$f_o = f_R\Big(N + \frac{K}{F}\Big) \tag{2.2}$$

where K corresponds to the input word and $F = 2^n$ for an n-bit accumulator used as a delta-sigma modulator. The phase noise is theoretically improved by $20log(F)$ compared to the integer case. In practice though, improvement is limited by the narrow filtering, and the method of fractional-N synthesis does not work for frequency steps as low as 1kHz [9].

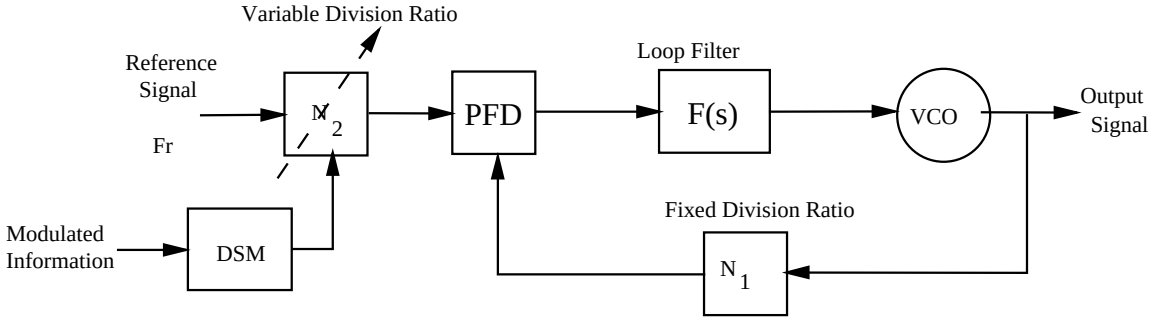
The fractional frequency division ratio is obtained with the help of a delta-sigma modulator, which controls the division ratio of a dual-modulus divider or a multi-modulus divider. A low-order delta-sigma modulator produces idle tones when a DC input signal is applied. However, as the order of the DSM increases, the idle tones disappear as the quantization noise becomes white. The output of the modulator contains both the average value of the division ratio and a high frequency component that is noise shaped. Noise shaping moves the quantization noise, due to the switching event, to a high frequency where it is shaped by the low-pass characteristic from the PLL. More details about noise shaping in DSM will be given in Chapter 3.

The FN frequency synthesizer may be modified so that there is a direct conversion of the baseband information to a high frequency as will be discussed in the next section.

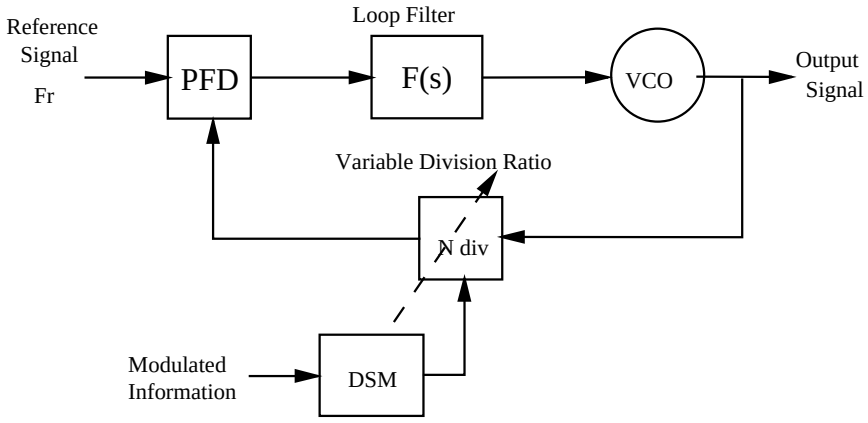
2.2.3.2 Information Modulation

There are several ways to introduce information into the loop, and to control the fractional value of the division ratio with a delta-sigma modulator in the fractional-N PLL.

Our goal is to obtain an output frequency given by $f_o = \frac{N_1}{N_2} f_R = N_{div}.f_R$, which corresponds to an average division ratio of $N_{div} = \frac{N_1}{N_2}$. The delta-sigma modulator (DSM) minimizes the noise introduced by the switching event in the fractional-N frequency synthesizer. Also, the DSM controls the value of the fractional division ratio. The modulation of the DSM input introduces a modulation into the loop without the need for opening the loop.



(a) Introduction of the information through the frequency reference



(b) Introduction of the information through the frequency divider

Figure 2.4: Introduction of the modulated information in the FN frequency synthesizer

In Figure 2.4, the VCO output frequency is given by $f_o = \frac{N_1}{N_2}.f_R = N_{div}.f_R$. One of the noise contributions from the frequency reference to the output $S_{\Theta_o|_R} = (N_{var})^2.S_{\Theta_R}$ is unchanged by an implementation with a single variable division ratio (Figure 2.4 (b)), or by two separated division ratios (Figure 2.4 (a)).

However, the noise produced by the dividers is multiplied by only the frequency division ratio placed in the feedback of the loop after the VCO. Therefore, the phase noise contribution from the dividers, and also from the DSM, is multiplied by N_1^2 (Figure 2.4 (a)); the phase noise contribution is multiplied by N_{div}^2 (Figure 2.4(b)). $N_{div} < N_1$, and the implementation of the fractional-N frequency synthesizer, shown in Figure 2.4 (b), is preferred to the implementation in Figure 2.4 (a) based on [10]. We conclude that the introduction of the modulation through the frequency divider after the VCO in Figure 2.4 (b) is preferred to the introduction of the modulation through the frequency reference N_2 in Figure 2.4 (a).

2.2.3.3 Wide Band Information and the Low Pass Characteristic of the PLL

The phase-locked loop has a low-pass characteristic in order to control the VCO with a low frequency signal with as few harmonics as possible. Unfortunately, if the bandwidth of the information that is transmitted is higher than the loop bandwidth, information is also low-pass filtered.

The loop-compensation with an equalizer and the dual point modulation of the PLL are two techniques to prevent such filtering. In the loop compensation, the information is pre-filtered by an equalizer, which amplifies the signal to compensate for the low-pass characteristic of the PLL. The precision of such a method is limited due to the imprecision of the model used to estimate the transfer functions of analog components such as the analog filter.

In the alternative method, the information is introduced at two points in the loop, before and after the filter, which is discussed in Chapter 4. This method also presents some shortcomings in the case of an analog implementation, because of the limited precision of the analog integrator.

2.2.3.4 State-of-the Art Fractional-N Frequency Synthesizers Based on Delta-Sigma Modulation

In this section, we are interested in the implementation of fractional-N synthesizers based on high-order delta-sigma modulation, these synthesizers were first introduced by Miller [11]. There are several types of architecture, and in the first designs, the bandwidth of the information is not a concern and no compensation method is presented.

GFSK Modulation Using a PLL

Miller's original design [11] was modified by Riley and Copeland [12] to add information to the loop through the DSM input [13] after Gaussian filtering. The Gaussian filter is placed before the DSM input, and insures a GMSK modulation scheme at the output of the VCO. However, this design is not sufficient if we want to modulate the PLL with wide bandwidth information such as in GSM or DECT.

A Delta-Sigma Frequency Discriminator-Based Synthesizer Architecture

Riley and Copeland [5] presented another design, which was also based on delta-sigma modulation, but in a different manner, as shown in Figure 2.5. In their architecture, delta-sigma modulation is introduced in the frequency divider block, the so-called frequency discriminator. An oversampled frequency discriminator converts the frequency information to an oversampled bit-stream, and the conversion is followed by several digital blocks which down-sample the signal and perform the low-pass filtering in the loop. The number of analog components is reduced, and the discriminator shapes the quantization noise in the digital-to-analog conversion. Most of the quantization noise is pushed outside the loop bandwidth, and the high frequency spectral components are filtered. To avoid time-aliasing in the PLL, the input information frequency f_{in} is chosen so that it is smaller than half of the sampling frequency, and the output frequency of the VCO is assumed to remain in the range $[N.f_R, (N+1).f_R]$.

The frequency discriminator in [5] is difficult to use in a frequency synthesizer for a mobile communication system. In the transmitter of a mobile phone, the frequency synthesizer should generate several channel central frequencies with a fine precision. In addition, we must control the synthesizer to select a given channel, which seems difficult in the structure presented in [5]. The frequency discriminator is identified as a delta-sigma modulator, but issues such as stability and input scaling of the identified modulator are not mentioned in [5].

Finally, the decimation filter may contribute to the added phase noise of the PLL which is difficult to filter out with only a first-order loop filter.

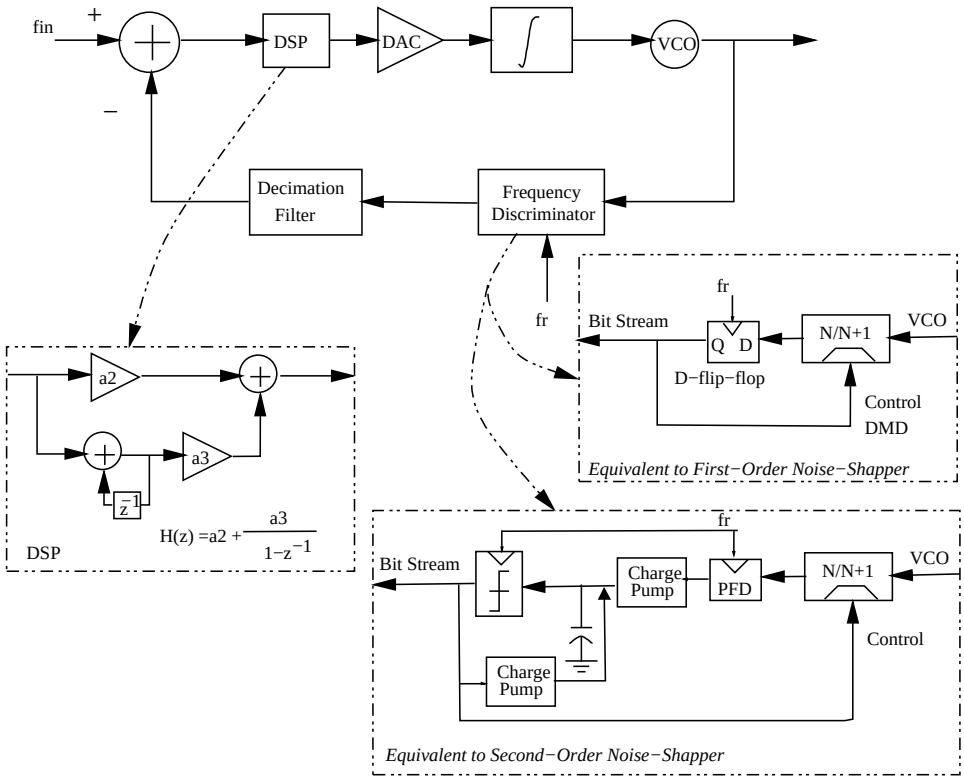


Figure 2.5: A delta-sigma frequency discriminator-based synthesizer architecture

Moreover, the implementation of a digital loop in [5]is not convenient for a frequency synthesizer in a mobile communication system, because we can not control the channel selection. The DSM in the frequency discriminator is partly analog which also increases the inaccuracy.

Fractional-N Synthesizers For DECT

In 1997, Perrott presented a low-power consumption CMOS fractional-N synthesizer which reaches the DECT frequency range [14], but does not cover the full DECT range. The information is introduced through the divider, but a gain control scheme and equalizer are placed in the loop to compensate for the low-pass characteristic of the loop in the wide band information.

The multi-modulus divider in Perrott design is based on a modified version of the high speed dual modulus divider from Steyaert and Craninckx [15]. Pipelining in the DSM is required to avoid a timing problem, when the frequency reference is in the range of 10-20MHz.

Fractional-N Synthesizers for ISM

A fractional-N synthesizer with an integrated compensation filter and Gaussian filter was presented by Filiol [16] who combined the ideas presented by Perrott [14] and Riley, Bax, and Copeland [12]. The modulation is introduced into the loop after filtering through four first-order DSMs in cascade, a structure, known as MASH [17]. It is based on Miller's original idea [11]. The frequency channel, controlled by a 3-bit serial interface, is added between the filter output and the DSM input. The coefficients of the filter are delta-sigma encoded to reduce the power consumption. However, this results in a reduced resolution. Dithering on the least significant bit (LSB) is required to insure the suppression of idle tones.

The target application is ISM, and good spurious performance, low phase noise, and fast settling time are obtained. The synthesizer is integrated in two chips with a CMOS modulator chip, and a bipolar high speed divider and phase detector.

Fractional-N Synthesizer for GSM

The type of Fractional-N PLL mentioned above has been modified to comply with the GSM specifications in [18]. In order to simplify the design of the equalizer, the frequency divider and the phase frequency detector are replaced by a delta-sigma discriminator and the loop filter is also digital. With mostly digital loop elements, we may compensate for the narrow loop bandwidth effect on the modulated signal in a precise manner. However, due to the uncertainty on the loop gain, some pre-tuning may be required as a 20% gain error has a strong influence on the modulation as visualized with the eye pattern in [18].

Finally, is a DSM based on a first-order stage a judicious choice though easy to implement, as a first-order DSM is known to present ideal tones for DC inputs ?. Spurious frequencies generated by fractionality can be improved with a higher order delta-sigma modulator obtained by cascading stable first-order and second-order modulators. Most designs use a third-order delta-sigma modulator based on the implementation that Miller [11] suggested.

In most of the modified versions of the original design from B. Miller [11], the main idea is to adapt the initial design to a given application, particularly to a mobile communication standard such as DECT [14], ISM [16], GSM [18]. A summary of the frequency synthesizer requirements in wireless communications will be given in Section 2.2.4.

Too often though, the fundamentals of fractional-N frequency synthesis are not fully explained.

There is no detailed methodology to design a fractional-N frequency synthesizer based on delta-sigma modulation, with respect to a given mobile communication standard. More details about fractional-N frequency synthesis will be given in Chapter 4.

In a PLL, several blocks contribute to the phase noise: the divider, the phase detector, the charge pump, and the digital-to-analog converter. We know that delta-sigma modulation will mitigate the noise somewhat. However, we need to understand how each noise source contributes to the overall noise in the PLL. More details about different phase noise contributors in the PLL will be given in Chapter 4.

2.2.4 Frequency Synthesizer Requirements in Wireless Communications

Table 2.1 summarizes some of the second generation wireless communications standards that are currently used [1].

	IS-95	IS-54/ IS-136	GSM	GPRS	DCS-1800	CT-2	DECT
F(MHz) (Rx/Tx)	869-894 824-849	869-894 824-849	925-960 880-915	925-960 880-915	1805-1880 1710-1785	864/868	1880-1900
Access Method	CDMA/ FDM	TDMA/ FDM	TDMA/ FDM	Packet	TDMA/ FDM	TDMA/ FDM	TDMA/ FDM
Duplex Method	FDD	FDD	FDD	FDD	FDD	TDD	TDD
# chan.	798	832	124	374	1600	40	10
Chan. Spacing (kHz)	1250	30	200	200	200	100	1728
Modulation	QPSK/ OQPSK	$\pi/4$ DQPSK	GMSK	GMSK	GMSK	GFSK	GFSK
Switching Time (μs)	Slow	Slow	577	200	577	1000	30:BS 450:HS
Freq. Accuracy		200Hz (0.2ppm)	50Hz (0.1ppm)	50Hz (0.1ppm)	100Hz (0.1ppm)	10KHz (10ppm)	50KHz (25ppm)

Table 2.1: Summary of 2G wireless communications standards [1]

As we can see from Table 2.1, all frequency standards demand switching speeds less than 1 ms, and frequency accuracies less than 25ppm. We should note that all the cellular standards require a frequency accuracy less than 0.2ppm. Also, we should note that the GSM (Global System

for Mobile Communications) standard is the most widely used digital standard worldwide, and it demands the most from frequency synthesizers. Both the frequency accuracy and switching speed of GSM are very aggressive.

In an effort to extend the use of wireless transmission from merely voice, new third generation standards are emerging. The objective of third generation wireless standards can be summarized as follows:

- Full coverage and mobility for 144kbps, preferable 384kbps;
- Limited coverage and mobility for 2Mbps;
- High spectrum efficiency compared to existing systems;
- High flexibility to introduce new services.

The bit rates of 384kbps and 2Mbps were set in order to meet the current video transmission standards of H.263 [19] and MPEG-2 [20], respectively. There are two third generation standards that have emerged. One is called wideband CDMA (WCDMA) [21]. The WCDMA standard has been widely accepted in Europe, Japan, and North America. This standard was made backward compatible with the GSM standard. Another version of WCDMA, called CDMA2000 [22], was created to be backward compatible with the IS-95 standard.

Wideband CDMA has a nominal bandwidth of 5MHz, so that it can incorporate data rates of 144kbps, 384kbps, and 2Mbps. In order to be compatible with GSM, different grades of data transmission have been created. The lowest grade is a 200kHz channel (which is the same as the GSM); higher data rates can be achieved by combining several GSM channels.

Current TDMA-based technologies [23], GSM, IS-136, and IS-54 use a single voice channel for data per user, which delivers data at a rate of 9.6Kbps and 14.4Kbps. Today, new standards enabling high-speed wireless data transmission are emerging. These standards, which exhibit some features of third generation standards, are extensions of current second generation standards. Such standards are referred to as 2.5 generation or 2+ generation standards. The two most popular are the GPRS [24] (general-packet-radio service) and HSCSD [24] (high-speed circuit switched data) standards. HSCSD is a circuit switched data transmission that can offer as much as 76.8Kbps. This is done by dedicating more than one channel to a user. Circuit switched data

transmission entails that a dedicated connection must be established, and this connection cannot be broken until all the transmission is complete. In contrast, GPRS is a packet switched data transmission that can offer data rates over 100kbps. In packet switched transmission, a physical connection exists only during the transmission burst. Not only does this mean that the channel is used more efficiently, but it also means that in GPRS, users can be "virtually" connected for hours at a time and only incur connection charges during transmission bursts. GPRS is expected to be the main enabling technology for high-speed wireless internet access in the near future.

As shown in Table 2.1, GPRS requires fast switching from one channel to another, because GPRS uses a combination of TDMA and FDMA. In this type of wireless transmission, a certain time slice (called a frame) is reserved for each user to transmit the data. When the frame transmission is over, the next user transmits his own frame, which can be transmitted at a different frequency. In this case, a certain time period must be allocated for the frequency synthesizer to complete the switching from one frequency to another. If less time is allocated for this frequency switching, more time can be allocated for data transmission, and hence, data transmission rates can be increased. In the GPRS standard, the frequency synthesizer is given less than 200 μs to switch from one frequency to another. As data rates increase, frequency synthesizer switching time is expected to be constrained even further.

Another important requirement of wireless standards that directly affect frequency synthesizers is spectral purity. Table 2.2 indicates the spectral purity requirements of some of the second generation wireless standards. The spectral purity requirements depend on several parameters, which include the data signal's dynamic range, channel spacing, and the modulation technique.

Standard	Phase noise requirement
GSM	-141dBc/Hz @ 3MHz
DECT	-131dBc/Hz @ 4.7MHz
DCS-1800	-123dBc/Hz @ 600KHz

Table 2.2: Spectral purity requirements of some 2G wireless communications standards

Chapter 3

Delta-Sigma Modulation

3.1 Introduction

Originally, the field of application for delta-sigma modulation was the conversion of signals between the analog and digital world with delta-sigma converters [4]. This field was later extended to a wider range of applications such as filters, and phase-locked loops.

In this chapter we will attempt to derive a linear model of the DSM. First, we will consider a linear model of the quantizer. Then, we will focus on a first-order DSM, a second-order DSM and a multistage noise shaping (MASH) structure to explain the concept of delta-sigma modulation. For each DSM, only digital implementations will be investigated. We also examine a higher order DSM that is more robust to DC input signals. The proposed linear model will be used to investigate the stability in the different types of DSMs.

3.2 Basic Delta-Sigma Modulator

Figure 3.1 depicts the general structure of the delta-sigma modulator. The delta-sigma modulator is a non-linear system with a filter (digital or analog), a feedback loop, and a quantizer, which operates at a frequency $f_{oversampled}$ several times higher than the Nyquist frequency f_s. The difference (delta) between the signal and the feedback signal is accumulated (sigma) into an integrator, that is, the filter, and reduced to a finite number of levels by the quantizer. The filter in the loop attenuates the noise introduced by the quantization so that the quantization

noise, which remains at the DSM output, is low compared to the DSM input signal in the band of interest. This shaping action of the quantization noise is also referenced as noise shaping [4]. The quantization noise is removed either with a low-pass filter or a decimation stage placed at the DSM output.

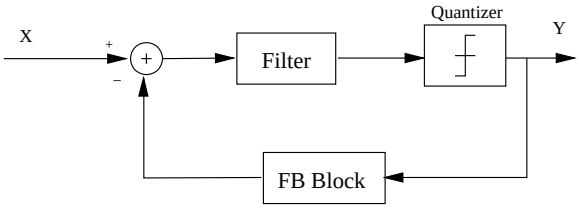


Figure 3.1: General structure of DSM

The oversampling ratio (OSR) is defined as the ratio between the sampling frequency $f_{oversampled}$ and the Nyquist frequency $f_s = 2.f_B$. For example, for a sinusoid of 600kHz, the Nyquist frequency is 1.2MHz to avoid aliasing. An oversampling ratio of 16 corresponds to a sampling frequency of 19.2MHz. The order of the modulator refers to the number of integrators in the DSM. The order of each DSM is added when the DSMs are placed in cascade in a structure, referenced later as MASH.

3.3 Quantization of a Signal From Multi-Bits to Single-Bit

The quantizer reduces a multi-bit input to a finite set of levels. The step size Δ is defined by

$$\Delta = \frac{2.X_{max}}{2^m} = \frac{X_{max}}{2^{m-1}} \tag{3.1}$$

where X_{max} is the maximum amplitude of the input and 2^m is the number of levels coded with m bits.

For inputs in the range $[-\Delta, \Delta]$, as demonstrated in Figure 3.2, the error is bounded, and the quantization error has a probability of lying anywhere in the range $\frac{\pm\Delta}{2}$ [25]. Figure 3.3 illustrates the probability density function for a rounding quantizer.

For a 1-bit quantizer, the variance [1] of the quantization noise is $\sigma_e^2 = \frac{1}{\Delta}\int_{\frac{-\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12}$, where Δ is the level spacing.

[1] The variance corresponds to mean square value of the signal e.

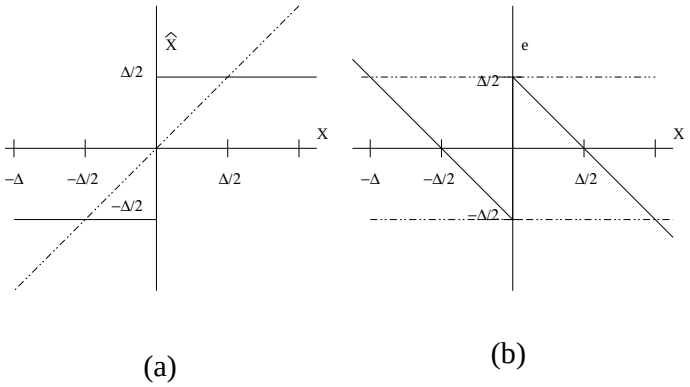


Figure 3.2: Multi-bits to 1-bit quantization: (a) quantizer output vs. input, and (b) quantization error

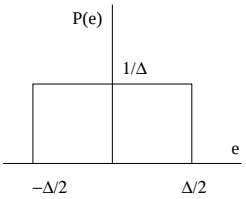


Figure 3.3: Quantization probability density function

In the first approach to linearize the quantization process, the quantizer is modeled by an additive white noise source with the following assumptions [25]:

- The error sequence is a sample sequence of a stationary random process.
- The error is uncorrelated with the input.
- The variance corresponds to the mean square value of the signal e.
- The error is a white noise process.
- The probability of distribution of the error is uniform over the quantization error.

In the delta-sigma modulator, a more sophisticated model of the quantizer such as the one proposed by Ardalan and Paulos [2] is required. An attenuation of the input by a gain g(x), which is dependent on the amplitude of the DSM input, is inserted before the additive white noise source, as illustrated in Figure 3.4.

For a small amplitude, no saturation occurs at the modulator and $g(x) \approx 1$. When the amplitude increases, the gain diminishes (i.e., $g(x) \rightarrow 0$).

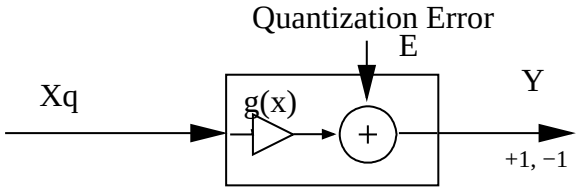


Figure 3.4: Quantizer linear model [2]

3.3.1 Different Types of DSM

First, we will present simple examples of delta-sigma modulators (DSM) with one integrator or two integrators. A methodology to obtain a stable high order modulator follows.

If we assume the previous linear model for the quantizer is valid, in the z-domain the DSM output, noted Y in Figure 3.1, can be expressed as a linear contribution from the small amplitude input X, and the quantization noise E given as follows:

$$Y(z) = H_{stf}.X(z) + H_{ntf}.E(z) \tag{3.2}$$

where H_{stf} is the signal transfer function, and H_{ntf} is the noise transfer function.

3.3.2 First-Order DSM

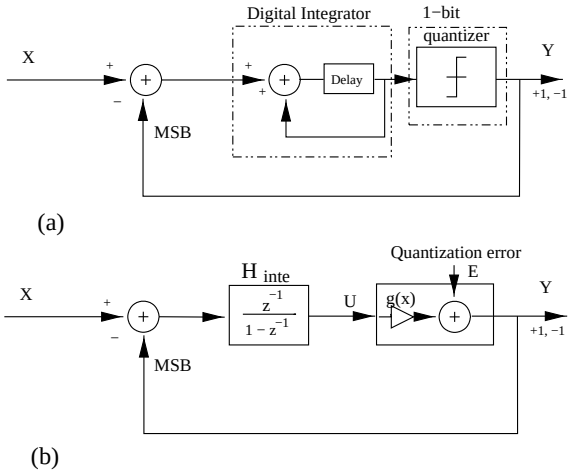


Figure 3.5: First-order DSM: (a) architecture, and (b) equivalent linear model

Figure 3.5(a) depicts a first-order delta-sigma modulator, which is composed of a digital inte-

grator, a quantizer, and a feedback loop. If the input and the quantization noise are uncorrelated, the quantizer is modeled by the quantizer model presented in Figure 3.4 as shown in Figure 3.5(b); the first-order DSM output is then given by

$$\begin{aligned} Y(z) &= \frac{H_{inte}}{1+H_{inte}}.X(z) + \frac{1}{1+H_{inte}}.E(z) \\ &= (z^{-1}).X(z) + (1-z^{-1}).E(z) \end{aligned} \tag{3.3}$$

where H_{inte} is defined by

$$H_{inte} = \frac{z^{-1}}{1-z^{-1}} \tag{3.4}$$

The magnitude of the signal transfer function, $|H_{stf}(z)|_{z=e^{\frac{2j\pi f}{f_s}}}$, and the noise transfer function $|H_{ntf}(z)|_{z=e^{\frac{2j\pi f}{f_s}}}$ are obtained by the identification of the terms between the general equation (3.2) and (3.3). Thus $|H_{stf}(f)| = 1$ and $|H_{ntf}(f)| = 2.sin(\frac{\pi f}{f_s})$ with $\frac{f_s}{2} \geq f \geq 0$, as illustrated in Figure 3.6(b). If we assume that the signal and quantization noise are uncorrelated, the output power spectral density may be given

$$S_Y(f) = |H_{stf}|^2.S_X(f) + |H_{ntf}|^2.S_E(f) \tag{3.5}$$

To illustrate the noise shaping action of the DSM, we apply a sinusoid with amplitude A, frequency f_o, and variance $\sigma_x^2 = \frac{A^2}{2}$ to the DSM input X. We assume a white quantization noise source E of variance $\sigma_e^2 = \frac{\Delta^2}{12}$, and also, we assume $\Delta = 1$ for the 1-bit quantizer.

In Figure 3.6(c), we can see that the signal spectrum remains unmodified by the signal transfer function (H_{stf}), while the noise spectrum is shaped by the modulator noise transfer function (H_{ntf}); then there is less quantization noise at low frequencies. The signal to noise ratio is improved when the noise at high frequencies is filtered. The SNR[2] is expressed by

$$SNR = 10.log\Big(\frac{\sigma_x^2}{\frac{1}{12}(\frac{\pi^2}{3})(\frac{2.f_B}{f_s})^3}\Big) \tag{3.6}$$

Provided that the amplitude of the input is small, the first-order modulator is stable (in

[2]The expression of the SNR is derived from the calculations developed in appendix A.

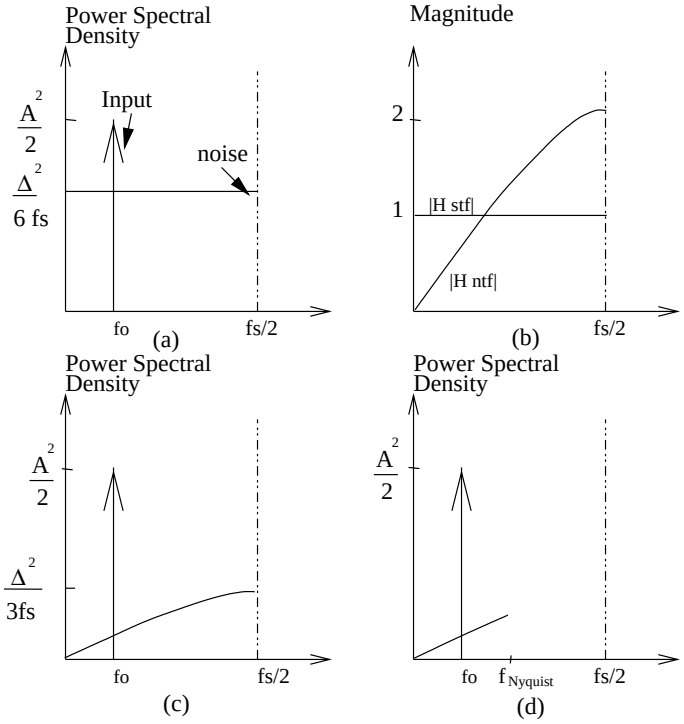


Figure 3.6: Noise shaping in the first-order DSM: (a) input spectra, (b) signal and noise transfer functions, (c) output spectra, and (d) down sampling to Nyquist frequency

the sense that bounded inputs lead to bounded outputs), as we will demonstrate in one of the following structures. In the case where the amplitude of the input signal is large, compared to the quantizer maximum level, the assumption g(x)=1 in (3.3) is no longer valid. It results in a modification of the signal transfer function and noise transfer functions, which are presented in appendix A.

3.3.2.1 Other Structures for the First-Order DSM

The delay in the signal transfer function can be suppressed (i.e., $H_{stf}(z) = 1$), by the modified structure of the DSM, shown in Figure 3.7. The digital integrator is replaced by the equivalent transfer function in Figure 3.7(b), and a delay is placed in the feedback. This is expressed in the following equation:

$$H_{inte} = \frac{1}{1 - z^{-1}} \tag{3.7}$$

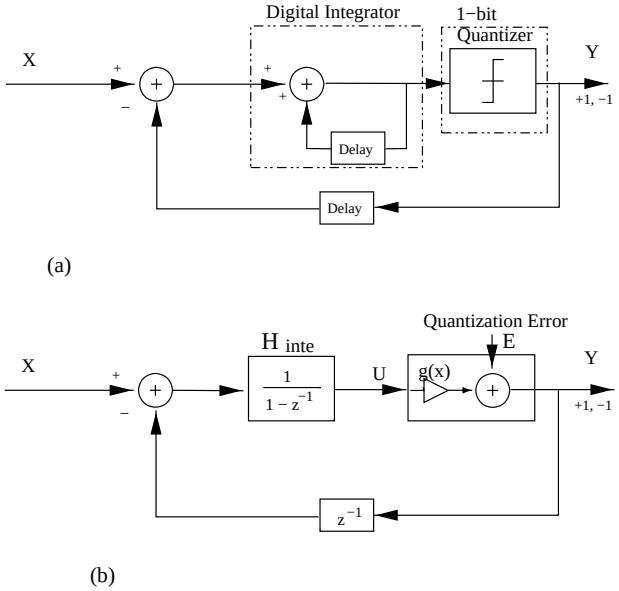


Figure 3.7: Second architecture of first-order DSM: (a) architecture, and (b) equivalent linear model

The contribution to the output Y of the input X and E is given by

$$\begin{aligned} Y(z) &= \frac{H_{inte}}{1 + z^{-1}.H_{inte}}.X(z) + \frac{1}{1 + z^{-1}.H_{inte}}.E(z) \\ &= X(z) + (1 - z^{-1}).E(z) \end{aligned} \tag{3.8}$$

Here, the noise transfer function is the same as previously, $|H_{ntf}(f)| = 2.sin(\frac{\pi f}{f_s})$ with $\frac{f_s}{2} \geq f \geq 0$. The noise is pushed close to the sampling frequency, while the signal remains unchanged. In a digital DSM, the contribution to the output Y is equivalent when the filter is placed in the feedback loop (see Figure 3.8), or when it is placed in front of the quantizer (see Figure 3.7). However, the number of delays is not the same. The modulator with error feedback (Figure 3.8) is only equivalent, when it is implemented with a digital circuit. Otherwise, the inaccuracies in the analog substractors strongly modify the modulator's properties [26].

3.3.2.2 State-Space Representation and Stability of the First-Order DSM

The first-order DSM is described by the following set of equations, which are referenced later as state-space equations of the first-order DSM:

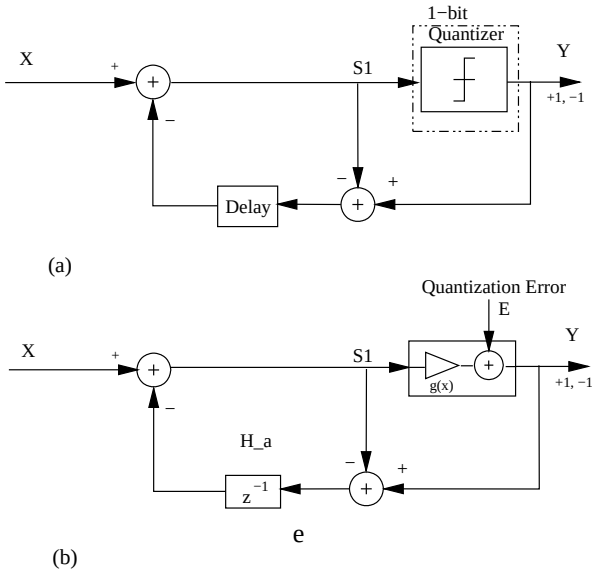


Figure 3.8: Third architecture of first-order DSM: (a) architecture, and (b) equivalent linear model

$$\begin{aligned} S_1|[n] &= x[n] - e[n-1] \\ y[n] &= \theta(S_1[n]) \\ e[n] &= y[n] - S_1[n] \end{aligned} \tag{3.9}$$

where the non linear function $\theta(y)$ is defined by

$$\theta(y) = \begin{cases} +1, & if y > 0 \\ -1, & if y \leq 0 \end{cases} \tag{3.10}$$

The choice of the value of $\theta(y)$, when $S_1[n] = 0$, is arbitrary, and we can also choose the output Y to be -1 or a random choice between 1 and -1.

The 1-bit quantizer dynamic implies that for small inputs S_1, the state variable which characterizes the input of the quantizer (i.e., $S_1[n] \leq 2$), the quantization error e is bounded (i.e., $|e[n]| \leq 1$). Assuming that $x[n+1] < 1$, we conclude that

$$|S_1[n+1]| \leq |x[n+1]| + |e[n]| \leq 2 \tag{3.11}$$

For all $|S_1[0]|$, and for $|x| < 1$, it can be proven that after a certain n, $|S_1[n]| \leq 2 \Rightarrow |S_1[n+1]| \leq 2$.

For small inputs ($X \leq 1$), the system is stable, because the bounded values from the input x and the feedback y lead to a bounded value of the quantizer input S_1.

In conclusion, an input of the first-order modulator that is smaller than one is a necessary and sufficient condition to insure the stability of the modulator. If $X > 1$, a scaling factor k, placed at the input, insures that this condition is respected ($k.X < 1$). The scaling factor k affects only the amplitude of the input signal. Because the input of the quantizer is bounded, we assume that $g(x) \approx 1$.

3.3.2.3 Problems Related to the First-Order DSM

When the first-order DSM is fed with a DC input, the quantized signal bounces between two levels and may be periodic. For a DC input, the error is periodic, and the system shows limited cycles [26]. The frequency content of the quantization noise for the first-order DSM depends on the DC-input level [4]. If the noise tones are in the same bandwidth as the signal range, the signal is corrupted with noise. Peaks of noise appear for the fractional values of the input [4]. The largest peaks exceed the values predicted by the linear model, which implies a degradation of the observed SNR compared to the theoretical SNR from (A.6).

From this, we can conclude that the first-order DSM is not appropriate, if a chain of DSM is used. It may be easy to scale the first-order DSM, but this structure is also more vulnerable to the DC inputs.

There may be several possibilities to improve the behaviour of the first-order modulator toward DC inputs:

- Dithering: In order to avoid tones in the first-order DSM, the input is kept busy by a low-level white noise signal added to the input before the quantization, which makes the total quantization error behave like white noise [27]. However, depending on the statistical properties of the dithering signal used, the noise quantization is up to four times worse than in the undithered case [27].

- A pseudo noise sequence: If we artificially introduce a known binary noise at the input of

the DSM and then remove it after the DSM, the input of the quantizer is noise; therefore, the quantization noise of the DSM is likely to be white. The pseudo random noise is then removed from the output of the DSM. A shift register and some logic circuit generate the required pseudo random noise sequence. In the case of the maximum length sequence, an XOR gate combines a certain output from the shift register to generate the value of the first tap so that the total code has a given periodicity. An example of outputs to use is shown in Table 3.1. Usually, this technique is adopted in spread-spectrum modulation (CDMA).

Number Of Registers	MLS Length	Feedback Taps
2	2^2-1=3	[2,1]
3	2^3-1=7	[3,1]
4	2^4-1=15	[4,1]
5	2^5-1=31	[5,2]
6	2^6-1=63	[6,1]
7	2^7-1=127	[7,1]
8	2^8-1=255	[8,6,5,1]

Table 3.1: Examples of maximum length sequence of shift-register length two to eight

The length of the pseudo noise (PN) sequence is determined by the number of shift registers, the initial value, and feedback logic. Also, the number of shift registers is referred to as the order of the maximum length sequence (MLS). The length of the MLS is $2^{number\ of\ shift\ registers} - 1 = 2^{order} - 1$.

If we denote $c[n]$ to be the output of the PN generator, we have $c[n] = \pm 1$ so that $c[n] * c[n] = 1$.

We simulate a first-order DSM with a maximum length sequence, and the PN generator is placed, as shown in Figure 3.9.

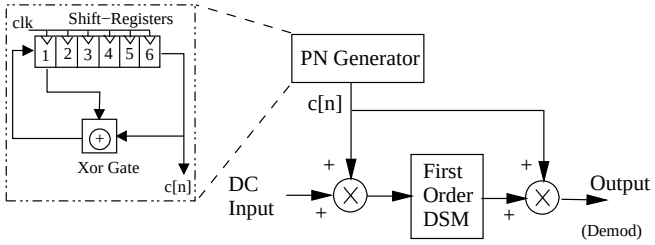


Figure 3.9: First-order DSM using pseudo noise sequence

When the output of the system is low-pass filtered, we should obtain the DC input that is fed

into the system if the filter is sharp enough. However, the simulation for a DC input level of 0.5 for PN sequences of 6 registers displays an additional signal, in Figure 3.10. The period of the signal depends on the length of the sequence, which is then be added to the DC value to control the divider. A sharper filter characteristic is needed to remove this undesirable signal component. The cutoff frequency of the sharp filter, shown in Figure 3.10, is $\frac{1}{20}$ of the normal one.

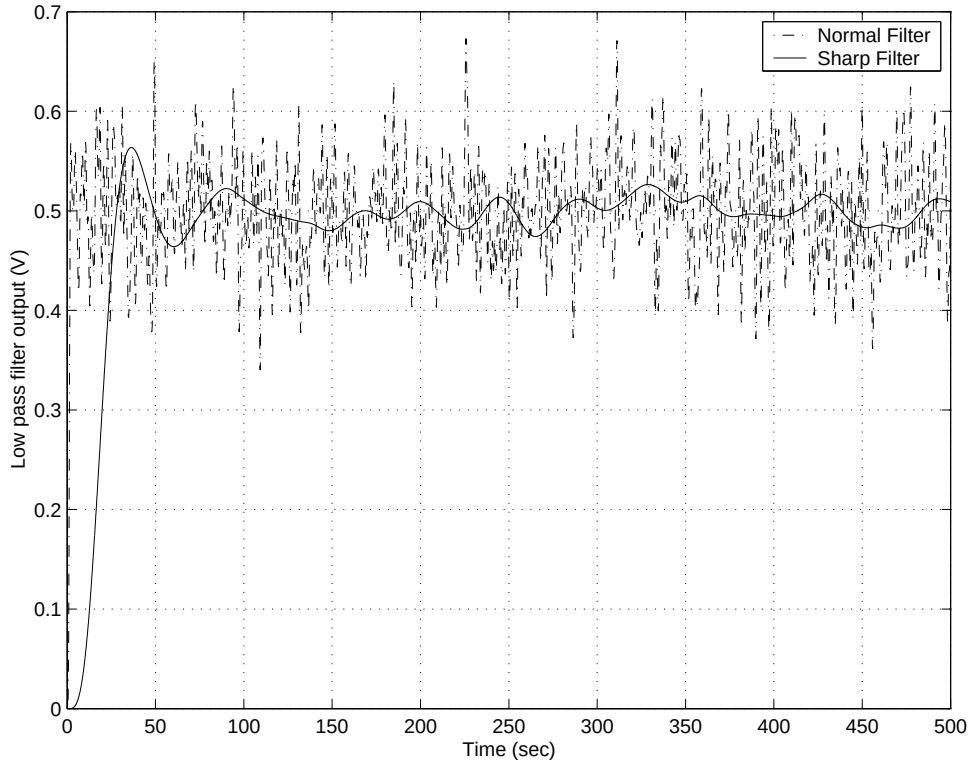


Figure 3.10: Pseudo noise sequence effect on the sharpness of the low pass output filter

In fact, if one considers a simplified model of the first-order DSM, the output of the second multiplier, referenced as *demod* in Figure 3.9, is the sum of several contributions given by the following:

$$\begin{aligned} demod[n] &= input[n] * c[n] * c[n] + (\sum_i h_{ntf}[i] * e[n-i]) * c[n] \\ &= input[n] + (\sum_i h_{ntf}[i] * e[n-i]) * c[n] \end{aligned} \tag{3.12}$$

The output *demod* depends on not only the input but also on the shaped quantization noise

$\sum_i h_{ntf}[i] * e[n-i]$ multiplied by the sequence from the pseudo noise generator. Therefore, the noise shaped spectrum of the quantization noise e is convolved with the spectrum of the pseudo noise sequence. The contribution of the additional signal increases with the length of the MLS. The pseudo noise sequence technique introduces more problems than it really solves: The DC problem in the DSM is replaced by a filter problem in the DSM, because a sharper filter is required to eliminate the unwanted components.

3.3.3 Second-Order DSM

The second-order DSM, illustrated in Figure 3.11(a) is composed of two digital integrators H_{inte1} and H_{inte2}, a quantizer, and two feedback loops.

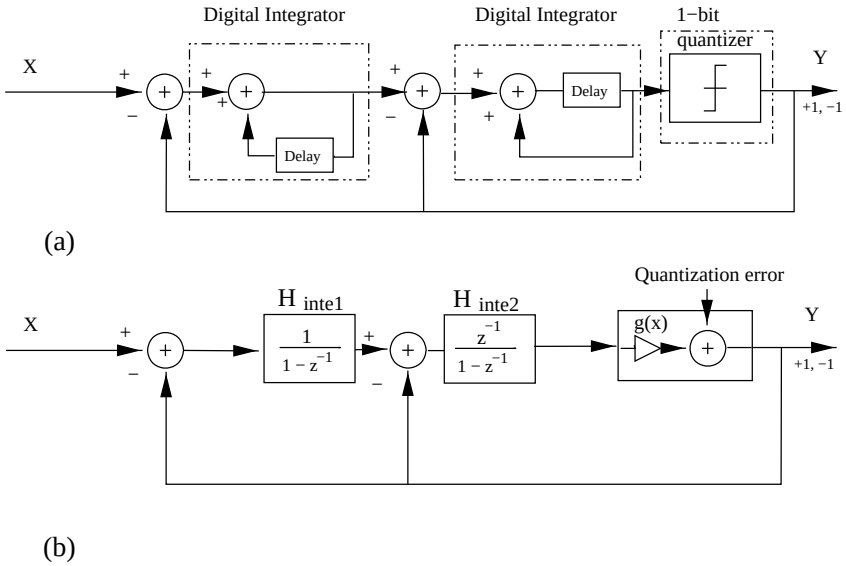


Figure 3.11: Second-order delta-sigma DSM: (a) architecture, and (b) equivalent linear model

In the z-domain, the output of the modulator $Y(z)$ is expressed as a linear contribution from the small amplitude input $X(z)$, and the quantization error $E(z)$ as in

$$
\begin{aligned}
Y(z) &= \frac{H_{inte1}.\frac{g(x)H_{inte2}}{1+g(x)H_{inte2}}}{1+H_{inte1}.\frac{g(x)H_{inte2}}{1+g(x)H_{inte2}}}.X(z) + \frac{1}{1+g(x)H_{inte2}(1+H_{inte1})}.E(z) \\
&= \frac{g(x).H_{inte1}.H_{inte2}}{1+g(x).H_{inte2}+g(x).H_{inte1}.H_{inte2}}.X(z) + \frac{1}{1+g(x)H_{inte2}+g(x).H_{inte1}.H_{inte2}}.E(z)
\end{aligned}
\tag{3.13}
$$

The equivalent transfer function of H_{inte1} and H_{inte2} is given by

$$H_{inte1} = \frac{1}{1-z^{-1}} \tag{3.14}$$

and

$$H_{inte2} = \frac{z^{-1}}{1-z^{-1}} \tag{3.15}$$

For $g(x) \approx 1$, (3.13) converts to

$$Y(z) = (z^{-1}).X(z) + (1-z^{-1})^2.E(z) \tag{3.16}$$

The noise transfer function is given by the following:

$$H_{ntf}(z) = \left.\frac{Y(z)}{E(z)}\right|_{X=0} = (1-z^{-1})^2 \tag{3.17}$$

Since $z = e^{\frac{2j\pi f}{f_s}}$ in the frequency domain, we obtain

$$H_{ntf}(f) = \left.\frac{Y(f)}{E(f)}\right|_{X=0} = \left(2.sin(\frac{\pi.f}{f_s})\right)^2 \tag{3.18}$$

The quantization noise of the second-order DSM is shaped by a sine elevated at the power of the DSM order. It is important to consider both the position of the poles and zeros, and the maximum gain of the transfer function (H_{stf} and H_{ntf}) to characterize the stability of the system. Indeed, if the quantizer input is large, compared to the quantizer range, then $g(x) < 1$ since the quantization error is large, compared to the output [2].

The expressions of the signal transfer function and the noise transfer function, when g(x) is

not equal to one, are given in Appendix A.

If the scaling factors are placed appropriately, they limit the maximum gain of the noise transfer function. If we place the scaling factors outside the DSM internal loop, the amplitude of the input signal is controlled without influencing on the signal transfer function for g(x) = 1. This is not the case if the scaling factors are introduced in the DSM loop. The signal transfer function of the DSM can be altered by the choice of the scaling factors.

For a high-order DSM with a single stage, the stability problem increases and makes the design of high-order modulator extremely difficult in a direct approach (with one quantizer and multiple feedback).

For example, Figure 3.12 illustrates, with the Evans root locus[3] of the noise transfer function $H_{ntf} = (1 - z^{-1})^3$, the variation in the noise transfer function due to the gain g(x). We can see that the system is unstable because the root locus crosses the unity circle.

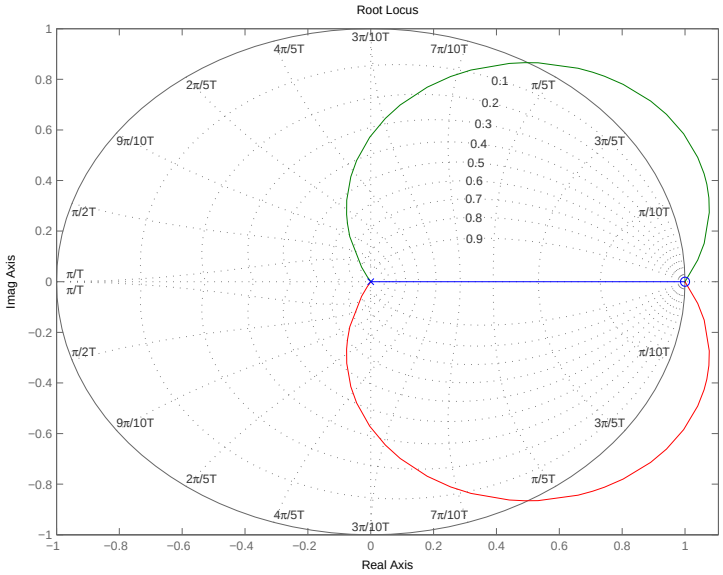


Figure 3.12: Root locus of the noise transfer function for third-order modulator with g(x)=1

For the modulator with $H_{ntf} = (1 - z^{-1})^n$, when n is greater than 2, the modulator is not stable: The output exhibits large states and poor SNR compared to the SNR predicted by linear models [26]. For the unstable DSM, the output presents a long sequence of ones and zeros with a low frequency.

[3]The root locus function plots the locus of the roots of H(z)=D(z)+k1*N(z), where D the denominator, N the numerator of the open loop gain, and k1 is a positive gain calculated to produce a smooth plot.

To ease the design process, we choose to cascade stable first-order and second-order, separated by scaling factors which insure a bounded input for each stage so that we can obtain a stable cascade of DSMs equivalent to a stable high-order DSM.

3.3.3.1 SNR of the Second-Order DSM

Under the same approximation as for the first-order DSM [4], the SNR of the second-order DSM is given by (3.19), with H_{ntf} from (3.18).

$$\begin{aligned} SNR|_{2^{nd}\ order\ DSM} &\approx 10.log\Big(\frac{\sigma_x^2}{2.\frac{\sigma_e^2}{f_s}.\int_0^{f_B}|2\frac{\pi.f}{f_s}|^4 df}\Big) \\ &\approx 10.log\Big(\frac{\sigma_x^2}{\sigma_e^2\frac{\pi^4}{5}(\frac{2.f_B}{f_s})^5}\Big) \end{aligned} \tag{3.19}$$

The general expression for the SNR in the Nth-order modulator, with a noise transfer function $H_{ntf}(f) = (2sin(\frac{\pi.f}{f_s}))^N$, is expressed by

$$\begin{aligned} SNR|_{N^{th}\ order\ DSM} &\approx 10.log\Big(\frac{\sigma_x^2}{2.\frac{\sigma_e^2}{f_s}.\int_0^{f_B}|2\frac{\pi.f}{f_s}|^{2N} df}\Big) \\ &\approx 10.log\Big(\frac{\sigma_x^2}{\sigma_e^2\frac{\pi^{2N}}{2N+1}(\frac{2.f_B}{f_s})^{2N+1}}\Big) \end{aligned} \tag{3.20}$$

Thus, the SNR may be improved by two parameters:

- The high sampling ratio, represented by $\frac{f_s}{2.f_B}$, improves the SNR. For example, doubling the OSR improves the SNR by 15 dB for the second-order DSM or 21 dB for the third-order DSM.
- For the order N of the DSM, the higher the order, the better SNR. For example, increasing the order from second to third improves the SNR by 11.5 dB for OSR=10, or 17.5 dB for OSR=20.

[4] $sin(x) \approx x$ for $x \to 0$ and the general expression used in (A.4).

3.3.3.2 Other Structure for the Second-Order DSM

Similar to the first-order DSMs, there are several structures of second-order DSMs that are available, for example, the second-order delta-sigma modulator with a single feedback and an error feedback structure, shown in Figure 3.13.

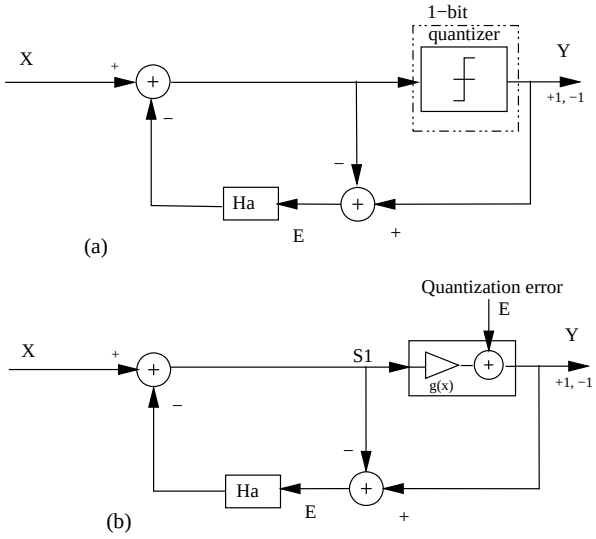


Figure 3.13: Alternative design of second-order DSM: (a) architecture, and (b) equivalent linear model

The second-order DSM with the error feedback structure is defined by (3.21).

$$Y(z) = X(z) + (1 - H_a(z))E(z) \tag{3.21}$$

H_a is chosen in (3.22) so that the noise transfer function is given by $H_{ntf}(z) = (1 - z^{-1})^2$. This is done to obtain the same noise transfer function as that of the second-order DSM presented earlier in this section.

$$H_a(z) = 1 - (1 - z^{-1})^2 = z^{-1}.(2 - z^{-1}) \tag{3.22}$$

The introduction of a pole in the noise transfer function H_{ntf} helps to stabilize the loop, and enhances the dynamic range. However, this pole produces more noise at low frequencies than the noise shaping loop with two zeros at z=0 [26].

We can plot $|H_{ntf}|$, given by (3.24), for g(x)=1, for different positions of the pole p_1 in Figure

3.14 to obtain a better insight into the modification implied by the introduction of the pole in the noise transfer function H_{ntf}. When g(x)=1, $H_{stf} = 1$ and H_{stf} is not modified by the position of the pole in the noise transfer function. Therefore, we only consider $|H_{ntf}|$. If the input is small and the pole keeps the quantizer input small, the approximation g(x)=1 is justified.

The modified version of H_a, with an additional pole is defined by

$$H_a(z) = 1 - \frac{(1 - z^{-1})^2}{1 - p_1.z^{-1}} = \frac{((2 - p_1) - z^{-1})z^{-1}}{1 - p_1.z^{-1}} \tag{3.23}$$

and the noise transfer function is given by

$$\begin{aligned} H_{ntf}(z) &= \frac{(1 - z^{-1})^2}{1 + (-p_1 + (2 - p_1).(g(x) - 1)).z^{-1} - (g(x) - 1).z^{-2}} \\ &= \frac{(1 - z^{-1})^2}{1 - p_1.z^{-1}} \quad \text{for } g(x) = 1 \end{aligned} \tag{3.24}$$

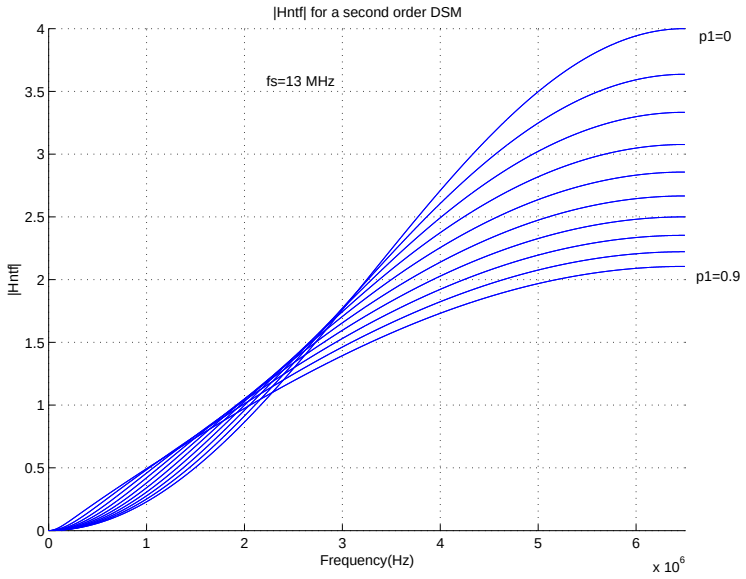


Figure 3.14: $|H_{ntf}(f)|$ with frequency in the range $[0, \frac{f_s}{2}]$ for second-order DSM

We can observe from Figure 3.14 that the maximum of the noise transfer function placed at $\frac{f_s}{2}$ decreases as $p_1 \to 0.9$, but in the same time, the noise at low frequencies increases. The choice of $p_1 = 0.5$ is a compromise between in-band noise and attenuation of the noise transfer function maximum.

3.3.3.3 State Space Representation of the Second-Order DSM

The DSM is a piecewise-linear system. It is defined by a set of equations, which describes the state of each point in the circuit that are valid in different regions. This is called the state-space method, where state variables correspond to the output of each integrator stage. We are primarily interested in the evaluation of the input of the quantizer denoted by the variable S_1. We can summarize the system in Figure 3.13, and H_a given by (3.22), by writing

$$\begin{aligned} S_1[n] &= x[n] - 2e[n-1] + e[n-2] \\ e[n] &= y[n] - S_1[n] \\ y[n] &= \theta(S_1[n]) \end{aligned} \tag{3.25}$$

with the non-linear function $\theta(y)$ defined by (3.10).

The 1-bit quantizer dynamic implies that for small inputs S_1 (i.e., $S_1[n] \leq 2$), the quantization error e is bounded (i.e., $|e[n]| \leq 1$).

With the hypothesis that $|S_1[n]| \leq 2$ and $x[n+2] < 1$, it follows that

$$|S_1[n+2]| \leq |x[n+2]| + 2|e[n+1]| + |e[n]| \leq 4 \tag{3.26}$$

even when $x = 0$, then $|S_1[n+2]| \leq 2|e[n+1]| + |e[n]| \leq 3$. This proves that the position of the poles and zeros within the unity circle is a necessary condition for stability, but it is not sufficient to insure that S_1 will not saturate the quantizer.

If we introduce a pole in the noise transfer function, H_a is expressed by (3.23) and the state space equations are given by

$$\begin{aligned} S_1[n] &= x[n] - \sum_{i=1}^{\infty} h_a[i] * e[n-i] \\ e[n] &= y[n] - S_1[n] \\ y[n] &= \theta(S_1) \end{aligned} \tag{3.27}$$

with the non linear function $\theta(y)$ defined by (3.10).

Again, we assume that $|S_1[n]| \leq 2$ and $x[n+2] < 1$.

Thus,

$$|S_1[n+2]| \leq |x[n+2]| + \sum_{i=1}^{\infty} h_a[i] * e[n-i] \tag{3.28}$$

If we consider the same expression in the frequency domain, we obtain

$$|z^2.S_1(z)| \leq |z^2.X(z)| + \Big|\frac{(1-z^{-1})^2}{1-p_1.z^{-1}} - 1\Big|.|E(z)| \tag{3.29}$$

The function $f_p(z) = |\frac{(1-z^{-1})^2}{1-p_1.z^{-1}} - 1|$ is maximum at the Nyquist frequency (i.e $z = -1$) which is clearly seen in Figure 3.14.

Therefore,

$$|S_1[n+2]| \leq |x[n+2]| + \Big(\frac{4}{1+p_1} - 1\Big).max|e[n]|, \quad with \;\; 1 > p_1 > 0 \tag{3.30}$$

Furthermore, $1 > p_1 > 0$ implies that $3 > \frac{4}{1+p_1} - 1 > 1$, and for $1 > p_1 > \frac{1}{3}$, $2 > \frac{4}{1+p_1} - 1 > 1$. If $1 \geq p_1 \geq \frac{1}{3}$, $|S_1[n]| < 2, |x| < 2 - (\frac{4}{1+p_1} - 1)$ and $max|e[n]| = 1$, we have $|S_1[n+2]| < 2$. The amplitude of S_1 is controlled by the choice of the appropriate pole p_1 and by the input signal amplitude. The system is stable as the additional pole avoids the saturation of the quantizer, while the poles and zeros remain within the unity circle.

With scaling factors and an additive pole in the noise transfer function, the input of the quantizer can be kept low, and thereby, insure stability. In a stable system, bounded inputs, DSM input and feedback from the quantizer, should lead to a bounded input to the quantizer, and thereby, a bounded output signal.

More literature can be found on the stability of the second-order DSM in related publications: for DC inputs [28], for sinusoidal inputs with low frequency and DC-average [29], and for stability of a second-order DSM [30]. Stability under constant inputs is a necessary condition for stability under more general inputs.

A scaling strategy which takes into account the SNR was proposed by Zakhor and Hein [31] for the second-order modulator with double feedback. The scaling factors improve the SNR, but the chosen values may not lead to values that are practical enough for implementation.

3.3.4 MASH Structure

Delta-sigma modulators of small orders (with few integrators) have a limited signal to noise ratio (SNR). The order of the DSM is increased to improve the SNR, while the OSR remains unchanged.

Higher order modulators with several feedbacks are not always stable, but this problem was overcome in the structure referred as MASH, proposed in [17], where a cascade of first-order modulators progressively shape the quantization noise at the output to a high degree.

If we low-pass filter the output of the MASH, the high frequency component $H_{ntf}(z).E(z)$ is eliminated, while the low frequency component $X(z)$ remains unchanged.

The total order of the modulator is determined by the number of low-order modulators that are placed in cascade. Usually, the third-order to fifth-order ones are used. We will give the equation associated with a third-order MASH, depicted by Figure 3.15, and extend it to n-order case in Chapter 4.

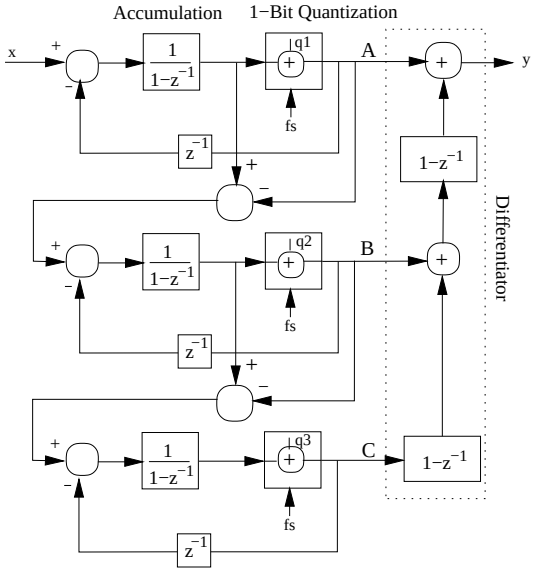


Figure 3.15: MASH 1-1-1 architecture

As for low-order DSM, the output y is a summation of the different contributions from the input X and several 1-bit quantizers q_1, q_2, q_3. If the quantization noise is assumed not to be correlated with the input, the expression of $Y(z)$ is given by

$$\begin{aligned} Y(z) &= A + B(1-z^{-1}) + C(1-z^{-1})^2 \\ &= X(z) + Q_1(z)(1-z^{-1}) \\ &+ (-Q_1 + Q_2(z)(1-z^{-1}))(1-z^{-1}) \\ &+ (-Q_2 + Q_3(z)(1-z^{-1}))(1-z^{-1})^2 \\ &= X(z) + (1-z^{-1})^3 Q_3(z) \\ &= X(z) + H_{noise}(z)Q(z) \end{aligned} \tag{3.31}$$

The output Y of the MASH architecture is a linear contribution from the different stages of the DSM. The lower-order stages are digitally compensated for so that only the highest noise shaping contribution remains. In the example of MASH 1-1-1, the modulator is stable for $|x| < 1$. It is based on a succession of first-order DSMs which are stable for $|x| < 1$. Each output is assigned the values ± 1, and this insures that the quantization noise fed into the next stage is also in the range ± 1.

The first-order DSM presents strong idle tones for DC inputs. Therefore, a second-order modulator is better suited for the first stage of the MASH structure. With a second-order modulator in the first stage, there is a smaller amount of noise in-band to be cancelled. Even when some of the noise of the modulator is not properly cancelled by the following stages in the MASH, the noise leakage has a second-order shaping characteristic.

Generally, we place all the second-order modulators first to obtain a strong noise shaping in the first stages. Due to the potential for imperfect cancellation, the number of stages are often limited to three in practice.

Scaling factors are introduced between each stage, and additional poles may be placed in each second-order stage to insure the stability of the MASH structure.

The expression of Y for the MASH 2-2-1, illustrated in Figure 3.16, is given by

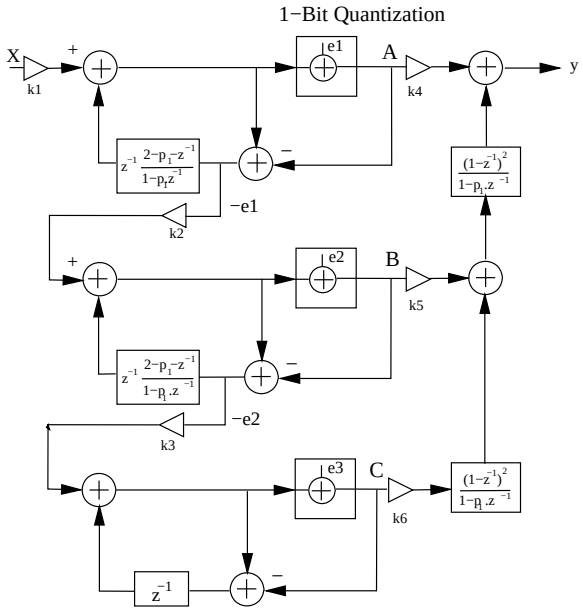


Figure 3.16: MASH 2-2-1 architecture

$$\begin{aligned} Y(z) &= k_4.A + k_5.B.\Big(\frac{(1-z^{-1})^2}{1-p_1.z^{-1}}\Big) + k_6.C.\Big(\frac{(1-z^{-1})^2}{1-p_1.z^{-1}}\Big)^2 \\ &= k_1.k_4.X(z) + k_4.E_1(z)\Big(\frac{(1-z^{-1})^2}{1-p_1.z^{-1}}\Big) \\ &+ k_5\Big[-k_2.E_1 + E_2(z)\Big(\frac{(1-z^{-1})^2}{1-p_1.z^{-1}}\Big)\Big].\Big(\frac{(1-z^{-1})^2}{1-p_1.z^{-1}}\Big) \\ &+ k_6\Big[-k_3.E_2 + E_3(z)(1-z^{-1})\Big].\Big(\frac{(1-z^{-1})^2}{1-p_1.z^{-1}}\Big)^2 \end{aligned} \tag{3.32}$$

For $(k_1.k_4 = 1; k_2.k_5 = k_4; k_3.k_6 = k_5; k_1 < 1; k_2 < 1; k_3 < 1)$, (3.32) translates to

$$\begin{aligned} Y(z) &= X(z) + k_6(1-z^{-1})\left(\frac{(1-z^{-1})^2}{1-p_1.z^{-1}}\right)^2.E_3(z) \\ &= X(z) + \frac{1}{k_1k_2k_3}(1-z^{-1})\Big(\frac{(1-z^{-1})^2}{1-p_1.z^{-1}}\Big)^2.E_3(z) \\ &= X(z) + H_{ntf}(z).E(z) \end{aligned} \tag{3.33}$$

The poles and scaling factors in the noise transfer function of the second-order stages insure

the stability of the system, without modifying the frequency characteristic of the signal transfer function. The choice of the scaling factors and poles is a compromise between the SNR requirement and stability requirement. If the scaling factors are chosen as power of two, the divisions and multiplications by two are implemented with bit shifters.

We notice from (3.33) that the SNR at the output Y depends on the input scaling factors. The scaling factors limit the internal signals amplitude, and maintain the input of the quantizer in a bounded range of values. This results in a bounded value for the quantization noise in each stage. If the chosen input scaling factors are too large, the cascade of stages may lead to large amplitude signals with strong tones in the noise spectrum.

3.4 Conclusion

We have briefly described delta-sigma modulation and the concept of noise shaping. Different delta-sigma modulators with the stability issues of each type were reviewed. Also, we have shown how to model these non-linear systems with a state-based structure. In addition, we considered some aspects concerning the application of delta-sigma modulation to fractional frequency synthesis for a MASH structure. The design of the fractional-N synthesizer by using the delta-sigma modulator and the MASH structure will be detailed in the Chapters 4 and 5.

Chapter 4

Fractional-N PLL

4.1 Introduction

The Phase-Locked Loop (PLL) concept is still popular, even though it was proposed many years ago. The PLL provides both a good frequency accuracy and a good phase noise performance within a wide tuning range. The PLL is used for frequency synthesis, signal regeneration, and in applications such as televisions, radio receivers, and transceivers.

The fractional-N PLL frequency synthesizer is considered to be the dominant frequency synthesis method for most wireless applications. The synthesizer has the merit of a fast lock time and a low phase noise. Its design has a large impact on the power consumption, area, and overall transceiver performance.

In this chapter, we will first explain the principle of fractional-N (FN) synthesis, and then present possible implementations of FN synthesizers. The introduction of modulated information, and the use of delta-sigma modulation in the fractional N PLL will also be presented.

4.2 PLL Basics

As shown in Figure 4.1, the PLL is a circuit which follows and reproduces a reference signal over a wide frequency range. The phase of a reference signal X_r is compared to the phase of the output signal X_{vco} from the voltage control oscillator (VCO) in the phase comparator (PD). The mean value of the output signal from PD, X_{PD}, is equal to the phase error between X_{ref} and X_{vco} .

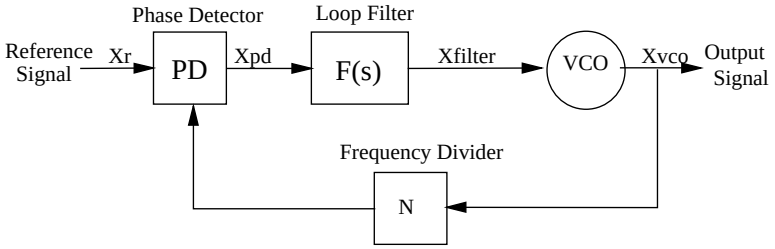


Figure 4.1: Basic PLL

The output of the filter X_{filter} is directly proportional to the phase difference between X_{ref} and X_{vco} . The phase-error at the output of the filter X_{filter}, controls the input voltage of the VCO to obtain the proper frequency.

If a frequency divider is placed between the VCO output and the phase detector in the feedback loop, the output frequency f_{vco} is then $f_{vco} = N.f_{ref}$, which represents the basic frequency synthesis.

4.2.1 Loop Parameters

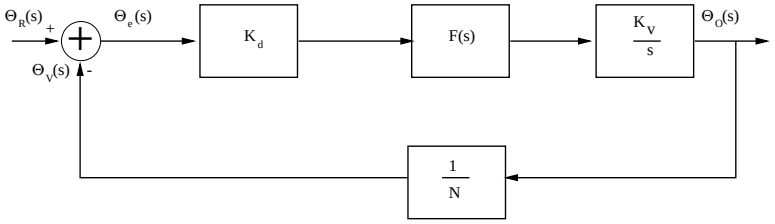


Figure 4.2: PLL linearized model

Often, a linear approximation is made to model the non-linear transient response of the PLL. The parameters of the PLL design are then given by an open-loop and a closed-loop transfer function. In Figure 4.2, the phase detector is modeled as a subtracter followed by a multiplication factor K_d . The VCO Laplace transfer function is $\frac{K_{vco}}{s}$. The open-loop transfer function of the PLL is given by

$$H_{open\ loop}(s) = \frac{K_d.F(s).K_v}{s} \tag{4.1}$$

The closed-loop transfer function is given by

$$\begin{aligned} H_{closed\ loop}(s) &= \frac{\Theta_O(s)}{\Theta_R(s)} \\ &= \frac{H_{open\ loop}}{1 + \frac{H_{open\ loop}}{N}} \\ &= \frac{\frac{K_d.F(s).K_v}{s}}{1 + \frac{K_d.F(s).K_v}{Ns}} \end{aligned} \tag{4.2}$$

As the loop filter introduces one or more poles, it is possible to compare (4.2) with the general second-order system equation,

$$H_{TF}(s) = \frac{{\omega_n}^2}{s^2 + 2.\xi.\omega_n.s + {\omega_n}^2} \tag{4.3}$$

where ξ is the damping factor, and ω_n is the natural frequency of the system.

If we choose $\xi \geq 1$, the roots of the denominator are two real constants ($s_{1,2} = \omega_n(-\xi \pm \sqrt{\xi^2 - 1})$). However, the system has a slow response but without oscillation. If we choose $\xi < 1$, the roots of the denominator are two complex constants ($s_{1,2} = \omega_n(-\xi \pm j\sqrt{1 - \xi^2})$). Then the system has a fast response, but with oscillation.

The value of ξ is set to $\frac{1}{\sqrt{2}}$ to provide a frequency response for an equivalent second-order system.

In the following section, several examples of transfer functions for the low-pass filter F(s) are described, and the PLL closed-loop transfer function, the damping factor and natural frequency are derived.

4.2.2 PLL Blocks

The PLL is composed of the following blocks:

- The reference signal is often obtained from a crystal quartz with a very accurate frequency.
- A phase detector compares the phase of the reference signal and the generated signal from the VCO.
- A loop filter follows the phase detector to limit the bandwidth of the loop and extracts the phase-error. Several types of filters (active or passive, analog or digital, with various

orders) condition the dynamics of the system.

- The input voltage of the VCO controls the generated frequency at the output of the oscillator.
- The output of the VCO is fed back to the phase detector, sometimes after a frequency-divider stage. The frequency divider is optional, but it has the possibility to generate an output frequency proportional by a factor N to the reference frequency.

4.2.2.1 Phase Detector

The phase detector, also known as the phase comparator, compares the phase of the reference signal and the feedback from the output signal to generate a signal proportional to the phase error.

Several digital implementations of the phase detector such as the edge triggered JK-flipflop, the XOR gate, and the phase frequency detector (PFD) exist. These implementations result in different characteristics of an average output signal versus the phase error θ_e as portrayed in Figure 4.2.

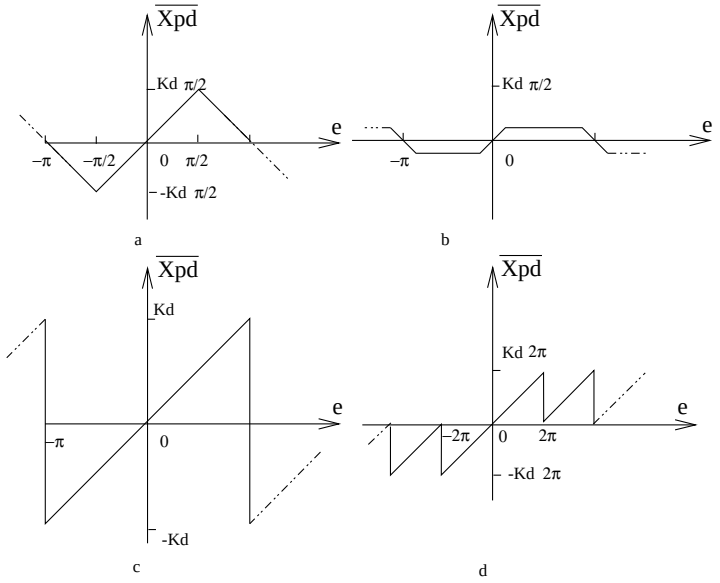


Figure 4.3: Average signal at the output of the phase detector versus phase error for different types of digital phase detectors: (a) XOR phase detector with symmetrical square waves, (b) XOR phase detector with asymmetrical square waves, (c) JK-flipflop phase detector, and (d) PFD.

The phase detector pulses have an amplitude equal to the supply voltage VDD, and the phase gain K_d is given by

$$K_d = \frac{V_{DD}}{4\pi} V/rad \tag{4.4}$$

4.2.2.2 Loop Filter

Different structures are available for the loop filter (passive or active, analog or digital) which lead to different filtering characteristics, that is, different forms for the transfer function F(s) in the phase-locked loop.

We are interested in a low-pass characteristic for F(s) to extract a low-frequency or mid-frequency signal to control the VCO output frequency f_{VCO}.

Passive Analog Filters

From the various types of passive filters, we consider only those that are based on resistors and capacitors. Since, inductors are difficult to implement in a system-on-chip approach.

A capacitor in serial is a high-pass filter, whereas a capacitor in parallel is a low-pass filter. Because a capacitor is not ideal, it is always possible to extract an associated serial resistor R_2. The connection wires to access the filter are also resistive, and we can extract a parasitic resistor R_1. Therefore, the passive lag filter from Figure 4.4 is a general structure for a first-order passive analog filter.

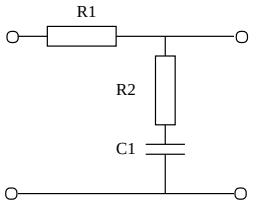


Figure 4.4: First-order passive analog filter

The transfer function of the filter from Figure 4.4 is given by

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{4.5}$$

where $\tau_1 = R_1 C_1$ and $\tau_2 = R_2 C_1$.

This transfer function can be approximated to an ideal integrator, if the leakage current is neglected and if a PFD-type is used for the phase detector [32]. Figure 4.5 depicts the consequence of the approximation on the transfer function F(s). Thus, (4.5) can be approximated to be

$$F(s) = \frac{1 + s\tau_2}{s(\tau_1 + \tau_2)} \tag{4.6}$$

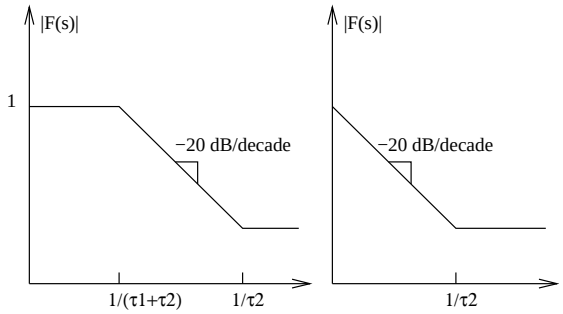


Figure 4.5: Bode plots of the transfer functions in (4.5) and (4.6)

The associated closed-loop transfer function, if we replace the latest expression of F(s) in (4.2), is given by

$$\begin{aligned} H_{closed\ loop}(s) &= \frac{\frac{K_d.F(s).K_v}{s}}{1 + \frac{K_d.F(s).K_v}{Ns}} \\ &= \frac{K_d.K_v(1 + s\tau_2)}{s^2(\tau_1 + \tau_2) + (1 + s\tau_2)\frac{K_d.K_v}{N}} \end{aligned} \tag{4.7}$$

By an analogy with (4.3), we obtain $\omega_n = \sqrt{\frac{K_d.K_v}{N(\tau_1+\tau_2)}}$, and $\xi = \frac{\omega_n.\tau_2}{2}$.

We can see that the closed-loop transfer function is always one order higher than the order of the transfer function F(s). Commonly, the order of the PLL design refers to the order of the closed-loop transfer function. A first-order loop filter leads to a second-order PLL, and a second-order loop filter to a third-order PLL.

A simple way to obtain higher order passive filters without using inductors is to cascade the first-order passive analog filter that is shown in Figure 4.4.

For example, a cascade of two identical first-order filters gives a second-order filter with a transfer function given by

$$F(s) = \Big(\frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}\Big)^2 \tag{4.8}$$

In analog IC design or mixed signal IC design, the most popular filters are often the simple ones: first-order and second-order based on the passive RC-filter, or a single operational amplifier.

The PFD produces a large rectangular excursion (ripple) on each cycle of operation, which can be sufficiently filtered by a first-order RC stage placed at the output of the PFD/charge pump block. If not filtered properly, these ripples lead to frequency side-bands at the VCO output [33]. A second capacitor is placed in parallel to improve the ripple filter with a pole placed further than ten times the loop bandwidth. This additive pole is carefully chosen to maintain the adequate stability margin. Active components such as operational amplifiers increase the noise contribution to the overall circuit, whereas only a limited bandwidth can be achieved due to the amplifier slew rate.

Digital Filters

Digital filters can be easily reprogrammed to meet multi-standard specifications. Their performance does not depend as much that of analog filters on the precision of the component values. It is possible to filter most of the signal in the digital domain, while an analog filter with limited requirements can be placed between the digital to analog converter and the VCO.

Because a digital phase detector is often used, the single-bit detector output can be applied to a digital filter. The analog filter specifications are mapped into the digital filter with either an impulse invariant or a bilinear z-transform.

The specification of the loop transfer function F(s) is transformed into the z-domain. Then, the loop transfer function becomes $F(z)|_{z=e^{\frac{s}{f_s}}}$. The sampled input and output signals of the filter exist only at a discrete time with a sampling frequency f_s, which is chosen to be much larger than the filter 3-dB corner frequency. If the sampling frequency is low compared to the input signal frequency, time aliasing occurs.

A digital filter is defined by its impulse response, in the z-domain as follows:

$$F(z) = F^*(s)|_{z=e^{\frac{s}{f_s}}} = \frac{1}{f_s}\sum_{0}^{\infty} f(n)z^{-n} \tag{4.9}$$

where $F^*(s)$ is a sampled version of $F(s)$.

The transfer function F(z) is implemented with an Infinite Impulse Response (IIR) filter, because the long delays, introduced by the long FIR, are not suitable for a PLL.

The need of a digital-to-analog converter between the filter and the VCO is a drawback for the digital filters in the PLL. The output signal from the PFD contains frequencies from DC to f_{ref}. Even though a filtering in the digital domain is more flexible, a multi-bit signal is required with a high sampling frequency to obtain a fine resolution for the output signal. Because a multi-bit high speed DAC is a power consuming solution, the choice of digital filter in PLL design may be unwise. Also, if the quantization noise from the DAC of the filter is not filtered properly, it modulates directly the VCO. As a result, the transmitter's performance is degraded.

However, no digital-to-analog conversion is needed when an analog filter is placed after the PFD, which use a charge pump scheme. The output of the charge pump stage detector is directly amplified and filtered to control the VCO output frequency.

Finally, we can implement an analog filter with digital control to obtain a flexible filter or a fast locking time. A digital switch short-circuits a resistor to modify the filter characteristics. The analog design in this last approach is a drawback, and the precision of the filter relies on the precision of the analog components used.

4.2.2.3 VCO

A VCO converts a continuous input voltage to a high frequency signal. Several performance criteria for the design of the VCO are the main concern. The criteria include cost, power consumption, linearity, supply and substrate noise rejection, jitter and phase noise, and finally the tuning range.

A low cost substrate such as that of a CMOS process is preferred to the expensive and power-hungry substrate that is used for bipolar. The VCO must have a low power consumption for mobile communications. At the same time, the VCO must be linear to avoid distortion of the modulated signal over a given tuning range. The VCO should be immune to substrate noise coupling and provide a low jitter at the output. The phase noise properties of the CMOS VCO are referred to in [34].

VCO on chip

Often, the VCO circuits used at low frequencies are based on modified classic oscillators such as

the Colpitt and Hartley oscillators. The value of the central frequency of the oscillator $\omega_c = \frac{1}{\sqrt{LC}}$ is set by the value of the inductor (L) and the capacitor (C), which is usually a varactor diode. However, the high quality factor (Q) that is necessary to obtain a good phase noise performance is not achievable with on-chip inductors implemented in a CMOS process. Furthermore, this type of resonator requires a large area on the chip and consumes a large amount of power.

The alternative to resonator-based VCOs are ring oscillators VCOs. Ring oscillators do not require any kind of resonator, but their frequency and phase characteristics are not as good as those of resonator-based approaches.

The oscillation frequency of the ring oscillator VCO is $f_c = \frac{1}{2n\tau_d}$ where n is the odd number of inverters in the oscillator, and τ_d is the gate delay per stage. The gate delay in each inverter is tunable, for example, by a control of the capacitive load at the output of the inverter. Thus, we obtain a VCO with a ring of 2k+1 inverters. The analogy between a logic gate and a capacitor indicates that the higher the voltage is, the longer the delay is. The time to accomplish a complete load-unload cycle is proportional to the energy stored. If a capacitor is loaded with a high voltage, the energy ($\frac{1}{2}CV^2$) is stored, and it leads to a high delay to perform the load-unload cycle.

External VCO

Another approach for the development of an integrated PLL is to use a commercial product as an external VCO to provide the voltage to frequency conversion.

4.2.2.4 Reference Signal

The reference signal is chosen with a high spectral purity and a precise value. Frequency synthesizers are not suitable for this type of signal generation due to the high phase noise associated with such circuit. Instead, crystal oscillators are better suited because of their good phase noise properties. These oscillators are external components that are available for frequency references lower than 30MHz. Close to the carrier (<100Hz in cellular applications), the output noise profile is determined mainly by the reference crystal noise [35].

4.2.2.5 Frequency Divider

The frequency division ratio is either fixed or programmable. When the divider is programmable, the frequency division ratio is controlled by an external signal. For a given frequency band to

synthesize, the divider switches between two or more division ratios.

4.2.3 Noise in the PLL

In the PLL, each block contributes to the total phase noise. For example, some noise contributions are provided by the divider, the phase detector, the charge pump, or the digital-to-analog converter. Fractional-N synthesis and delta-sigma modulation are ways to improve several contributions in the PLL.

Usually, phase noise and amplitude noise contributions are not specified separately. Figure 4.6 presents the contributions of different noise sources in a linearized small-signal model of the PLL. The analysis is done with the assumption that the noise sources generated or added in each block are small compared to the useful signal. Each block is decomposed as an ideal functional block plus a noise contribution, which can be placed before or after the ideal block.

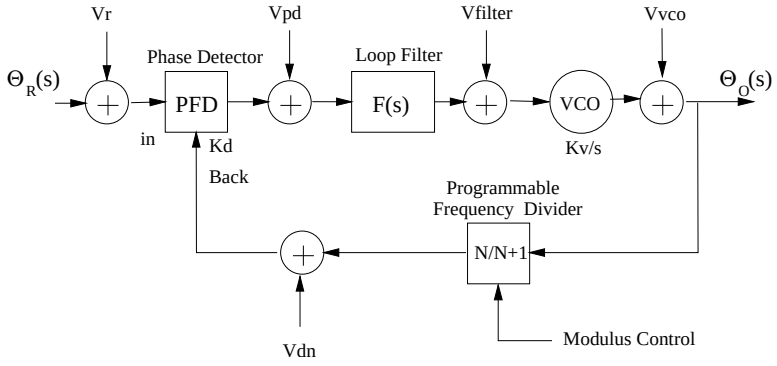


Figure 4.6: Different noise contributors in the PLL

The noise of the reference oscillator is expressed as

$$\Theta_{in} = \Theta_R + V_{ref} \tag{4.10}$$

A quartz is often chosen as a reference signal, since most of the energy is contained in a tiny bandwidth, which is smaller than that in any other type of frequency synthesizer. For the case of the crystal oscillator (quartz), 99.99 percent of the energy is contained in less than a 0.01Hz bandwidth, whereas for a high-quality frequency synthesizer, the same amount of energy is spread in less than 1Hz bandwidth [9].

The output phase noise is given by

$$\Theta_O = V_{vco} + ([(\Theta_{in} - \Theta_{back})K_d + V_{pd}]F(s) + V_{filter})\frac{K_v}{s} \tag{4.11}$$

The feedback phase noise is derived from

$$\Theta_{back} = \frac{\Theta_O}{N} + V_{dn} \tag{4.12}$$

The combination of (4.11) and (4.12) leads to the output phase noise as follows:

$$\begin{aligned}
\Theta_O &= \Big[\Big((\Theta_{in} - \frac{\Theta_O}{N} - V_{dn})K_d + V_{pd}\Big)F(s) \\
&\quad + V_{filter}\Big]\frac{K_v}{s} + \Theta_{vco} \\
&= \Big[\Big((\Theta_{in} - V_{dn} + \frac{V_{pd}}{K_d})F(s) + \frac{V_{filter}}{K_d}\Big)\frac{K_d.K_v}{s} \\
&\quad + \Theta_{vco}\Big]\frac{1}{1 + \frac{K_d.K_v.F(s)}{s.N}} \\
&= \Theta_{vco}\frac{1}{1 + \frac{K_d.K_v.F(s)}{s.N}} \\
&\quad + V_{filter}N\frac{\frac{K_v}{sN}}{1 + \frac{K_d.K_v.F(s)}{s.N}} \\
&\quad + \Big((\Theta_{in} - V_{dn}) + \frac{V_{pd}}{K_d}\Big)N\frac{\frac{K_d.K_v.F(s)}{sN}}{1 + \frac{K_d.K_v.F(s)}{s.N}}.
\end{aligned} \tag{4.13}$$

To simplify 4.13, we introduce the low-pass transfer function H(s) given by

$$\begin{aligned}
H(s) &= \frac{1}{N}\frac{\Theta_O(s)}{\Theta_R(s)}\Big|_{V_{pd}=V_{filter}=V_{dn}=V_{vco}=0} \\
&= \frac{\frac{K_d.F(s).K_v}{sN}}{1 + \frac{K_d.F(s).K_v}{Ns}}
\end{aligned} \tag{4.14}$$

Using the expression of H(s), we can rewrite (4.13) as follows:

$$\begin{aligned}\Theta_O &= \Theta_{vco}[1 - H(s)] \\ &+ V_{filter} N \frac{H(s)}{K_d.F(s)} \\ &+ \Big[(\Theta_{in} - V_{dn}) + \frac{V_{pd}}{K_d}\Big] N.H(s)\end{aligned} \tag{4.15}$$

For low frequencies, $\omega \ll \omega_n$ (i.e $s \to 0$),

$$|H(s)| \approx 1 \;\; and \;\; |1 - H(s)| \approx 0 \tag{4.16}$$

For high frequencies, $\omega \gg \omega_n$ (i.e $s \leftarrow \infty$),

$$|H(s)| \approx 0 \;\; and \;\; |1 - H(s)| \approx 1 \tag{4.17}$$

Consequently, (4.15) can be simplified to the approximations of equations (4.18), and (4.19) In the PLL pass-band $|H(s)| = 1$, the output noise is given by

$$\begin{aligned}\Theta_O &\approx V_{filter} \frac{N}{K_d.F(s)} \\ &+ \Big[(\Theta_{in} - V_{dn}) + \frac{V_{pd}}{K_d}\Big] N\end{aligned} \tag{4.18}$$

while in the PLL stop-band,

$$\Theta_O \approx \Theta_{vco} \tag{4.19}$$

In the PLL stop-band, the PLL output noise is approximated by the noise of the VCO.

Equation (4.20) shows that the contribution from every term is proportional to N^2, where N is the division ratio from the frequency divider. Therefore, it is as important to minimize the noise of each block by using small values of N. If N is a fixed division ratio, the precision or resolution that is required for the synthesized frequency controls the choice of N and f_R. A small reference frequency (f_R) is chosen to obtain a fine frequency resolution, a large value of N is required to obtain the proper output frequency $f_O = N.f_R$. Each increment of N corresponds to a frequency step as that is required to achieve a fine resolution.

For example, if we want to synthesize f_O = 1800MHz with a precision of 1kHz and N fixed,

we need f_R =1kHz and $N = 1800000$. The noise is improved if N is a fractional value, which provides both higher values of f_R and lower values of N for an equivalent precision on the output frequency.

If we assume that the different noise sources are random and uncorrelated, we may sum the respective spectral densities. The output noise spectral density S_{Θ_O}, for a small-signal model within the loop bandwidth, is given by

$$S_{\Theta_O}(f) = S_{V_{filter}}\Big(\frac{N}{K_d.|F(f)|}\Big)^2 + \Big[(S_{\Theta_{in}}(f) + S_{V_{dn}}(f)) + \frac{S_{V_{pd}}(f)}{{K_d}^2}\Big]N^2 \tag{4.20}$$

Outside the loop bandwidth, the output noise spectral density S_{Θ_O}, for a small-signal model, is given by

$$S_{\Theta_O}(f) = S_{\Theta_{vco}}(f) \tag{4.21}$$

In conclusion, it is important to have a low value of N in the loop bandwidth and a low noise contribution from each block (frequency divider, reference signal, filter, phase detector); also, it is necessary to get a low phase noise contribution of the VCO outside the loop bandwidth in order to obtain an overall low output noise spectral density.

4.2.3.1 Noise in the Digital Phase Detector

The noise in the phase detector can be expressed as (4.22) [36].

$$S_{V_{pd}}(f) = K_d^2.\frac{10^{-10.6\pm.3}}{f} \tag{4.22}$$

For the charge pump, the phase noise is approximately $10.log(f_R)$.

4.2.3.2 Noise in the Programmable Frequency Divider

It is more difficult for us to obtain the expression of the noise in the fractional-N divider. Several effects lead to increased noise in the divider.

The fixed-ratio frequency divider yields an ideal noise figure $F = -20.log(N)$. Also, an internal noise contribution is given by the divider and the output noise is

$$\begin{aligned} S_{\Theta_{V_{dn}}}(f) &= \frac{S_{\Theta_{divider_{in}}}(f)}{N^2} + S_{internal} \\ &\approx \frac{S_{\Theta_{divider_{in}}}(f)}{N^2} + \frac{10^{-14.7}}{f} + 10^{-16.5} \end{aligned} \tag{4.23}$$

For fractional-N division, N is not a fixed-ratio. This leads to an additional noise contribution ($S_{N \longleftrightarrow N+1}(f)$), since there is an abrupt phase change each time the dual-modulus divider switches from N to N+1. This can be written as

$$S_{\Theta_{V_{dn}}}(f) = \frac{S_{\Theta_{divider_{in}}}(f)}{N^2} + S_{internal} + S_{N \longleftrightarrow N+1}(f) \tag{4.24}$$

When a third-order delta-sigma modulator is used in a fractional-N frequency synthesizer, $S_{N \longleftrightarrow N+1}(f)$ can be expressed as

$$S_{N \longleftrightarrow N+1}(f) = \frac{(2\pi)^2}{12.f_R} |2.sin\Big(\frac{\pi.f}{f_R}\Big)|^4 \tag{4.25}$$

4.2.3.3 Noise in the Loop Filter

The contribution of the noise source V_{filter} corresponds to the contribution of several factors, including the conversion noise from analog-to-digital converter, and the noise in the filter.

The contribution of the digital-to-analog converter is improved by the introduction of delta-sigma modulation, which allows the quantization noise to be shaped and pushed to higher frequencies. A second-order or third-order analog filter follows the delta-sigma digital-to-analog converter and removes the quantization noise.

The choice of a delta-sigma data-converter is justified only if the noise contribution of a classic digital-to analog-converter is larger than the contribution of the delta-sigma converter and the additional analog filter.

In the case of the passive analog filter, the main sources of noise are the internal noise in the components that is, capacitors and resistors. Certain types of capacitors and resistors can generate substantial $\frac{1}{f}$ noise. If several chips are used to build the PLL, the choice of special technologies such as metal-film type resistors limits the problem. In the system-on-chip approach with a single technology and a restricted number of external components, the analog component

precision is low, and the $\frac{1}{f}$ noise is difficult to improve. It is also difficult to change the filter characteristics, if several standards share the same architecture.

If a digital filter is considered instead, the noise is due to the finite length of the filter coefficients, and is determined by the structure that is chosen. Several standards may share the same filter, provided that the filter coefficients are updated each time the standard is switched.

4.2.3.4 Noise in VCO

There are different types of VCO, where implementation on a chip is possible, that are not equivalent in terms of phase noise performance.

- **LC-Oscillator**

  The LC-oscillator is sensitive to supply noise and substrate noise. The required values for quality factors are difficult to obtain in a monolithic implementation [37]. Indeed, high-quality factor(Q) inductors are not available in CMOS technology.

  The trends in research today of suitable VCO in CMOS technology for an integrated RF front-end are focused today on improved oscillators-based on LC structures.

- **Ring Oscillator**

  In ring oscillators, the fully differential form limits the contribution of external noise such as supply voltage noise, and no external component are needed. However, the internal phase noise remains high.

A complete analysis of a three-stage CMOS ring oscillator is presented in [37]. The linear analysis of the oscillator indicates several sources of noise as follows:

- Additive noise to the output is due to thermal noise current source in the linear model of the oscillator.

- Non-linearities occur in each stage of the ring, when the transistor turns off. The noise components are then multiplied by the frequency carrier or by each other such as in a non-linear frequency-mixer. This is high-frequency multiplicative noise. (Low-frequency multiplicative noise is also added.)

- The periodic switching events and associated bias conditions in the transistors generate a cyclo-stationary noise.
- Finally, the differential structure does not completely suppress the supply and substrate noise, due to, for example, the device mismatches that result from the fabrication process.

Even though this structure generates frequencies suitable for mobile communication, noise in this type of VCO is a major drawback.

As we can see in (4.21), the VCO noise has a major contribution to the overall phase noise in the PLL stop-band and should, therefore, be kept as small as possible.

4.2.3.5 Overall Noise Contribution

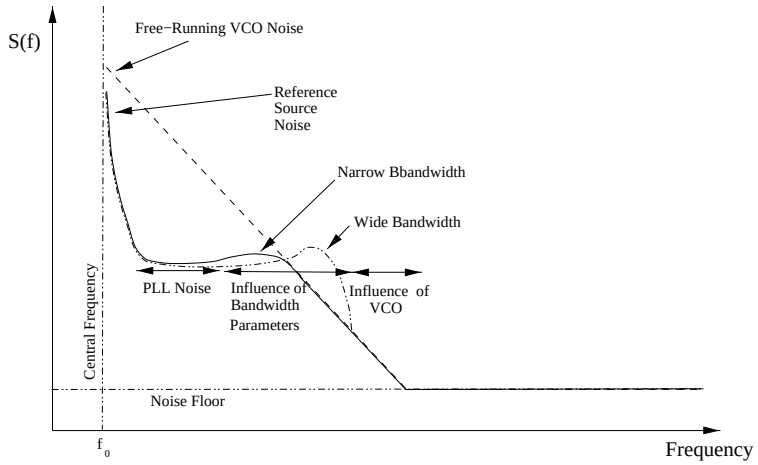


Figure 4.7: PLL phase noise contributors

Figure 4.7 summarizes the contributions of the different terms to the PLL phase noise versus frequency, for a narrow and wide bandwidth filters. Close to the central frequency f_0, the reference source is the main contribution to phase noise, whereas the VCO contribution is dominant outside the loop bandwidth. In between, a region corresponds to the contribution of the PLL noise, where the level of the zone is proportional to N. Then, there is an overshoot, for which the frequency depends on the bandwidth chosen, that is, for a wide bandwidth, the overshoot is placed in a higher frequency than that for a narrow bandwidth, with an increased flat-zone.

4.2.4 Introduction of Modulated Information into the Loop

In telecommunications, the reproduction of a high frequency image of the reference signal is not always the only purpose of the frequency synthesizer. The PLL, described in Section 4.2 generates a stable and adjustable frequency carrier. The VCO output can be used as a local oscillator in the traditional heterodyne structure. Then, a mixer is necessary to add information around this carrier, but non-linearities of the mixing process severely limit the overall performance of the system sometimes.

Alternatively, the output of the VCO is a direct modulated signal around the frequency carrier. The introduction of the modulated information directly in the loop suppresses the need for a mixing stage. The signal can be either introduced as phase modulation or frequency modulation in the loop, as shown in Figure 4.8 [38]. The loop responds to the addition of the modulation by adjusting the VCO phase by $\delta\phi$, as if it was a constant error added to the output of PD.

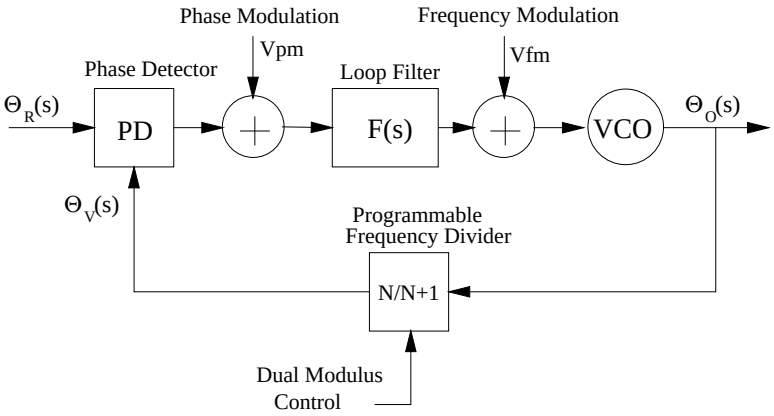


Figure 4.8: PLL modulation

The introduction of the modulating signal before (Phase Modulation) or after (Frequency Modulation) the loop does not have the same effect on the system response. The phase modulation is filtered by the loop filter, and the loop follows the phase deviation $\delta\phi = \frac{NV_{pm}}{K_d}$ before the loop's natural frequency. The transfer function $\frac{\Theta_O}{V_{pm}}$ is a low-pass characteristic, as follows:

$$\begin{aligned}\frac{\Theta_O}{V_{pm}} &= \frac{\frac{F(s).K_v}{s}}{1+\frac{K_d.F(s).K_v}{Ns}} \\ &= \frac{H_{closed\ loop}(s)}{K_d}\end{aligned} \tag{4.26}$$

This type of modulation can be used when the information frequency is below $2\omega_n$ [38].

If the loop is sufficiently slow, the frequency modulation, which is added after the filter directly modulates the VCO. This occurs because the loop is not able to compensate for the error introduced by the modulation. The transfer function $\frac{\omega_O}{V_{fm}}$ is a high-pass characteristic,

$$\begin{aligned}\frac{\omega_O}{V_{fm}} &= \frac{K_v}{1+\frac{K_d.F(s).K_v}{Ns}} \\ &= K_v\Big(1-\frac{H_{closed\ loop}(s)}{N}\Big)\end{aligned} \tag{4.27}$$

This type of modulation can be used when the information frequency is above the natural frequency ω_n [38]. If the information can not be modulated over the desired frequency range, alternatives such as compensation filters or two-point modulation can be used [38].

The compensation filter extends the pass band zone of the loop filter. For example, the compensation filter for the high-pass transfer function from (4.27) is an amplifier with a cut-off frequency which closely matches that of the loop. The PLL loop is modified so that all the modulated information is transmitted. The compensation filter approach has several limitations. If the information bandwidth is wide (over a decade, for example), the strong amplification required to compensate for the low-pass characteristic of the PLL leads to high signal levels at the input of the loop filter. Moreover, a strong amplification implies increased distortion problems and associated noise problems [38].

The other alternative to introduce information in the closed-loop is the two-point modulation, and then no compensation filter is needed. Both the entry point for the phase modulation, and the entry point for the frequency modulation are used. This takes advantage of the relation between the phase and the frequency. Indeed, in a phase modulation, the instantaneous phase θ of a modulated carrier is expressed by $\theta(t) = \omega_{carrier}t + KV_{pm}(t)$ and the instantaneous frequency is

given by $\omega(t) = \omega_{carrier} + K\frac{dV_{pm}(t)}{dt}$. In a frequency modulation, $\omega(t) = \omega_{carrier} + KV_{fm}(t)$ yields the instantaneous frequency. Comparison of the two expressions of the instantaneous frequency leads to

$$V_{fm}(t) = \frac{dV_{pm}(t)}{dt} \tag{4.28}$$

An example of frequency modulation using two points modulation is displayed in Figure 4.9.

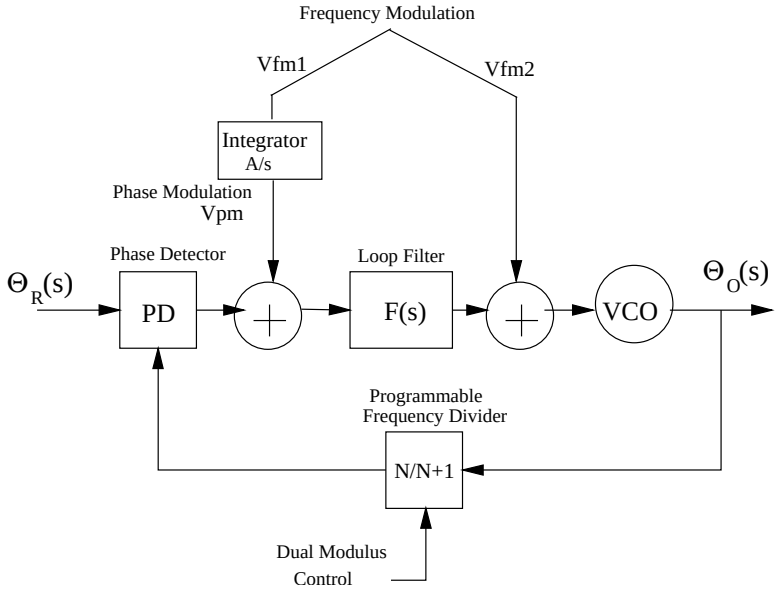


Figure 4.9: Two-point modulation

The integrator converts the frequency modulation into a phase modulation. One frequency is introduced in the loop before the loop filter as a phase modulation, while the other frequency is inserted in the loop as a frequency modulation.

If we note that $\omega_{out}(s) = s.\theta_{out}(s)$, and if we choose $A = \frac{Kd.Kv}{N}$ in Figure 4.9, the output $\omega_{out}(s)$ is then

$$\begin{aligned}\omega_{out}(s) &= f_{m1}\frac{A.H_{closed\,loop}(s)}{K_d} + f_{m2}[1 - \frac{H_{closed\,loop}(s)}{N}]K_v \\ &= \Big(f_{m1}\Big[\frac{H_{closed\,loop}(s)}{N}\Big] + f_{m2}\Big[1 - \frac{H_{closed\,loop}(s)}{N}\Big]\Big)K_v\end{aligned} \tag{4.29}$$

which is simplified when $f_{m1} = f_{m2} = f_m$ so that $\omega_O = K_v.f_m$. In this case, the information

is not modified by the loop characteristics.

In practice, the integrator is not ideal and has a finite gain at DC, which implies that the cancellation of the low frequency components of the signal has been imperfect.

If a phase modulation is introduced in the loop with a double point insertion instead of the frequency modulation, a differentiator stage will be inserted before the entry point for frequency modulation, while the entry point for the phase modulation will be directly available.

4.3 Fractional-N Synthesis

4.3.1 Principle of Fractional-N Synthesis

Fractional frequency synthesis does not require more current, complexity or bigger dies [39]. In fractional-N synthesis, the reference frequency f_R is many times the step frequency f_{step}, and the output frequency of the PLL, f_O is given by

$$f_O = f_R(N\frac{K}{F}) \tag{4.30}$$

where F is the fractionality, and K is the product between the phase detector constant and the VCO constant in the PLL linear model.

Let us consider the following example to see the difference between the traditional approach and the fractional-N frequency synthesis.

If we assume $f_R = f_{step} = 30$kHz, and we have a 32/33 divider. To generate a $f_O = 912$MHz, with this fixed step, we obtain

$$\begin{aligned} N &= \frac{f_O}{f_{step}} \\ &= \frac{912MHz}{30kHz} \\ &= 30400 \end{aligned} \tag{4.31}$$

This value of N is obtained when the divider is set to divide 950 times by 32 and 0 times by 33 (N=32*950+33*0=30400). To increase the output frequency by one frequency step (f_O =912.03MHz), the divider is reset to N=32*949+33*1=30401.

If we now choose f_R = 480kHz > f_{step} , while we keep $f_{step} = \frac{f_R}{F}$ = 30kHz, then the total division ratio is given by

$$\begin{aligned} N &= \frac{f_O}{f_R} \\ &= \frac{912MHz}{480kHz} \\ &= 1900 \\ &= 47 * 32 + 12 * 33 \end{aligned} \tag{4.32}$$

To obtain f_O =912.03MHz, the counter cannot increment N by one, since it corresponds to an incorrect frequency step (f_O = 912.48MHz, instead of f_O =912.03MHz). The output of the VCO can only be in two states, but the loop filter averaging (over F cycles) generates the proper fractional value, because the loop is not wide [9]. The average frequency for F=16, is

$$\begin{aligned} f_{average} &= f_R \frac{(N * (F-1) + (N+1) * 1)}{F} \\ &= 0.48MHz * \frac{1900 * 15 + 1901 * 1)}{16} \\ &= 912.03MHz \end{aligned} \tag{4.33}$$

In our example, the change between N integer and N fractional leads to a diminution of N by F (N = 1900 = $\frac{f_O}{f_R} = \frac{F * f_O}{f_R}$, instead of $\frac{f_O}{f_{step}}$ = 30400). Theoretically, the phase noise is improved by $20 * log(F)$. But in practice, improvement is limited by the additional narrow filtering that is needed, and the phase noise contribution of the PFD noise which increases as $20 * log(f_R)$ [35]. Residual noise at low frequencies increases the need for a narrow filter ($\frac{f_R}{100}$ or lower) [9].

To extend (4.33) to a more general case, the average frequency division ratio in the dual modulus frequency divider by $N/N+1$ is

$$\begin{aligned} N_{fractional} &= \frac{(N * (F-K) + (N+1) * K)}{F} \\ &= N + \frac{K}{F} \end{aligned} \tag{4.34}$$

with $F \geq K \geq 0$.

To obtain a given frequency divider ratio, we set the frequency modulus divider to $N/N+1$ for the integer part; then we set the modulus control to $\frac{k}{F}$ (k division by N+1 and division by N otherwise).

4.3.2 Implementation of FN Synthesizers

Let us consider a given frequency dual-modulus divider by $N/N+1$. The fractional part $\frac{K}{F}$ is obtained with a digital accumulator of size F, clocked at the frequency of the reference signal f_R.

The digital accumulator is made of an adder (X+Y) and a latch. The output (X+Y) of the adder is latched, and fed as an input to the adder (i.e., Y). The other input X of the adder contains the data to be accumulated. When the total (X+Y) exceeds the maximum size of the adder, an overflow is produced.

If K = 0, no overflow occurs, whereas if K = F, overflow occurs every clock cycle. In general, the average frequency of overflow may be written as $\frac{K}{F} * f_{clk}$.

During $\frac{k}{f_{clk}}$, the division ratio is set to N+1, but it is set to N during $\frac{F-K}{f_{clk}}$. Therefore, the average division ratio is available after $\frac{F}{fclk}$. For example, if $F = 2^7 = 128$ and $f_R = 20$MHz, the complete cycle will last $\frac{128}{20MHz} = 6.4\mu s$.

In the first implementation of FN synthesis used by Hewlett-Packard in the eighties, the overflow of the accumulator directly modulated the division ratio by the modulus control, as shown in Figure 4.10.

The main problem of this implementation is the phase perturbation that is introduced by the programmable frequency divider, when N is switched to N+1. These perturbations lead to spurious signals at the output of the VCO. The spurs are multiples of F_j , as defined in

$$F_j = \frac{F_{clk}}{F} * D \tag{4.35}$$

where D is the highest common divider between K and F.

The peak phase deviation at the VCO when N changes to N+1 is 2π radians. At the phase detector, this is equivalent to a peak of $\frac{2\pi}{N}$, represented in Figure 4.11.

Since this phase perturbation is entirely predictable, the first solution proposed for this problem was a FN synthesizer with analog compensation.

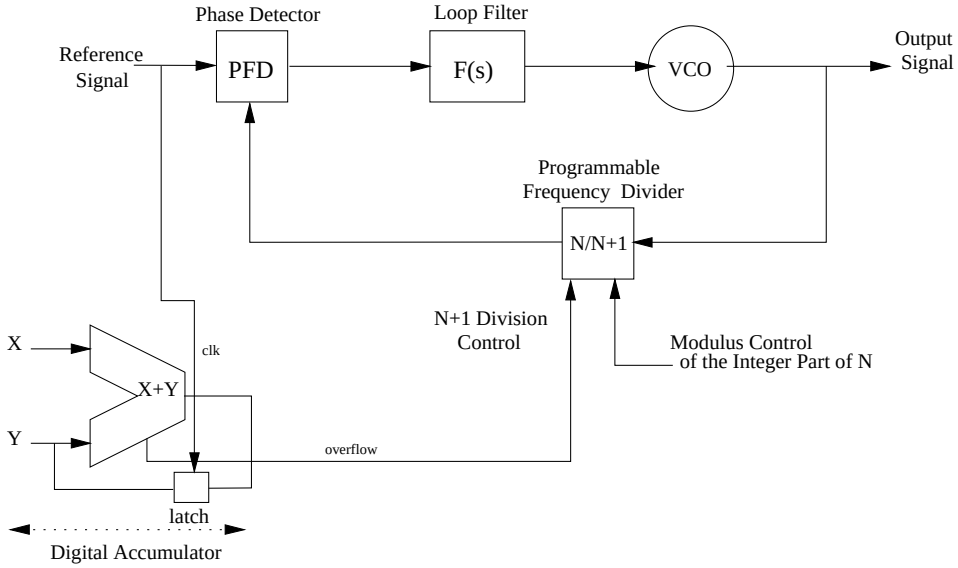


Figure 4.10: FN implementation with digital accumulator

4.3.2.1 FN Synthesizer with Analog Compensation

Figure 4.12 depicts the FN frequency synthesizer with analog compensation. The accumulation of the phase of the fractional part of N is subtracted from the output of the phase detector with an analog signal. If the two signals match, the analog signal cancels the phase error signal. The output spurious signal, due to fractional synthesis, is reduced [11]. This implementation is widely used in the fractional-N frequency synthesizers available in today's market.

The precision of the compensation directly depends on the DAC accuracy, and the sensitivity

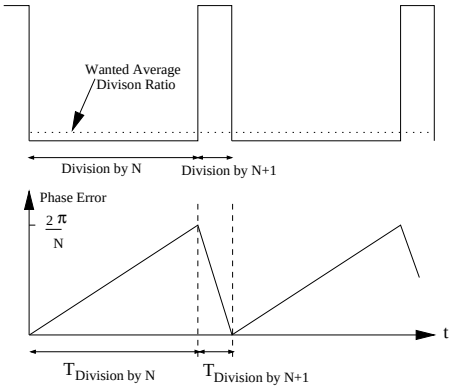


Figure 4.11: Sawtooth phase error of conventional FN synthesizer

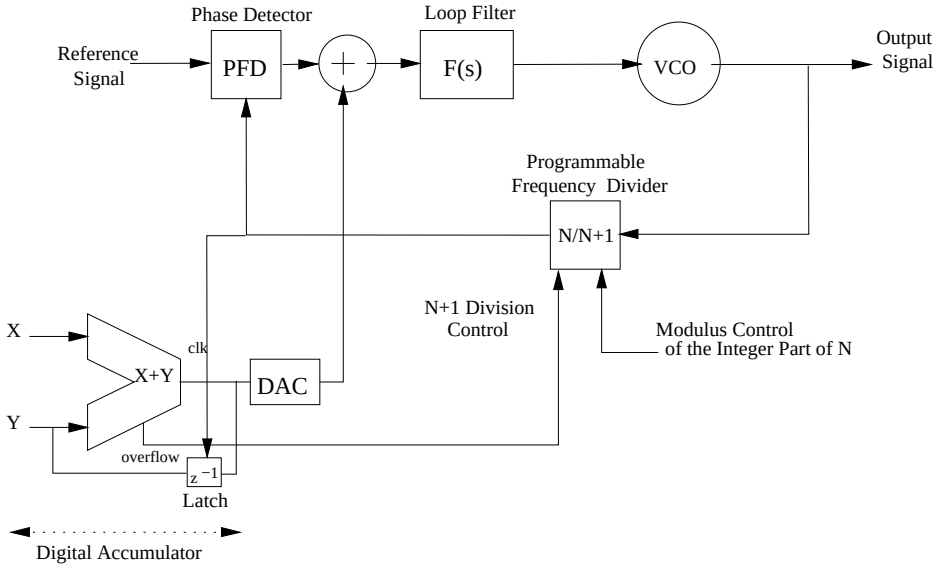


Figure 4.12: FN Synthesizer with analog compensation

of analog components. Even if the system is well compensated for the phase error during the production phase of the design, the compensation does not remain accurate as the characteristics of the analog components are altered by such factors as aging, and temperature. For all of these reasons, a spurious rejection is limited to 35 to 45 dB in ASICs [9].

Consequently, another solution was then proposed to implement the fractional-N frequency synthesizer, based on delta-sigma modulation.

4.3.2.2 FN with Multi-Stages Delta-Sigma Modulation

In the FN synthesizer from Figure 4.10, a switch of the division ratio from N to (N+1) occurs only K times over F cycles. This is a low-frequency switching to reach the wanted phase.

However, if the switching frequency is increased, and the ratio of division by (N+1) remains the same during F cycles, the phase noise is moved to higher frequencies, where it is filtered by the loop. Only some residual noise remains at low frequencies, but the overall phase noise of the PLL is improved.

The system modifies the pattern to minimize the low-frequency spectral content of the phase noise due to the switching of the division ratio, rather than trying to cancel the phase error. This can be obtained by a noise-shaping technique called delta-sigma modulation [4], [40], which

has been introduced in Chapter 3. The switching frequency is increased, while the target phase remains unchanged.

Delta-Sigma Modulation

In an analog-to-digital converter, the analog input is fed to an integrator, followed by a quantizer that works at a high sampling frequency compared to the Nyquist frequency. A negative feedback loop, placed after the quantizer, is also applied to the input of the integrator. In our case, the input (x) is a digital word, representing the desired fractional value to synthesize; therefore, we consider a digital delta-sigma modulator equivalent to the analog delta-sigma modulator. An example of a first-order digital delta-sigma modulator is depicted in Figure 4.13.

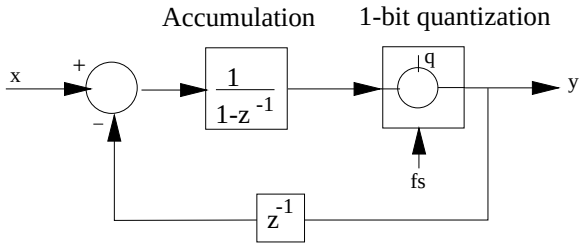


Figure 4.13: First-order delta-sigma modulator

The delta-sigma modulator filters the quantization noise (q) differently from the input signal (x), as illustrated by 4.37 for a first-order delta-sigma modulator.

We first define the integrator transfer function (H_{int}) as

$$H_{int} = \frac{1}{1 - z^{-1}} \tag{4.36}$$

The expression of the output of the delta-sigma modulator (y) is given by

$$\begin{aligned} Y(z) &= \frac{H_{int}}{1 + z^{-1}H_{int}}X(z) + \frac{1}{1 + z^{-1}H_{int}}Q(z) \\ &= X(z) + (1 - z^{-1})Q(z) \\ &= X(z) + H_{noise}(z)Q(z) \end{aligned} \tag{4.37}$$

The expression of the modulus of $H_{noise}(f)$ is written in the frequency domain to obtain the expression of the noise shaping action by the DSM as follows:

$$
\begin{aligned}
|H_{noise}(f)| &= |1 - z^{-1}| \\
&= |1 - e^{\frac{-2j\pi f}{f_R}}| \\
&= \left|2sin\Big(\frac{\pi f}{f_R}\Big)\right| \text{ for } \frac{f_R}{2} \geq f \geq 0
\end{aligned}
\tag{4.38}
$$

with $f_R = f_s$, which is the sampling frequency.

$|H_{noise}(f)|$ is proportional to a sinusoid in the range $\frac{f_s}{2} \geq f \geq 0$: At low frequencies, $|H_{noise}(f)|$ approaches zero as $|H_{noise}(f)| \rightarrow \frac{2\pi f}{f_s}$, while at frequencies near $\frac{f_s}{2}$, $|H_{noise}(f)|$ approaches a maximum of two.

Higher-order delta-sigma modulators improve the noise shaping characteristic $|H_{noise}(f)|$. However, higher-order modulators with several feedbacks are not always stable, but this problem is overcome in the structure referred to as MASH [17] and is discussed in Section 3.3.4, where a cascade of first-order modulators is used to progressively shape the input to a high degree.

The MASH 1-1-1 architecture is shown in Figure 3.15 with the output expression given by (3.31). We will repeat them here for convenience in Figure 4.14 and (4.39), respectively.

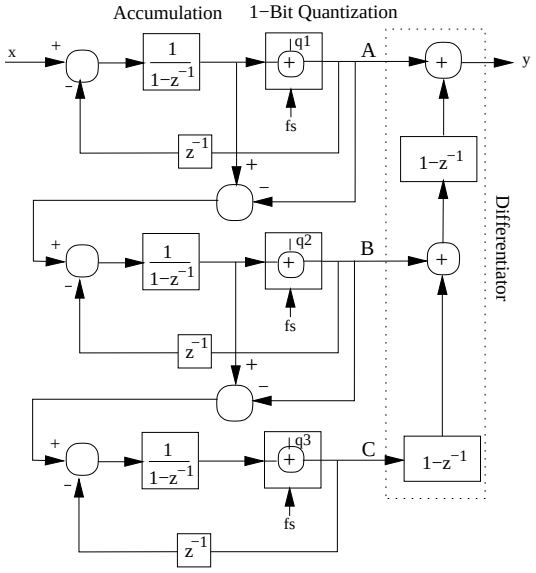


Figure 4.14: MASH 1-1-1 architecture

$$\begin{aligned} Y(z) &= A + B(1-z^{-1}) + C(1-z^{-1})^2 \\ &= X(z) + Q_1(z)(1-z^{-1}) \\ &+ (-Q_1 + Q_2(z)(1-z^{-1}))(1-z^{-1}) \\ &+ (-Q_2 + Q_3(z)(1-z^{-1}))(1-z^{-1})^2 \\ &= X(z) + (1-z^{-1})^3 Q_3(z) \\ &= X(z) + H_{noise}(z)Q(z) \end{aligned} \tag{4.39}$$

Thus, we can deduce the frequency noise that is introduced by the fractional division, when the MASH 1-1-1 controls the division ratio by (N/N+1) with $x = \frac{k}{F}$. Indeed, $f_{vco} = (N_{integer} + N_{fractional})f_R = N.f_R + (\frac{k}{F} + H_{noise}(f)Q_3(f))f_R$. From this equation, the constant term $N.f_R + \frac{k}{F}.f_R$ is removed, and the term $f_{noise}(f) = H_{noise}(f).Q_3(f).f_R$ remains, which is the expression of the frequency noise introduced by fractional-N frequency synthesis.

Now, let us assume the quantization q_3 is uncorrelated with x. Furthermore, if q_3 is assumed to be a uniformly distributed white-noise sequence, the mean of q_3 is zero, and the variance is $\sigma^2_{q_3} = \frac{\Delta}{12}$, with $\Delta = 1$ [25]. As the power is spread over the bandwidth f_R, the power spectral density (PSD) of the quantization error q_3 is $\frac{\sigma^2_{q_3}}{f_R} = \frac{1}{12.f_R}$. This enables us to write the expression of the frequency fluctuation $f_{noise}(z)$ as $S_{f_{noise}} = |H_{noise}(f).f_R|^2.\frac{1}{12.f_R} = \frac{|1-z^-1|^6.f_R}{12}$.

In terms of noise contribution, the expression of the phase noise is more relevant than the frequency noise expression. Phase and frequency are related by an integration, as $\Theta = \int 2.\pi.f_{instantaneous}dt$ [11], which leads to

$$\begin{aligned} S_{N\longleftrightarrow N+1}(z) &= S_{f_{noise}}.S_{integration} \\ &= \frac{|1-z^{-1}|^6.f_R}{12}.\frac{(2\pi)^2}{|1-z^{-1}|^2.f_R} \\ &= \frac{(2\pi)^2}{12.f_R}|1-z^{-1}|^4 \ \frac{rad^2}{Hz} \end{aligned} \tag{4.40}$$

By replacing z by $e^{\frac{2j\pi f}{f_R}}$ in (4.40), we obtain

$$S_{N\longleftrightarrow N+1}(f) = \frac{(2\pi)^2}{12.f_R}|2.sin\Big(\frac{\pi.f}{f_R}\Big)|^4 \tag{4.41}$$

The transition from the output of the MASH 1-1-1 (4.39) to the phase noise contribution (4.40) is generalized to an n-order DSM output,

$$\begin{aligned} Y(z) &= X(z) + (1-z^{-1})^n Q_n(z) \\ &= X(z) + H_{noise}(z)Q(z) \end{aligned} \tag{4.42}$$

and results in the following phase noise contribution:

$$S_{N\longleftrightarrow N+1}(f) = \frac{(2\pi)^2}{12.f_R}|2.sin\Big(\frac{\pi.f}{f_R}\Big)|^{2(n-1)} \tag{4.43}$$

When $f \ll f_R$, then (4.43) may be approximated by

$$S_{N\longleftrightarrow N+1}(f) \approx \frac{(2\pi)^2}{12.f_R}|2.\pi\Big(\frac{f}{f_R}\Big)|^{2(n-1)} \tag{4.44}$$

When a MASH structure controls the fractional frequency division, the quantization noise is shaped, as shown by (4.44). Higher frequency components are then removed by the low-pass characteristics of the PLL, and thus, the level of spurs is reduced.

A digital accumulator is a compact realization of a DSM [11]. The output of the accumulator is delayed by a latch, and fed back to the input of the accumulator as in a delta-sigma modulator. The overflow is a 2-level signal corresponding to the quantized output of the modulator. Figure 4.15 illustrates an example of FN synthesizer with a MASH 1-1-1 structure.

The degree of noise shaping is directly related to the order of the delta-sigma modulator that is used. In practical designs, three or four accumulators should be sufficient to eliminate the spurious signals. It is advised in [9] to keep the ratio between the loop bandwidth and the sampling greater than 100:1, for an improved filtering of residual noise at low frequencies.

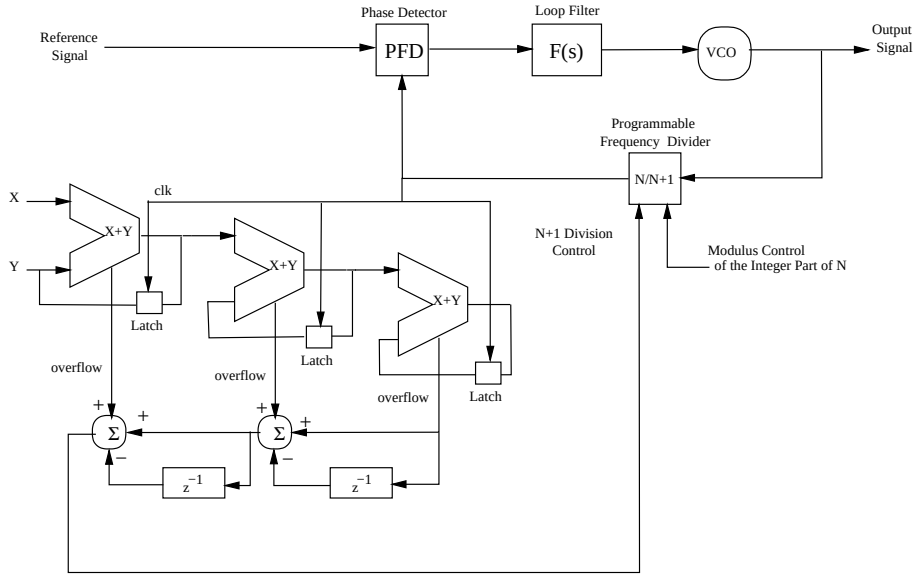


Figure 4.15: FN synthesizer with a MASH 1-1-1 implementation

4.4 Conclusion

In this chapter, the closed loop equation of the PLL was derived. The PLL parameters such as the natural frequency and the damping coefficient were detailed. Also, we described various PLL loop blocks. The fractional-N frequency synthesizers, and the concept of fractionality were introduced with a discussion of early and current implementation methods. The phase noise and the contribution of different blocks were given, and the governing equations were derived. The phase noise contribution of MASH 1-1-1 architecture was derived and extended to an n-order MASH architecture. In the next chapter, we will implement a new MASH 1-1-1 architecture, which is flexible enough to facilitate the study of the delta-sigma order effect on the fractional-N frequency synthesizer. Also, the architecture has a bypass mode to ease the study of more delta-sigma implementations, which have been developed in this research work.

Chapter 5

MASH Delta-Sigma Fractional-N PLL

5.1 Introduction

Frequency synthesizers are widely used as local oscillators for frequency translation in wireless communications. The principal limitation of an integer-N frequency synthesizer is that its frequency resolution is equal to the PLL reference frequency. The Fractional-N approach eliminates this limitation, but the fractional spur is a concern. Delta-sigma noise shaping techniques are applied to fractional-N synthesis to achieve an arbitrary fine resolution, and to enhance the phase noise properties of the synthesizer.

As we discussed in Chapter 4, digital delta-sigma modulation techniques can be applied to fractional-N PLLs in order to digitally compensate for fractional spurs. The advantage of this technique over analog compensation is that it avoids the maximum fractional spur reduction limitation due to device mismatch.

In this chapter, an implementation of a MASH delta-sigma PLL that was discussed in Chapter 4 is explained. The GPRS wireless data communication standard is targeted. First, architecture parameters are adjusted to meet the specification requirements. Then, the circuit implementation of the PLL components is detailed. Finally, the performance of this design is evaluated through a test chip. The developed chip will be used later to validate and characterize the new architectures in Chapter 6.

5.2 Architecture

As stated in Chapter 4, limitations of analog compensated fractional-N PLLs include limited spur reduction and limited resolution. These two factors lead to limitations in lock time, and the spectral purity performance of the synthesizer. One alternative to this architecture is to provide a digital solution to eliminate spurs found in fractional-N PLLs. A digital delta-sigma modulator may be used to accomplish this.

The delta-sigma PLL using MASH 1-1-1 architecture that is based on digital accumulators is represented in Figure 5.1. The operation of the MASH 1-1-1 architecture is very simple. The overflow from the accumulator is one bit, that is, either zero or one, and so the noise cancellation logic has a low complexity. The output has eight-levels and spreads from -3 to 4 with an average between zero and one. The stable input range normalized to the modulus is from zero to one. It is inherently stable, and this topology is suitable for the pipeline operation to achieve high clock frequencies.

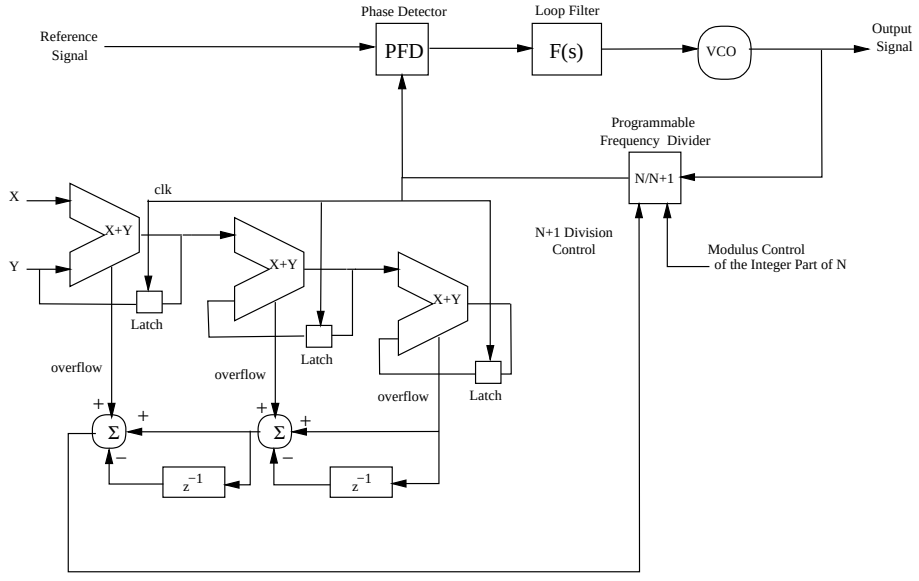


Figure 5.1: FN frequency synthesizer using MASH 1-1-1 with digital accumulators

In this work, a programmable digital MASH delta-sigma modulator is introduced, as shown in Figure 5.2, to replace the regular MASH 1-1-1 in Figure 5.1. The key difference between the regular MASH 1-1-1 and the proposed architecture is in the programmability to change the order of the modulator using control bits denoted by "CTL".

The "CTL" control bits determine whether a first, second, or third-order delta-sigma modulator is chosen. Another important feature of this structure is the external bypass mode. In this mode, the whole modulator can be bypassed, and an external control signal can be supplied externally. This mode will be very important to test and characterize the new architectures that will be proposed in Chapter 6. The datapath width of the modulator is set to 24-bit to achieve a high frequency resolution at high reference frequencies (around 10MHz to 50MHz).

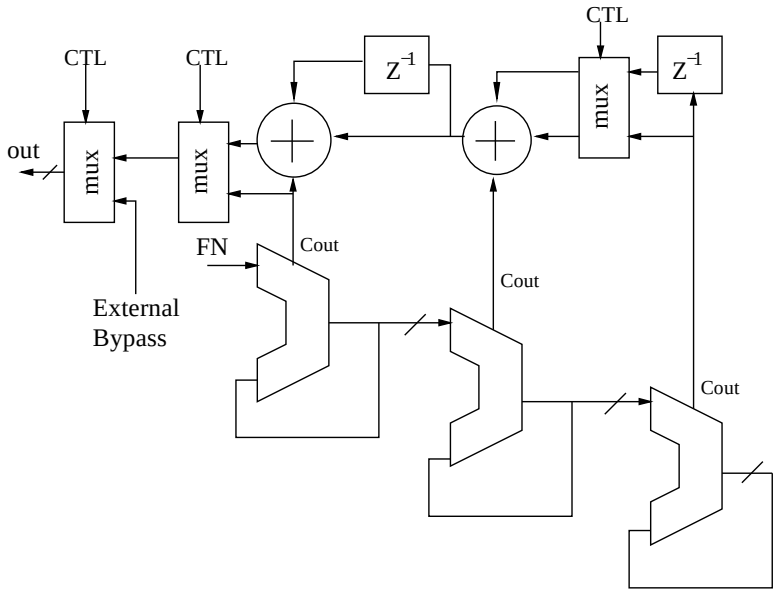


Figure 5.2: A programmable MASH delta-sigma modulator

5.3 Architecture Implementation

The GSM and GPRS standards are targeted when determining the optimal parameters of the delta-sigma modulator. On one hand, maximum spur suppression is required. On the other hand, the quantization noise has to be suppressed sufficiently at high frequencies in order to meet the phase noise specifications at high frequency offsets. A reference frequency of 13MHz is specified for the GSM/GPRS standards [41]. This sets f_R for the modulator to be 2^i.13MHz where i is either positive or negative. For simplicity, only 6.5MHz and 13MHz reference frequencies are considered. For sufficient spur suppression, it has been assumed that the closed loop PLL response is one order higher than that of the delta-sigma modulator.

The delta-sigma PLL architecture, described in Section 5.2, has been implemented in a 0.35 μm BiCMOS technology. The chip pin layout is shown in Figure 5.3, and the corresponding terminal functions are listed in Table 5.3. All the loop components have been included on chip, except for the VCO and loop filter. The PLL operated from a 3.3V supply voltage. A close-in phase noise of -80dBc/Hz was targeted. This specification is well below that of most wireless standards.

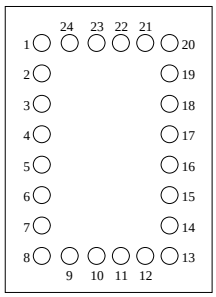


Figure 5.3: Chip pin layout

5.3.1 Low-Pass Filter Parameters

The choice of the closed loop bandwidth plays an important role in the PLL performance. A smaller bandwidth means a better phase noise (out of band), but at the expense of a higher lock time. With a closed loop bandwidth of 30KHz, the necessary loop filter parameters may be computed in order to meet the lock time specification of 200 μs.

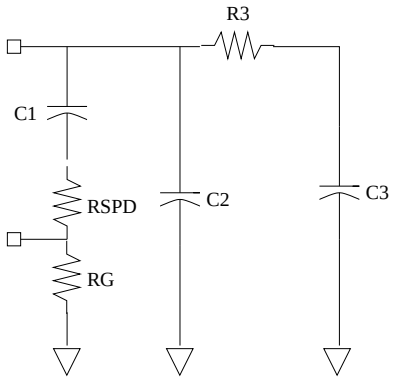


Figure 5.4: PLL loop filter

Figure 5.4 depicts the PLL loop filter schematic, and Table 5.2 indicates the loop component

Pin No.	Symbol	Function	Description
1	GCPM	–	Main Charge Pump Ground
2	PHP	O	Main Charge Pump Output
3	VCPM	I	Main Charge Pump DC Supply
4	GPSM	–	Main Prescaler Ground
5	RFMN	I	Main Channel RF Input (Differential +)
6	/RFMN	I	Main Channel RF Input (Differential -)
7	VPSM	I	Main Prescaler DC Supply
8	STRB	I	Serial Interface Strobe
9	DATA	I	Serial Interface Data
10	CLK	I	Serial Interface Clock
11	GDIG	–	Digital Ground
12	LDET	O	Lock Detect Output
13	VDIG	I	Digital DC Supply
14	GREF	-	Reference Buffer Ground
15	REFI	I	Reference Buffer Input
16	SD_BIT0	I	ΣΔBypass Input bit 0
17	SD_BIT1	I	ΣΔBypass Input bit 1
18	VCXO	I	Main Reference Buffer DC Supply
19	VDD_SD	I	ΣΔDC Supply
20	SD_OUT2	O	ΣΔOutput Bit 2
21	SD_OUT1	O	ΣΔOutput Bit 1
22	SD_BIT2	I	ΣΔBypass Input bit 2
23	RSET	–	Charge Pump Current Setting Resistor
24	SWM	O	Speedup Switch – Main

Table 5.1: Chip pins description

values that are necessary in order to meet the specification. Figure 5.5 shows the lock time simulation of the delta-sigma PLL using the calculated filter parameters. A two-mode fast lock technique [42] was used.

The two-mode pull-in technique is based on varying the damping factor of the PLL using two methods:

- the switching of the loop filter
- the switching of the loop gain

In the first method, a loop filter with a large bandwidth is used during the acquisition process, and then switched to a narrow bandwidth after the lock is achieved. This method requires a lock

detector to control the switch. The second method employs two charge pump circuits to provide a high-gain mode for a fast phase acquisition, and a low-gain mode for phase tracking after the synchronization is achieved. The charge pump speedup current is chosen to be 1.6mA, and a switch is used to change the resistor value from 1734Ω to 613Ω. The switch time was set to 40 μs. The settling time was 95 μs for the PLL to settle within 90Hz.

Component	Value
RSPD	613 Ω
RG	1121 Ω
C1	7.38nF
C2	1.24nF
R3	195 Ω
C3	124pF

Table 5.2: Loop filter component values

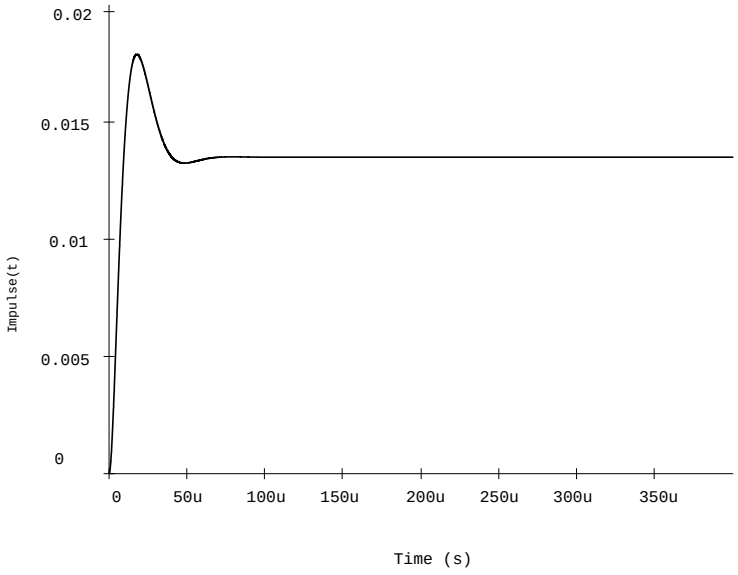


Figure 5.5: PLL lock time simulation

5.3.2 Frequency Divider Design

The frequency divider is the most complicated portion of the fractional-N PLL. As Figure 5.6 indicates, the divider consists of a high-speed dual-modulus prescaler [43], and two programmable counters [44]. The advantage of this architecture is that only a small portion of the divider, the

prescaler, needs to work at the VCO frequency. This is important for reducing power consumption.

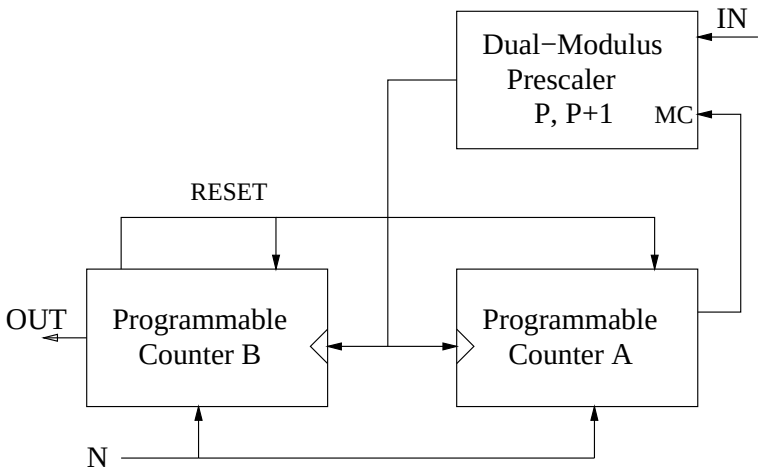


Figure 5.6: PLL divider architecture

A description of the overall operation of the divider is as follows. Initially, counters A and B are loaded with their respective values. The size of counter B is assumed to be larger than that of A. The prescaler division ratio is initially set to $P + 1$. When counter A completes, it sends its complete signal to the dual modulus prescaler to change its division ratio from $P + 1$ to P. At this time instant, the total division ratio is $A(P + 1)$, where A is the value loaded into the A counter. The B counter continues for more cycles. When the B counter completes counting, its completion signal resets both A and B counters, and the process repeats. At this time instant, the counters will have counted an additional $(B - A).P$ VCO cycles. Therefore, the total division ratio is

$$N = (B - A)P + A(P + 1) = BP + A \tag{5.1}$$

We should note that for correct frequency division, several conditions must be met. First, the value that is loaded into the B counter must be greater than that of the A counter. In the case of the fractional-N divider with delta-sigma modulation technique, a negative value may be added to N. Then, the minimum value for B becomes $B > A + k$ where k is the maximum negative value, produced by the delta-sigma modulator. Secondly, the value loaded into the B counter

must also be greater than P, and the value loaded into the A counter cannot exceed P. These two conditions are necessary in order to guarantee a contiguous division range. These constraints give rise to a minimum division ratio given by

$$N_{min} = P.(P-1) \tag{5.2}$$

Since the dual-modulus prescaler runs at the VCO frequency, its size must be limited in order to reduce its power dissipation. Since the voltage swing of the VCO is small, the input sensitivity of the prescaler is also a concern. In order to satisfy these two constraints, the flip-flop gates used in the prescaler are designed by using bipolar ECL logic with a 250mV swing. An input buffer is designed to work with -20dBm input power levels. The currents in the ECL gates are used to meet the required voltage swing, and the phase noise specification of -90dBc/Hz (measured at the output). In order to enable two reference frequencies of 6.5MHz and 13MHz, and for possible multi-standard operation, a dual-modulus prescaler of 8/9 and 16/17 was implemented (Figure 5.7). The SEL control signal selects either an 8/9 dual-modulus division ratio or a 16/17 dual-modulus division ratio. The MC signal selects either an even division ratio, or an odd division ratio. Table 5.3 shows the truth table for the division ratio of the prescaler. The top portion of Figure 5.7 is a divide by 4/5 synchronous counter. The bottom portion, called the extender, uses the divide by 4/5 counter to produce a total division ratio of either 8/9 or 16/17.

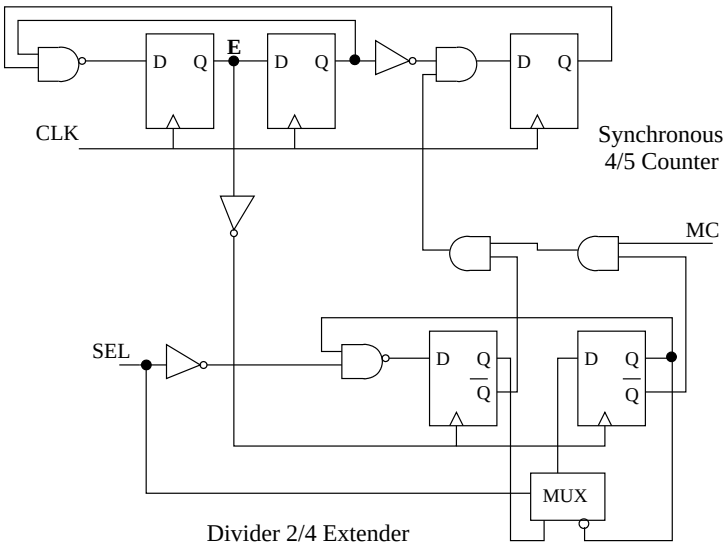


Figure 5.7: Dual-modulus prescaler

SEL	MC	Division Ratio
0	0	16
0	1	17
1	0	8
1	1	9

Table 5.3: Dual-modulus prescaler truth table

Prescaler Division	Reference Division	F_{min}	F_{max}
8/9	1	728MHz	>1.2GHz
	2	364MHz	>1.2GHz
	4	128MHz	>1.2GHz
16/17	1	Out of Range	
	2	Out of Range	
	4	780MHz	>1.2GHz

Table 5.4: Design frequency plan

The rest of the divider is implemented in CMOS with a standard cell library. In order to cover an output frequency of around 1GHz, the sizes of the B and A counters were 6-bit and 3-bit, respectively. This yields a frequency division ratio of 56 to 519. Table 5.4 shows the frequency plan of the design. It is note worthy that 1.2GHz is the maximum operating frequency of the prescaler, which is limited by the critical path of the divider.

An ECL to CMOS level converter is necessary to provide an interface between the prescaler and the rest of the divider. Figure 5.8 demonstrates a circuit schematic of the level converter used. The level converter is designed to give a reasonable tradeoff between delay, power, and phase noise.

The critical path of the divider, depicted in Figure 5.9, is an issue. This critical path sets the maximum frequency of the divider, and hence, the PLL's maximum operating frequency. The critical path begins with a $0 \rightarrow 1$ transition at node E in the prescaler (see Figure 5.7). This signal must propagate all the way to the output of the prescaler, which is connected to the clock input signal, and then to the counters. The delay in the counters includes both the setup time of the flip-flops used in the counters, and the delay in the logic associated with the counters. Then, the output of the A counter toggles, and changes the value of the MC input to the prescaler. Next, The MC input must propagate through 3 ECL AND/NAND gates and one flip-flop. The

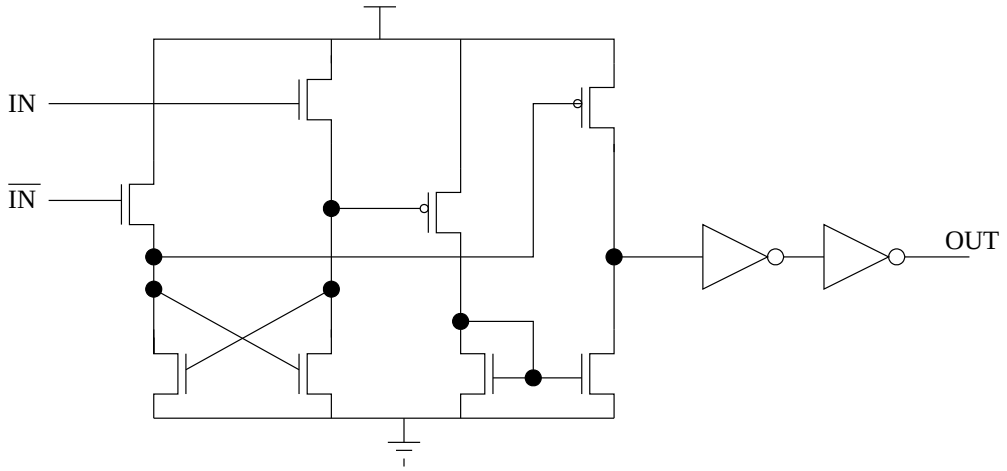


Figure 5.8: ECL to CMOS level converter

measurement of the worst case critical path is 6.78ns. We note that the critical path occurs only when the prescaler is dividing by 9. This indicates that the PLL's maximum operating frequency is approximately 1.3GHz (9/6.78ns $\approx$ 1.3GHz). This is simulated using the worst case process, temperature, and supply voltage variation on the extracted layout of the frequency divider. A safety margin of 0.1GHz provides the maximum reliable operating frequency for the prescaler of 1.2GHz.

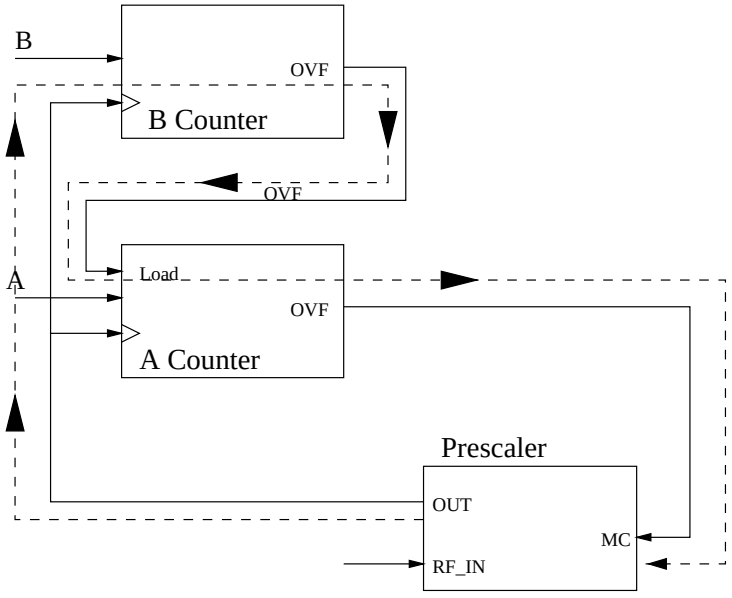


Figure 5.9: Critical path delay in the divider

5.3.3 Charge Pump Design

Figure 5.10 portrays the schematic diagram of the charge pump that we used [45]. One advantage of this architecture is that it has a fast settling time. Simulations indicated that the settling time of this charge pump is less than 7ns, within 1% of the final value.

The reason for this small settling time is that the current sources are never turned off; their current flows either to the output or to one of the supply rails. In short, the structure provides a high-speed single-ended charge pump. The disadvantage of this architecture is that up/down current mismatches may occur due to the difficulty in matching PMOS and NMOS devices.

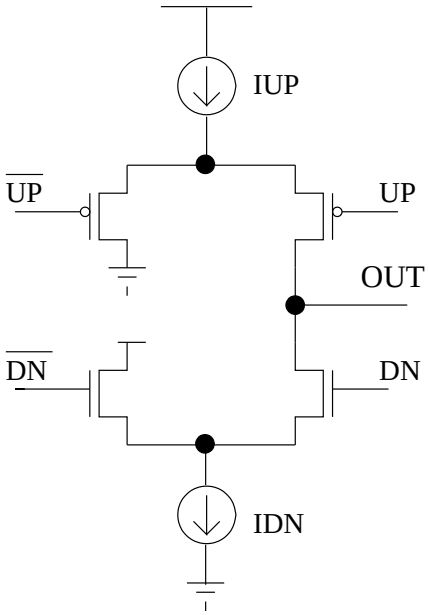


Figure 5.10: Current steering charge pump

5.3.4 Phase-Frequency Detector

A phase-frequency detector (PFD) is capable of detecting both phase and frequency differences. A logic diagram of the implemented PFD is depicted in Figure 5.11. Input $u_2(t)$ is the signal from the frequency divider, and $u_1(t)$ is the reference signal (external input). When $u_1(t)$ lags behind $u_2(t)$, the frequency generated by the VCO is too high. In this case, the DN signal is enabled. The DN signal goes into the charge pump, which lowers the control voltage of the VCO and decreases the output frequency of the VCO. A similar explanation holds true for the case

DN	UP	State
0	1	VCO frequency is too low
1	0	VCO frequency is too high
1	1	Both flip-flops are reset

Table 5.5: Different PFD states

when $u_1(t)$ leads $u_2(t)$. Conceptually, the PFD can be thought of as an ideal sampler with two mutually exclusive outputs. One output is asserted, if the VCO frequency is lagging behind the reference frequency, and vice versa. The different PFD states are listed in Table 5.5.

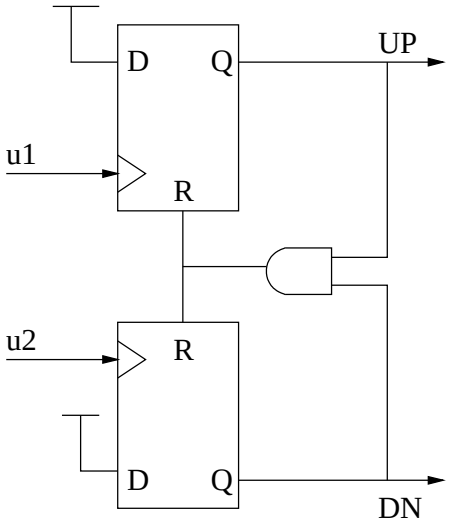


Figure 5.11: PFD logic diagram

One important issue concerning PFDs is the phase resolution that they are able to detect. For example, if the PFD can detect phase differences between $u_1(t)$ and $u_2(t)$ that are at least 100 ps apart, and the feedback division ratio is 10, this translates to a 1ns jitter on the PLL's output. The region in which the PFD cannot distinguish between the phases of the two input signals is known as the dead-zone band [46]. In this dead-zone band, the PFD behaves as a nonlinear device. Thus instead of acting as an ideal sampler, the PFD can cause the mixing of unwanted high frequency noise back to the baseband.

One method of reducing the effect of the dead-zone is by using a PFD with a delayed reset signal [47], as shown in Figure 5.12. This is similar to a conventional PFD, except that there is a delay on the feedback reset path. If we assume that the PLL is in lock, the PFD will always

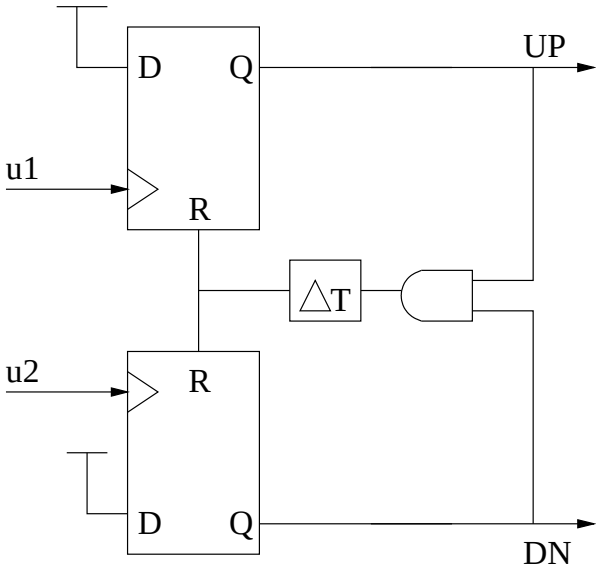


Figure 5.12: PFD with delayed reset signal

send two short UP and DN pulses, simultaneously, at every positive edge of $u_1(t)$ and $u_2(t)$. If a small differential phase develops between $u_1(t)$ and $u_2(t)$, the fall times of the two pulses may be much less than one gate delay. By using a PFD with a delayed reset signal, a timing resolution of less than 10 ps can be achieved. We note that the dead-zone band may still exist if slow circuit techniques are used, or if the circuit delay paths between the input and the UP and DN outputs are not balanced. Also, the output pulses are high for a longer time due to the additional delay in the reset path. Therefore, the problem of a mismatch of the current source in the charge pump increases by the number of additional delays in the reset path. This occurs because the amount of current added to the filter is proportional to the pulse width.

5.3.5 Digital Circuit Implementation

Although the maximum available operating frequency is higher than the targeted 13MHz, pipelining is used to speed up the delta-sigma modulator even further, for two reasons. First, it enables an even higher reference frequency to be used during testing to determine the effect of increasing the reference frequency on the phase noise performance of the delta-sigma PLL. Secondly, it enables the delta-sigma modulator to work at lower supply voltages while still operating at 13MHz. This helps to reduce the power consumption of the delta-sigma modulator. The accumulator

word width has been chosen equal to equal 24-bit to provide the targeted accuracy of the FN synthesizer.

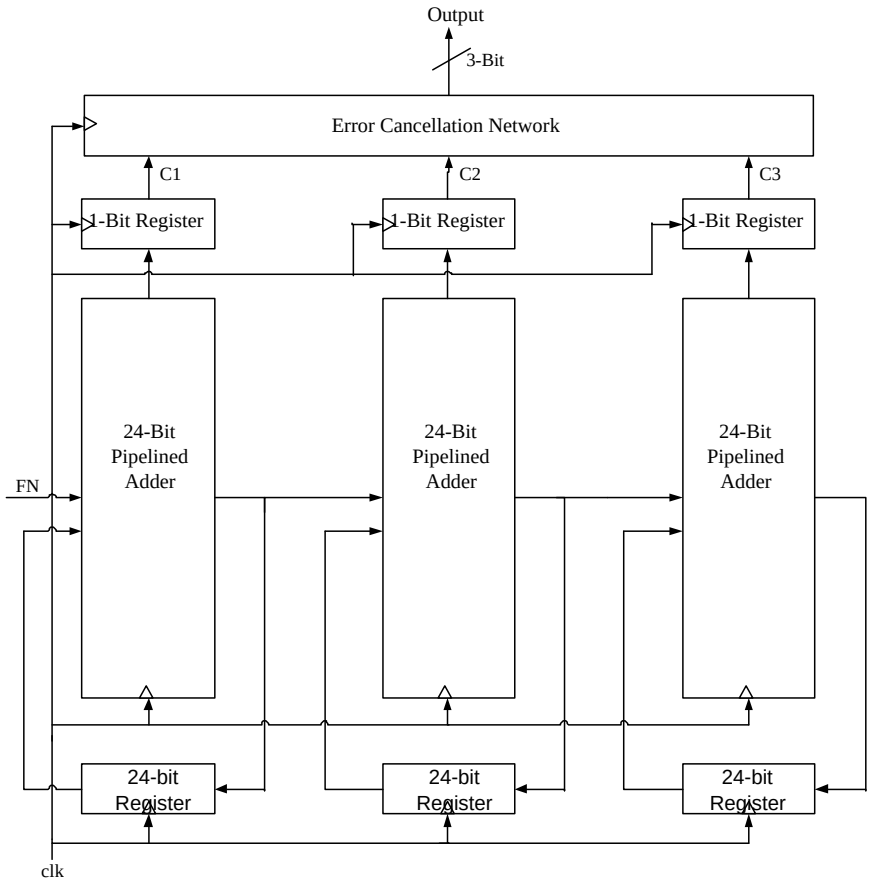


Figure 5.13: MASH 1-1-1 architecture implementation

Figure 5.13 illustrates the circuit realization of the MASH architecture of Figure 4.14. Each accumulator employs a pipelined 24-bit adder and a 24-bit register. It can be seen that there is a long delay chain between the accumulator overflow outputs; therefore, they appear at different time instances. To provide synchronization among the carry overflows, they are captured in 1-bit registers before being forwarded to the error cancellation network. The network performs the specific function of cancelling the quantization error from the first two stages, and produces a 3-bit output.

A 24-bit adder can be easily realized by using 24 full-adder (FA) logic circuits connected in cascade. However, a carry propagation between each FA may significantly reduce the operation speed of the overall design. For speed-up purposes, we have decided to use six cascaded 4-bit

carry-look-ahead (CLA) adders in the realization of 24-bit adders, as indicated in Figure 5.14. Since the clock operating frequency is equivalent to 13MHz, thus a pipelined stage can withstand a propagation delay of 77ns. We will therefore not gain the full benefits of using the high speed 4-bit CLA adder. However, the CLA adder has been chosen to clock this design at higher frequencies. In general, the 4-bit CLA adder is 50% faster than the 4-bit ripple adder [48].

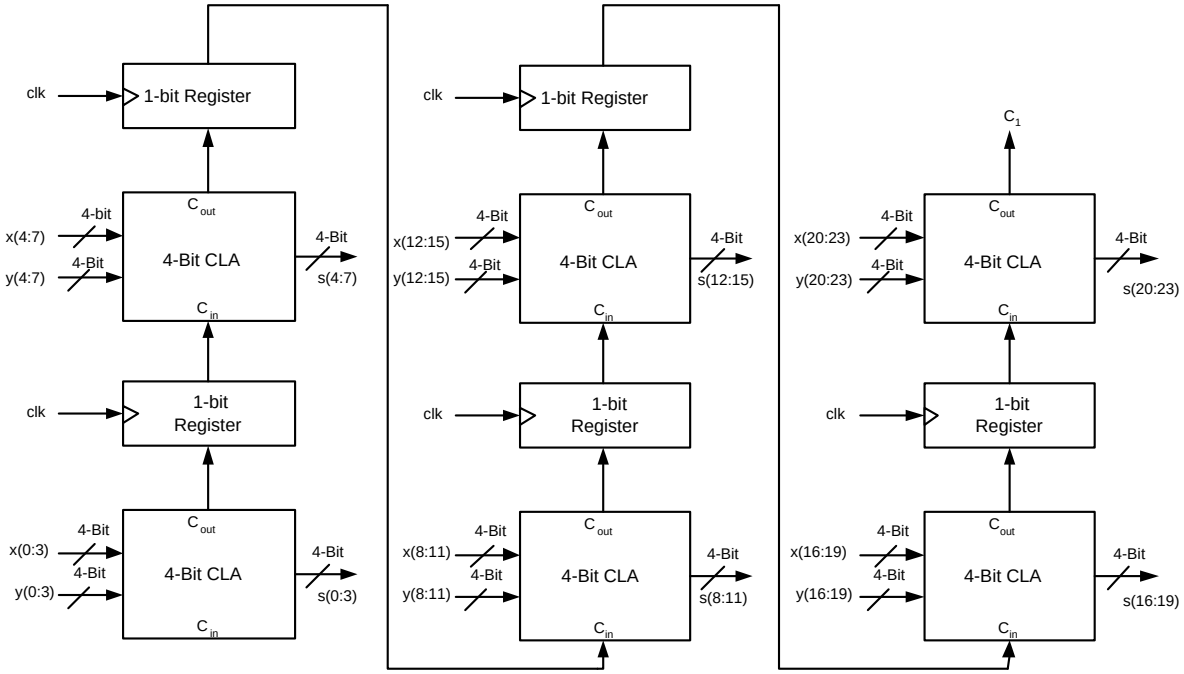


Figure 5.14: Pipelined 24-bit adder

Typically, a CLA adder circuit consists of three sub-systems, the propagate generator, the carry generator, and the sum generator. The logic equation for each sub-system is [49]

$$\begin{aligned} g_i &= x_i \bullet y_i \\ p_i &= x_i + y_i \\ c_{i+1} &= p_i \bullet (g_i + c_i) \\ s_i &= (p_i \bullet g_i) \oplus c_i \end{aligned} \tag{5.3}$$

where $x_i, y_i, c_i, and s_i$ represent the i^{th} bit of the first input, second input, carry out, and sum out, respectively. The carry propagation between each CLA stage results in the critical delay path

within the 24-bit adder; thus the maximum achievable operating frequency in a given process is limited by the overall computation speed of the six 4-bit CLA adders. A 24-bit CLA does not suffer from the carry chain problem, and may provide faster operation speeds. However, the hardware complexity increases exponentially with the number of bits at the CLA adder input. A simple approach to break the long carry chain in the adders is to employ the pipelining technique so that the carry information is only forwarded by one stage. In Figure 5.14, a 1-bit register is incorporated between each CLA stage to pipeline the 24-bit adder.

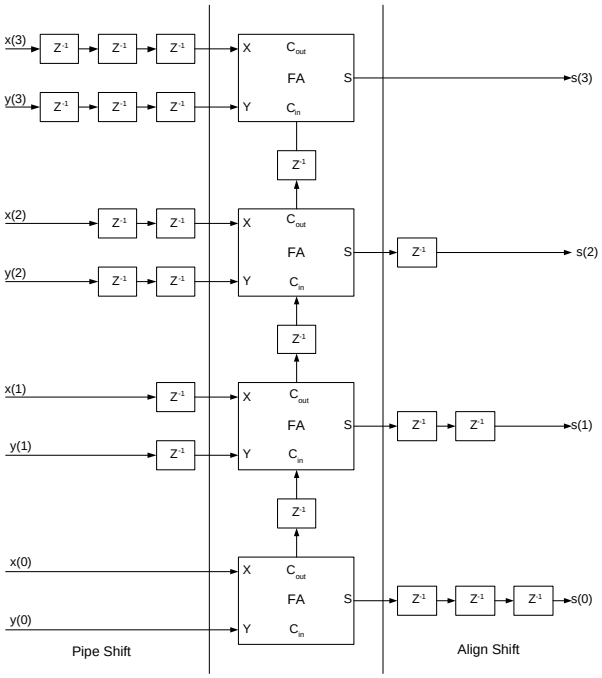


Figure 5.15: Pipelined 4-bit adder [3]

It should also be noted that in normal pipelined adders, additional registers are required to provide a time alignment between the input, delayed carry information, and the output. The bits of both inputs of the adder should be appropriately delayed to synchronize them with the true carry signals. Conversely, the output bits are realigned in time by employing the appropriate delays. A 4-bit example of such a pipelined adder is shown in Figure 5.15 [14]. Clearly, this topology operates on general time varying inputs. Since the modulator input is constant for the entire time, the input and output alignment registers can be completely eliminated in FN frequency synthesis applications. This occurs because the magnitude of the input to the modulator

Output Level	Out_3	Out_2	Out_1
-3	1	0	1
-2	1	1	0
-1	1	1	1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0

Table 5.6: Coding table for the MASH output

does not change with time, and hence, there is no need to store the same input bits and their corresponding output bits in the registers for synchronization. Consequently, the pipelined accumulator in Figure 5.14, without including the time alignment registers at the input and output of the adder, has been successfully utilized in the design of our MASH modulator. This results in a considerable savings in area and power.

The error cancellation network performs the following function [50]:

$$f(n) = C_3[n] - 2C_3[n-1] + C_3[n-2] + C_2[n] - C_2[n-1] + C_1[n] \tag{5.4}$$

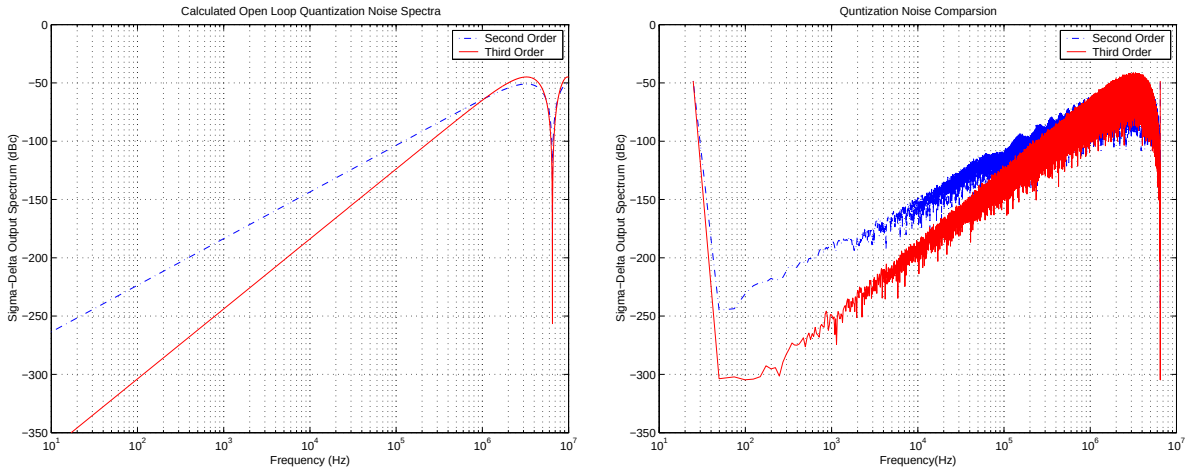
where $C_1, C_2, and C_3$ are the carry outs of the first, second, and third accumulators, respectively.

The output of the MASH is a signed multi-bit (3-bit) number, and 2's complement binary number representation is chosen, because it allows simple addition and subtraction. However, the 3-bit 2's complement system covers the numbers between -4 and +3, whereas the MASH 1-1-1 produces output levels between -3 and +4. To eliminate one additional bit coding at the output, we have coded the output level +4 as -4. Table 5.6 indicates the coding table of the MASH output indicating the output bits and their corresponding levels.

A serial interface is used to program and test the PLL chip. This serial interface controls various parameters of the MASH delta-sigma PLL such as the division ratio, operating mode of the delta-sigma modulator, and charge pump current. Both the serial interface, and the entire digital delta-sigma modulator are implemented using standard cells. A detailed description of the serial programming interface is shown in Appendix B

5.4 Simulation Results

High-level simulations using Verilog and Matlab are first conducted to compare the Verilog output with the Matlab output. The Verilog output sequence is windowed, and an FFT (Fast Fourier Transform) is applied on it to obtain the power spectrum of the output. Figure 5.16(b) shows the spectrum of the bit stream for a 24-bit static input of 258111, which corresponds to the fraction $\frac{1}{65}$. The simulation is run on 2^{18} samples, and the reference frequency is 6.5MHz. A slope of 40dB/dec of high-pass noise shaping is achieved for the second-order modulator, which increases to 60 dB/dec for the third-order modulator. The output spectrum from the model in (4.44) is shown in Figure 5.16(a), and indicates a close match with the Verilog output spectrum in Figure 5.16.



(a) (b)

Figure 5.16: MASH output spectrum for $\frac{1}{65}$ fractional channel: (a) theoretical output spectrum, and (b) Verilog output spectrum

We run the next set of simulations to measure the total output phase noise.

Figure 5.17 summarizes the contribution of the different blocks for both the second-order MASH and third-order MASH. The loop BW was set to 30kHz and the damping factor, ξ, was chosen to be 0.7.

In general, the phase noise spectrum can be divided into three regions (as previously discussed in Section 4.2.3.5. Near the central frequency f_o, the reference source is the main contribution to phase noise. At the greatest distance, from the loop bandwidth, the VCO contribution is

dominant. For both of these regions, the spectrum depends on an external component; as a result, their effect was not considered for simulation here. The third region, which is in between these two regions, depends on the PLL and the filter parameters.

From Figure 5.17, it is clear that in the loop bandwidth the charge pump contribution is dominant, since the quantization contribution is much less. The third-order has, approximately a 6dB degradation from the second-order modulator. Practically, we attain more degradation due to the non-linearity of the PFD. In our experimental measurements, we obtained a degradation of about 10dB. Outside the bandwidth, the quantization noise is the main contributor, which means the third-order modulator has better performance than the second order modulator.

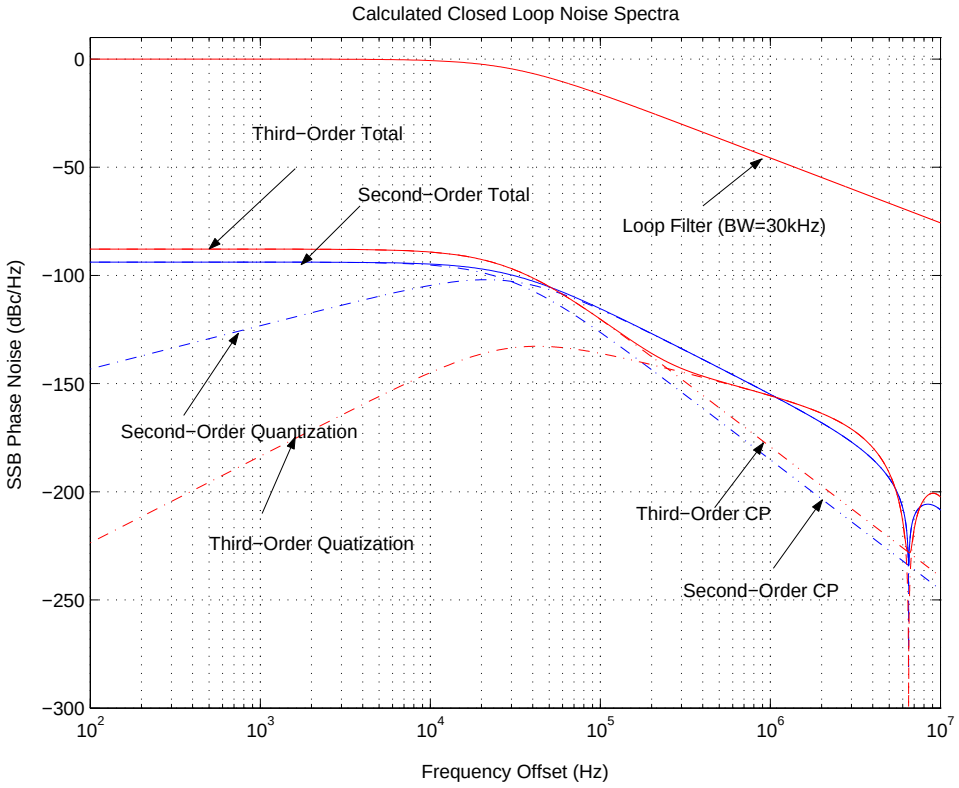


Figure 5.17: Calculated closed loop noise spectra

5.5 Experimental Results

A prototype fractional-N frequency synthesizer is fabricated in a 0.35 μm BiCMOS technology. The chip photograph is shown in Figure 5.18. The die area is 1.85x2.33 mm^2, which includes

the programmable digital delta-sigma modulator, serial interface, charge pump, phase-frequency detector, divider, and reference buffer amplifier. An external VCO with a centre frequency of 800MHz, and a gain of 50MHz/V is used. For a 13MHz reference frequency, a fractionality of $\frac{1}{65}$ is required to obtain a channel spacing of 200kHz. The channel spacing is reduced to 100kHz, if the reference frequency is reduced to 6.5MHz.

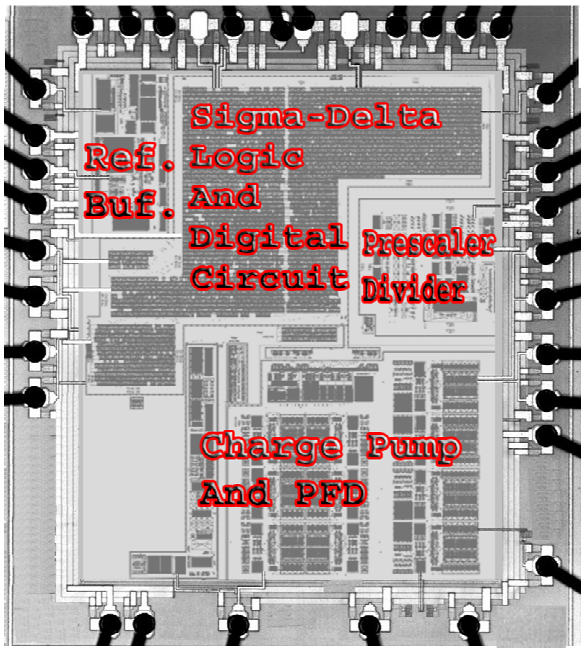


Figure 5.18: Fabricated chip

Several measurements are taken. The first set of measurements is the spurious performance of the delta-sigma PLL, and are carried out with a Hewlett-Packard HP8562A spectrum analyzer. The spur measurements for all the 65 channels are provided in Appendix C; the spurs for various orders of the delta-sigma modulator for fractional channels of $\frac{1}{65}$ and $\frac{4}{65}$ are depicted in Figure 5.19(a), and 5.19(b), respectively. The channel spacing is 100kHz, which corresponds to a 6.5MHz reference frequency.

The first-order delta-sigma modulator corresponds to a single accumulator controlling the division ratio. As the figures show, the maximum spur for the first-order delta-sigma modulator is at the desired fractional ratio. With the second-order and third-order delta-sigma modulators, the spurs at all the channels, but the desired fractional ratio, are fully suppressed. It was expected

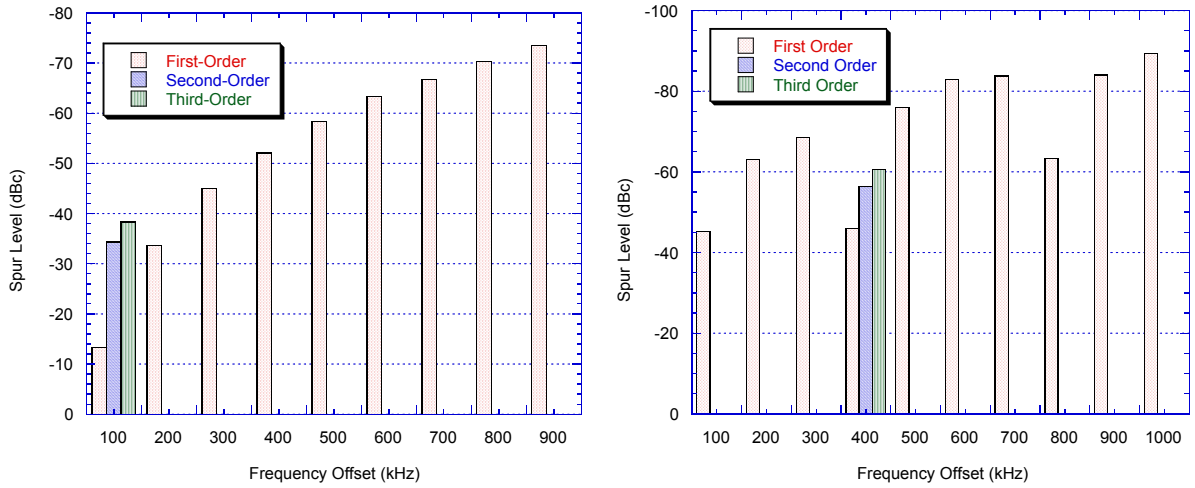


Figure 5.19: Spurious performance for: (a) $\frac{1}{65}$ fractional channel, and (b) $\frac{4}{65}$ fractional channel

that all the spurs would be eliminated. Even when constant seed[1] values are used, the spurs are not completely eliminated. However, the spur levels are less than those of the first order delta-sigma PLL. The second order delta-sigma PLL facilitates the reduction of the spur level by 20dB, and the third order delta-sigma PLL by 25dB, compared to the first order delta-sigma PLL. Another significant measurement that we can mention is that the spurs of the second-order and third-order modulators for fractional channels beyond $\frac{10}{65}$ are completely suppressed. This occurs because the spur are generated at a 10*100kHz=1MHz offset away from the carrier, which is high enough in frequency to be suppressed by the closed-loop low-pass filter response.

The phase noise performance of the delta-sigma PLL is also measured. An HP8562A spectrum analyzer with a phase noise measurement module is used. The phase noise for various orders of the delta-sigma modulator for the fractional channels of $\frac{2}{65}$ and $\frac{26}{65}$ are shown in Figure 5.20(a) and 5.20(b), respectively.

As we mentioned in Section 5.3.1, the closed loop bandwidth is 30kHz. The close-in phase noise is measured at a 10kHz offset. For the first-order and second-order delta-sigma PLLs, a close-in phase noise of around -90dBc/Hz is measured for all the fractional channels. For the third-order delta-sigma PLL, the close-in phase noise is measured to be between -75 and -85dBc/Hz. This represents a 5dBc/Hz to 15dBc/Hz degradation in phase noise. This phase noise has been

[1]A dithering signal applied by altering one or more LSBs

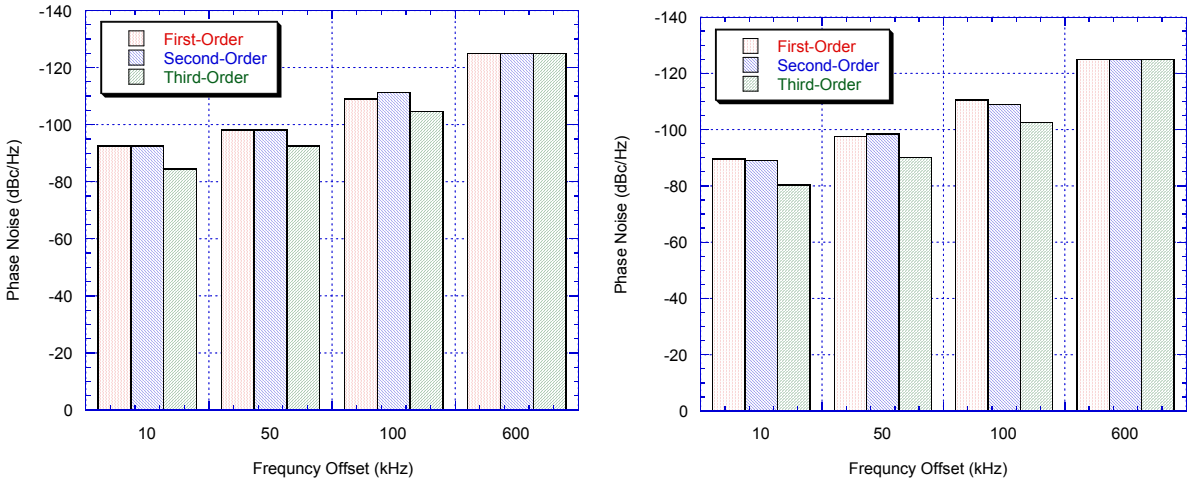


Figure 5.20: Phase noise performance for: (a) $\frac{2}{65}$ fractional channel, and (b) $\frac{26}{65}$ fractional channel

attributed to the nonlinear behaviour of the PFD due to the presence of a dead-zone region.

The power consumption of the delta-sigma PLL has also been measured. If we use a 3.3V supply voltage to all parts of the PLL, the total power consumption of the test chip is 27mW for the third-order delta-sigma. In our design, the emphasis was on a robust and safe design, rather than a low-power design. As the results have shown, the close-in phase noise of the PLL is far less than the -70dBc/Hz required for the GSM and GPRS standards. This extra performance can be traded off for less power consumption in future designs.

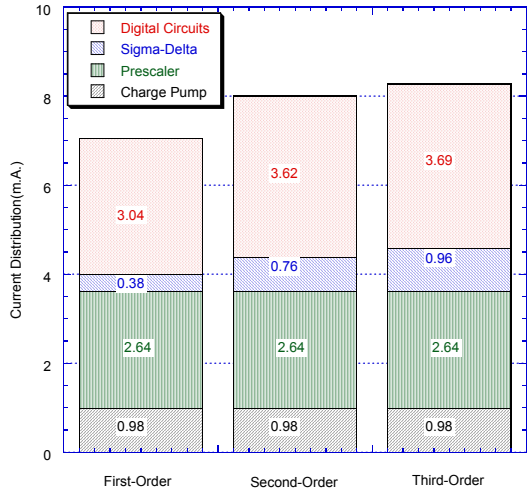


Figure 5.21: Measured current distribution

	GPRS	Measured
Phase Noise @ 10kHz (dBc/Hz)	-70	-80
Phase Noise @ 3MHz (dBc/Hz)	-123	-125
Power Supply (V)	-	2.0 - 5.0
Fractional Spurs (dBc) @ 0.4MHz	-54	-60
Power Consumption (mW)	-	27 @3.3V 13 @2V
Lock Time (μs)	200	95
Frequency Range (MHz)	880-915	128-1200
Frequency Resolution (Hz)	200k	< 1

f_R = 6.5MHz, Loop Bandwidth = 30kHz

Table 5.7: Performance summary

The current breakdown of the chip for different delta-sigma orders is illustrated in Figure 5.21. The use of a first-order or second-order delta-sigma modulator consumes a total power of 23mW and 26mW, respectively.

The measured performance is summarized in Table 5.7.

5.6 Conclusion

In this chapter, the design of a MASH delta-sigma fractional-N PLL has been detailed, optimized for GSM and GPRS wireless communications standards. A test chip has been fabricated, and the test results have been demonstrated. We have demonstrated that delta-sigma modulation has reduced the spurs, but not completely eliminated them. However, the spur levels meet the GSM and GPRS specifications. The power consumption of the chip was dominated by the dividers. In future designs, a lower power consumption can be achieved by using less current in the prescaler. The effect of the use of a constant seed has been investigated. A constant seed did not succeed in eliminating the spurs as we anticipated. To completely eliminate the spurs generated by the fractional-N divider, different architectures must be explored. In Chapter 6, new architectures will be proposed to address the spur problem, as well as the power consumption of the modulator developed in this chapter.

Chapter 6

New Fractional-N Frequency Synthesizer Architectures

6.1 Introduction

The proliferation of wireless products over the last decade has been rapid, and has increased the momentum to make wireless computing a reality. New wireless data standards such as GPRS and HSCSD have brought new challenges for the design of a wireless transceiver. One pivotal component of the wireless transceiver is the frequency synthesizer.

In mobile computing applications, narrow channel spacing is necessary to efficiently utilize the available frequency spectrum. In contrast, fast switching from one channel to another is necessary for high-data rates. One way to satisfy these two conflicting requirements is to use a fractional-N PLL architecture. Fractional-N PLLs are capable of synthesizing frequencies at channel spacings that are less than the reference frequency. This helps to increase the reference frequency, and therefore, reduce the PLL's lock time [51].

One major disadvantage of fractional-N PLLs is the generation of high tones at multiple values of the channel spacing. The use of digital delta-sigma modulation techniques in fractional-N PLL frequency synthesis has been previously suggested [11] to eliminate spurs. Other advantages of delta-sigma PLLs include an arbitrarily small frequency resolution, a wide tuning bandwidth, and a fast switching speed. However, the designed chip in Chapter 5 which was based on a modified version to the modulator in [11], showed a significant spur level, as well as a high power

consumption.

In this chapter, three alternative delta-sigma modulator architectures will be proposed. The first architecture addresses the spur reduction through the use of the delta-sigma modulator output as a dithering signal. The second architecture targets the speed and stability issue, and the power dissipation by replacing the delta-sigma block with a pre-calculated ROM. The last architecture is a tapered one, which deals with both the power dissipation and the spur level. Each new architecture design will be presented, and the experimental results analyzed to evaluate the overall performance. Some conclusions are drawn in Section 6.6.

6.2 Dithering

When a DC input is fed into the delta-sigma-modulator (which is the case for a frequency synthesizer), a periodic quantization error signal is obtained at the output [26]. The frequency content of the quantization noise depends on the DC-input level [4]. If the noise tones are in the same bandwidth as the signal range, the signal is corrupted with noise. Peaks of noise (spurs) appear for the fractional values of the input [4].

There may be several possibilities to improve the behaviour of the delta-sigma modulator toward the DC inputs; one of these solutions is dithering. In order to avoid tones in the delta-sigma modulator, the input is kept busy by a low-level white noise signal that is added to the input before the quantization, which makes the total quantization error behave like white noise [27].

In the following sections, new frequency synthesizer architectures will be detailed to address the spur problem in fractional-N frequency synthesizers.

6.3 Feedback Architecture

As we discussed in Section 6.2, one of the common solutions to the problem of reducing the spurs in fractional-N frequency synthesizers is to introduce some perturbation into the delta-sigma sequence. This is achieved by using a dithering signal, which is usually generated from a pseudo random generator.

Since the output of the delta-sigma modulator is somewhat similar to the pseudo random generator, we can use the output of the delta-sigma modulator as a source for the dithering

signal. The main constraint is the stability of the new architecture. However, this problem may be avoided by selecting an unconditionally stable architecture such as the MASH architecture, which has been implemented in Chapter 5.

Figure 6.1 represents the block diagram of the designed delta-sigma modulator frequency synthesizer, and the implemented delta-sigma modulator is illustrated in Figure 6.2. This architecture is the same as the modulator that was implemented in Chapter 5, except for the addition of the dithering block. The dithering block design was flexible enough to allow a change up to six LSBs with any required combination, and with a controllable frequency which is driven form the main delta-sigma clock frequency. One cell from the dithering block schematic is represented in Figure 6.3. As shown in this figure each output bit from the dithering block can be assigned to any of the three sigma-delta modulator output bits. The chip layout is the same as the chip that was shown in Figure 5.18 after adding the dithering block layout, which is shown in Figure 6.4.

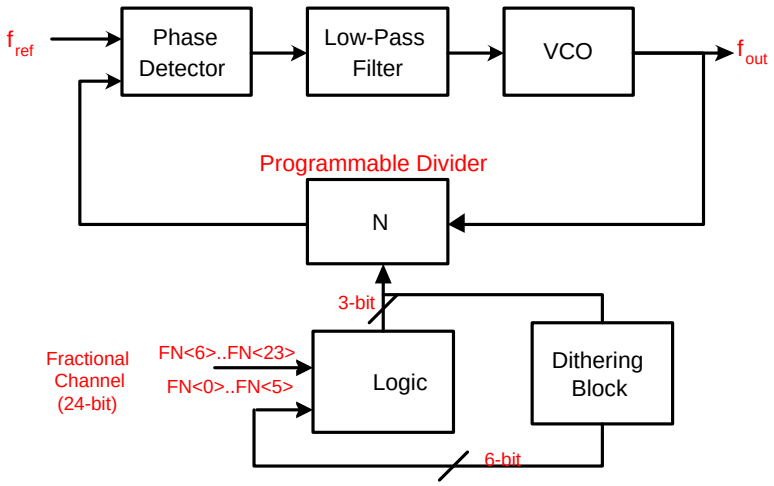


Figure 6.1: Feedback delta-sigma modulator frequency synthesizer

A choice of up to six LSBs has been allowed to make sure that the final fraction is not affected by altering the bits. The output signal of the proposed structure, and the original architecture, implemented in Chapter 5, are compared in terms of spur performance and phase noise.

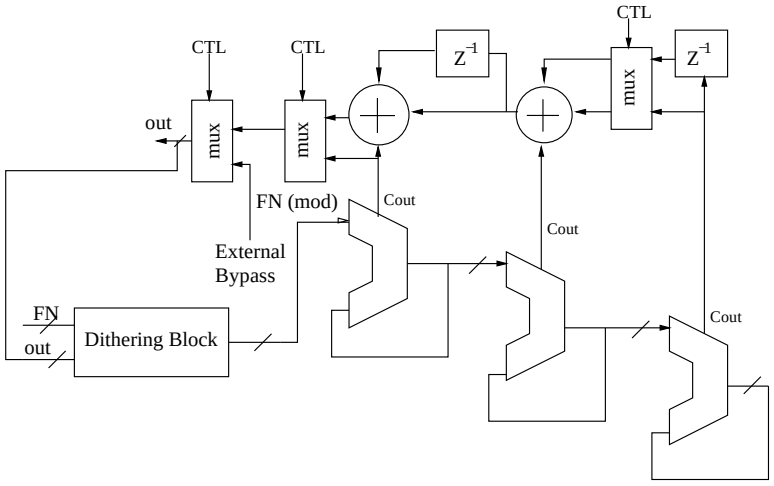


Figure 6.2: Feedback MASH 1-1-1 architecture

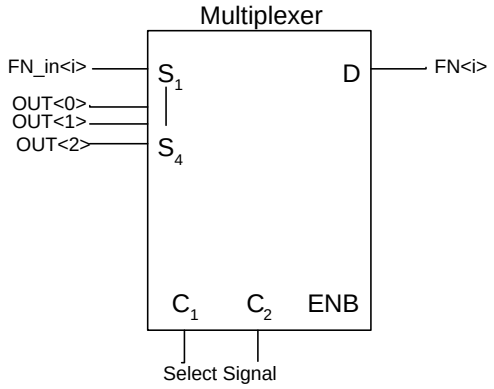


Figure 6.3: Basic dithering block cell

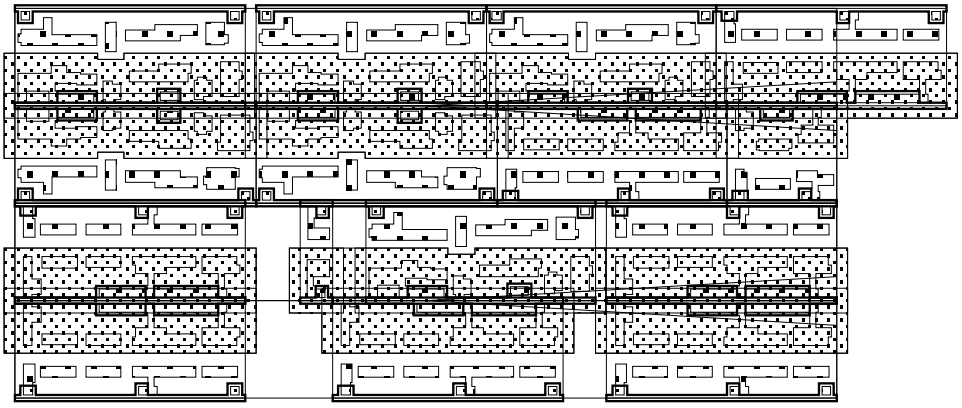
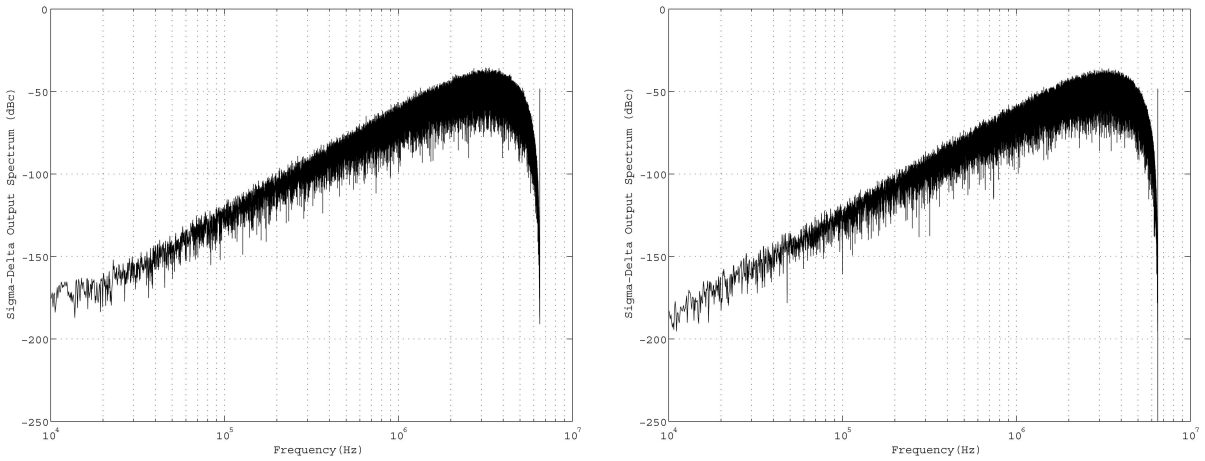


Figure 6.4: Dithering block layout



(a) (b)

Figure 6.5: Output spectrum: (a) with delta-sigma feedback, and (b) without feedback

6.3.1 Simulation and Experimental Results

A high level simulation by using Verilog and Matlab was conducted to compare the quantization noise of the regular and the feedback MASH structure. The simulation was done for a fractional channel $\frac{1}{65}$, which corresponds to a 100KHz channel-spacing, if we assume that we have a 6.5MHz reference frequency. The FFT of the modulator output for a decimal input 258111, corresponding to a $\frac{1}{65}$ fraction, is shown in Figure 6.5, where a clock frequency of 6.5 MHz is used. Both versions confirm the 60dB/dec increase in the spectrum validating the third-order noise shaping.

Now, we must use the feedback technique to measure the fractional spurs reduction. Using HP8562A spectrum analyzer, the output spectrum of the feedback architecture is compared to the original MASH architecture in Chapter 5. A reduction of 14dB is measured, as demonstrated in Figure 6.6, for the same 0.0153846 fraction which corresponds to a 100KHz spacing with a clock frequency of 6.5 MHz.

6.4 ROM-Based Architecture

As we discussed in Chapter 4, the delta-sigma technique is considered to be a valuable approach for fractional-N frequency synthesis. However, it suffers from some limitations, which may be summarized as follows:

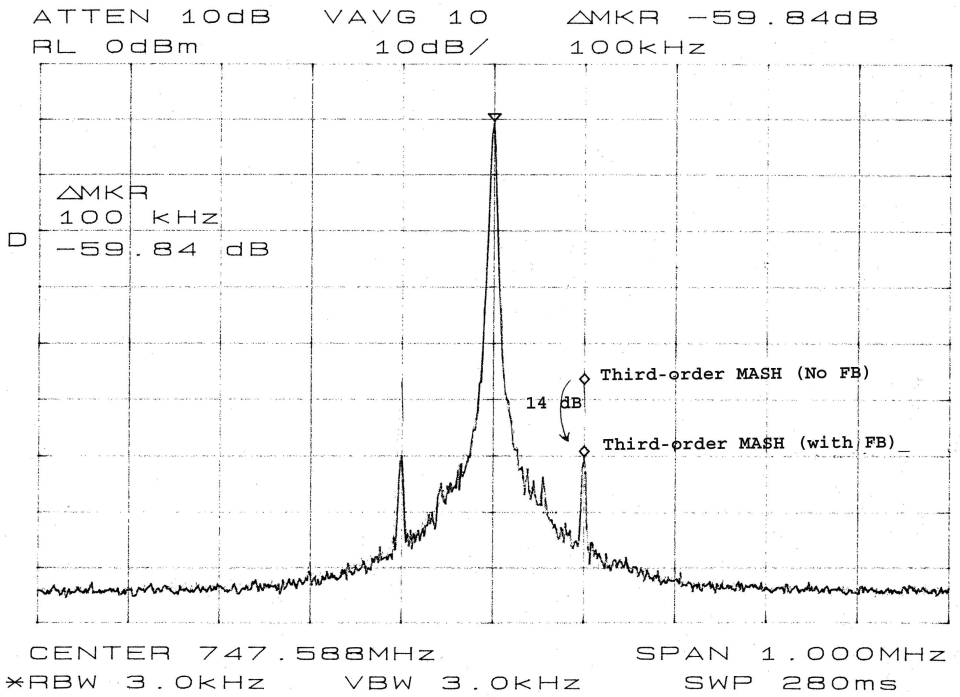


Figure 6.6: Measured spectrum at VCO output

- **Speed Limitation:** The delta-sigma output is calculated in real time, which significantly reduces the maximum operating frequency.
- **Power Dissipation:** The power dissipation depends mainly on the delta-sigma architecture, and the order of the delta-sigma. Increasing the order results in a better close-in noise, but it is at the expense of design simplicity, stability, and low-power dissipation.
- **Stability:** Not all delta-sigma modulators are unconditionally stable, especially higher order ones.
- **Fixed Design:** Achieving the specification for each individual channel may require a different design in terms of the delta-sigma order and parameters.

To overcome these limitations a ROM-based delta-sigma frequency synthesizer is proposed. Figure 6.7 illustrates the architecture that is developed to overcome the previously discussed limitations.

In this approach, we replace the delta-sigma logic with a ROM and a counter to control the divider using the pre-stored sequence obtained from Verilog/Matlab simulations. The counter width

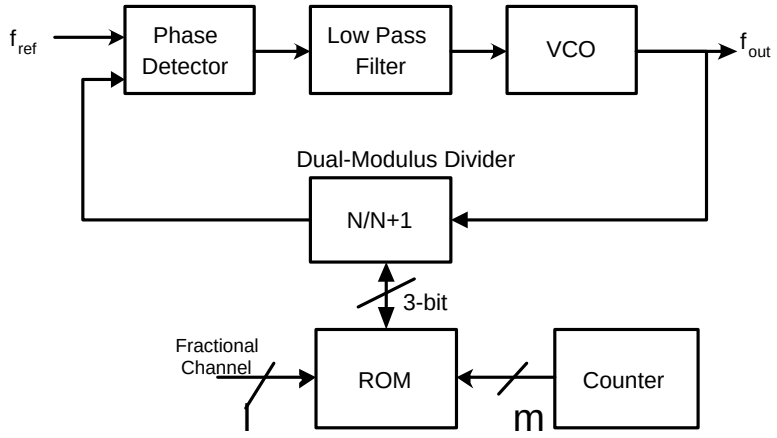


Figure 6.7: Proposed ROM-based fractional-N frequency synthesizer

m is chosen to scan the entire ROM address for one channel. The total bit stream length/channel is equal to 2^m. The ROM size is equal to 2^m times the total number of fractional channels. If we choose a bit stream length of 64K word/channel and assume that we have 65 different fractional channels (corresponding to 200 kHz channel spacing at a reference frequency of 13 MHz in GSM standard), the total ROM size is equal to 12Mbits for the required 3-bit output word.

6.4.1 Simulation and Experimental Results

A high level simulation using Verilog and Matlab is conducted to compare the phase noise between the ROM implementation and the real time delta-sigma. The simulation is run for a fractional channel $\frac{1}{65}$ which corresponds to a 100KHz spacing, if we assume that we have a 6.5MHz reference frequency. Figure 6.8 portrays a comparison between the quantization noise for the ROM and the real time version.

As we discussed in Section 5.2 one of the advantages of the structure proposed in Chapter 5 is its flexibility to test new techniques by using the bypass mode. The third-order delta-sigma 3-bit output sequence was generated by using the Verilog/Matlab simulation. The results were stored in an HP8180A data generator to simulate the required ROM. Figure 6.9 reflects the measured spectrum at the VCO output for the regular third-order MASH delta-sigma, and two different ROM settings. The first ROM setting contains the output stream of the Matlab simulations on the real MASH architecture, whereas the other setting contains the output from Verilog simulations. The measured results show a close match between the real time calculations and both ROM

versions.

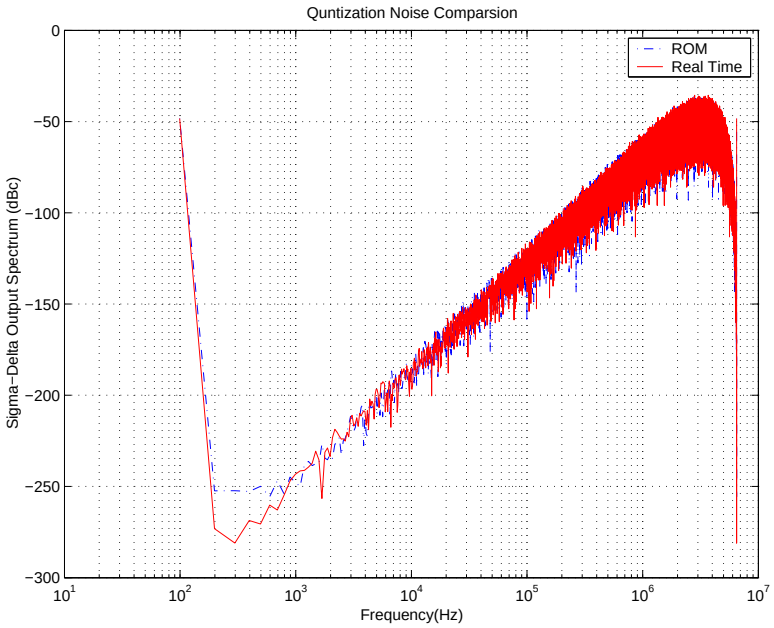


Figure 6.8: Quantization noise comparison between ROM and real time calculations

To calculate the power that is saved, the power required by the ROM is compared to the power consumption by the delta-sigma modulator. In [52], a 1M-bit is reported, which consumes 0.02694 mW/MHz at 5V supply voltage. This can be expressed as 0.005388 mA/MHz for 1M-bit ROM. The size required for a 64M word is calculated earlier as a 12M-bit. Therefore, the current consumption is 0.42mA, if a reference frequency of 6.5MHz is assumed. In Section 5.5, the current consumption of the third-order MASH at the same reference frequency is 0.96mA, whereas the total synthesizer current consumption is 8.17mA. Consequently, we can achieve a power saving of more than 56% in the delta-sigma block, or 6.6% in the whole synthesizer by using the ROM architecture[1]. The current distribution is modelled in Figure 6.10.

The concept that is introduced here may be extended to more transmitter blocks to enhance the power and speed performance. In Chapter 7, we will use a similar concept to design a high performance memory-based analog-to-digital converter.

[1]The counter power dissipation is not taken into consideration

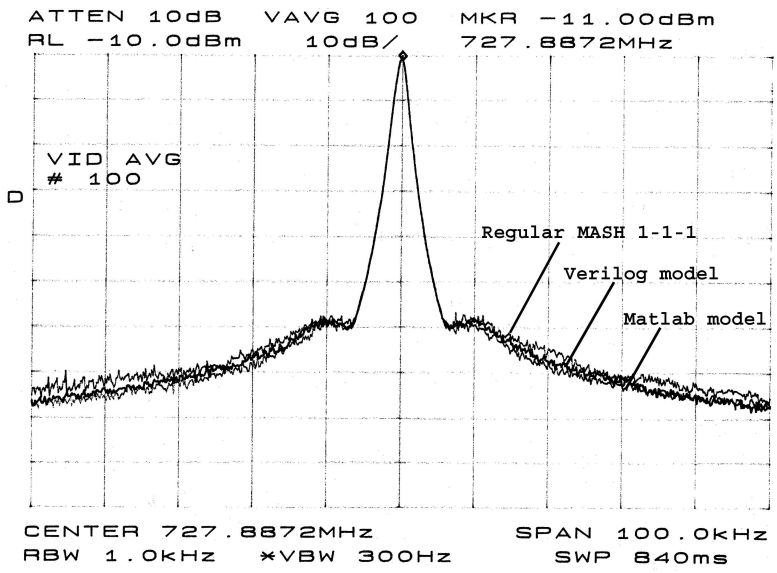


Figure 6.9: Measured spectrum at VCO output

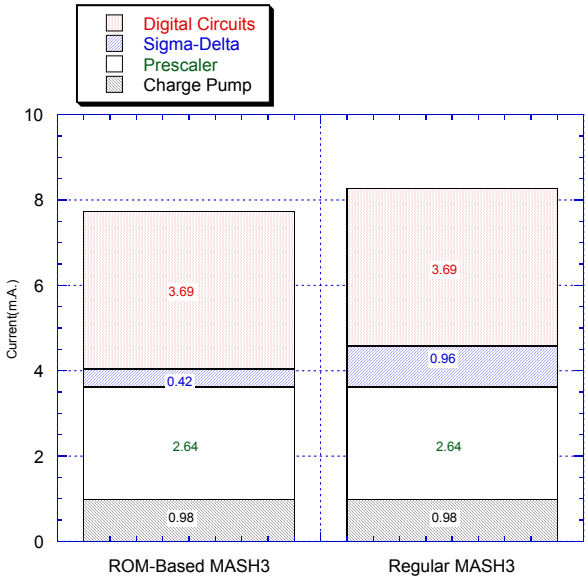


Figure 6.10: Current distribution for regular and ROM-based MASH 1-1-1 delta-sigma modulator

6.5 Tapered Architecture

In the last two sections, two architectures have been proposed for FN delta-sigma frequency synthesis. The major advantage of the feedback architecture is the reduction of fractional spurs without affecting the power dissipation of the architecture, whereas the ROM-based architecture reduces the power dissipation without affecting the spurious performance. In this section, we will propose another architecture which combines these two advantages. We will call it tapered architecture.

Ideally, the tapering should not alter the final outcome of the delta-sigma structure, as compared to the non-tapered implementation. A typical example of a tapered structure is a third-order structure, which has 24-bit at the first integrator output, 17-bit at the second integrator output, and 10-bit at the last integrator output.

In the following sections, two delta-sigma structures that were developed to verify the new architecture are described. These structures are a third-order single-stage multiple feedback delta-sigma modulator, and a third-order MASH 1-2 delta-sigma modulator. Each structure is realized in both a tapered and non-tapered implementation. Tapering means that the word width of each integrator stage is reduced to a smaller size than the previous stage. This not only saves hardware, but also power. Another advantage, is the spur reduction, which may be explained by the internal dithering properties of the proposed tapered structure.

6.5.1 Third-Order Single-Stage Multiple Feedback Delta-Sigma Modulator

Figure 6.11 shows the block diagram of the third-order single-stage multiple feedback delta-sigma modulator, which has three cascaded integrators.

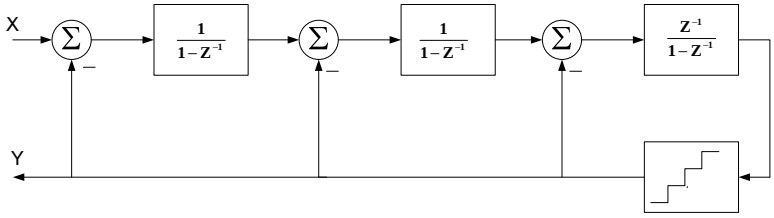


Figure 6.11: Single-stage multiple feedback delta-sigma modulator

In a cascaded architecture, each integrator stage is in itself a single-stage delta-sigma modula-

tor. The quantization error in each stage, which is defined to be the difference between the input and output of the quantizer, serves as the input to the following stage. The output of the following stage is then an approximation of the quantization error. By subtracting the approximated error from the output of the previous stage, most of the quantization error can be cancelled. The principal disadvantage of cascaded architectures is that they have more restrictions on device tolerances. In order to properly cancel the quantization error, the gains in each integrator stage must match closely.

The top level I/O interface of the third-order single-stage multiple feedback delta-sigma modulator structure is depicted in Figure 6.12.

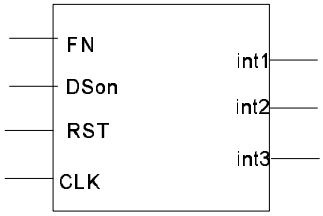


Figure 6.12: I/O interface of single stage multiple feedback delta-sigma modulator

The used I/O pins are detailed as follows:

- The input signal, FN, is 21-bit wide. It represents the fractional part of the divide value that the fractional-N frequency synthesizer is required to create.
- The input signal, DSon, is used to enable or disable the whole delta-sigma block.
- The input signal, RST, is used to reset all the flip-flops within the integrators.
- The input signal, CLK, is the input clock, nominally set at 26MHz.
- The output signal, int1, is the output of the first integrator stage.
- The output signal, int2, is the output of the second integrator stage.
- The output signal, int3, is the output of the third integrator stage.

6.5.1.1 Top Level Description of the Third-Order Single-Stage Multiple Feedback Delta-Sigma Modulator

In this section, the architectures of the third-order single-stage multiple feedback delta-sigma modulator are described. Figure 6.13 shows the details of the non-tapered (regular) version; Figure 6.14 shows the tapered version.

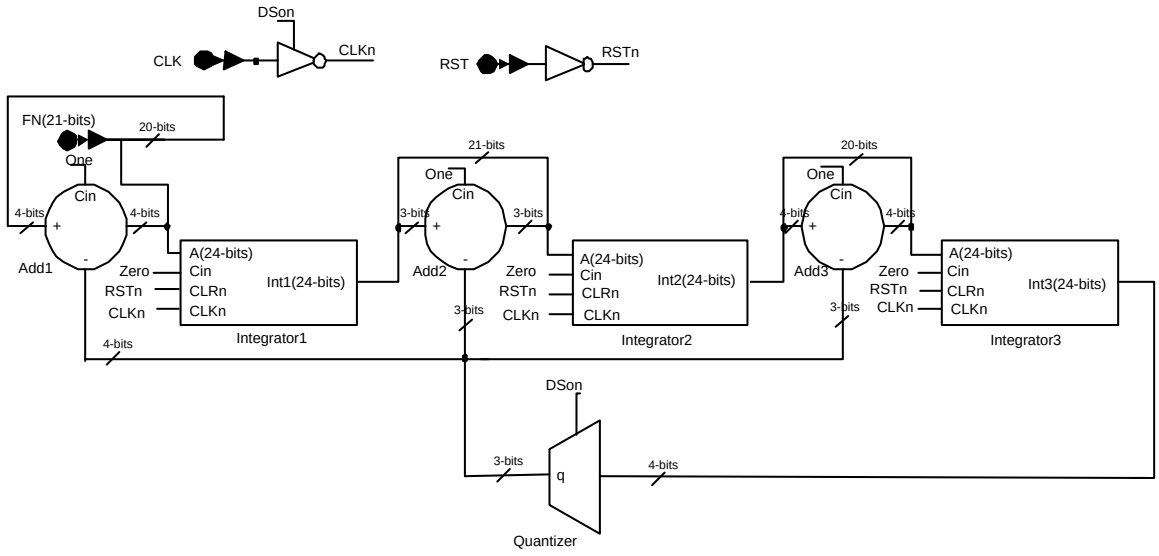


Figure 6.13: Regular single-stage multiple feedback delta-sigma modulator schematic

The third-order single-stage multiple feedback delta-sigma modulator structure has three stages. For the tapered version, the word widths of the first, second and third-stage are 24-bit, 17-bit, and 10-bit, respectively. The non-tapered version has a width of 24-bit for all three integrators. The optimum width for each integrator is obtained from Simulink simulations.

For the first stage, the most-significant-bit (MSB) of the input signal, FN, is bit extended four times before being passed to the adder "Add1". The 3-bit feedback quantization signal, q, is also bit extended to 4-bit and passed to this adder.

We should note that the C_{in} bit is set to HIGH (i.e., One). This indicates that 2's complement arithmetic is used in "Add1". The rest of the FN bits are not altered by the adding operation; thus, they are passed directly to the input of the first stage integrator.

For the tapered version, the first-stage integrator passes the 2-MSBs after the bit extension to 3-bit to the adder "Add2", whereas the next 14-bit are passed directly to the input of the

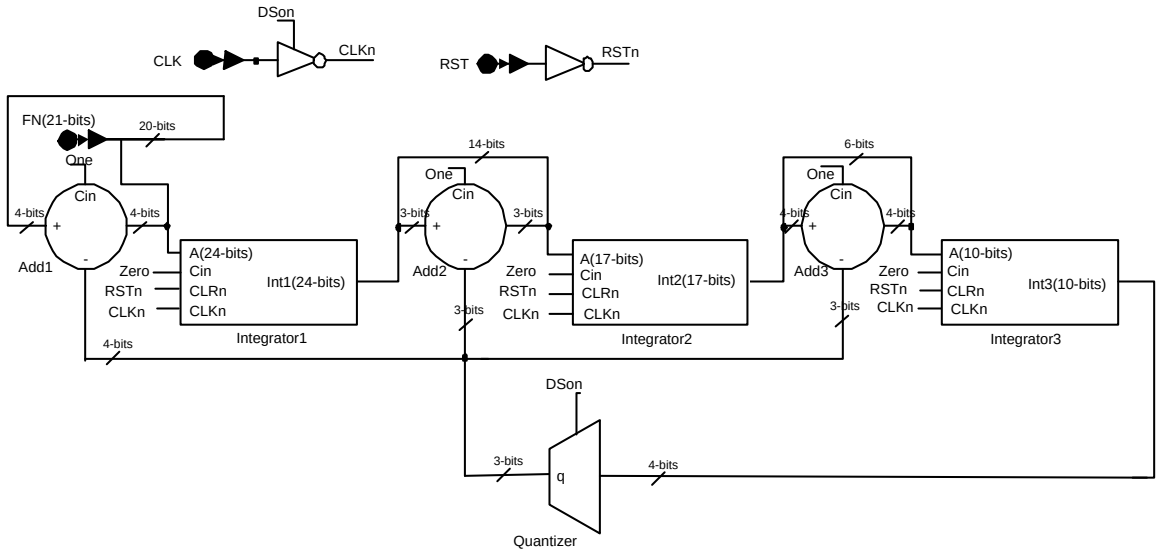


Figure 6.14: Tapered single-stage multiple feedback delta-sigma modulator schematic

second-stage integrator. We can see that the first seven bits are tapered off. For the non-tapered version, the first-stage integrator passes the 3-MSBs to the adder "Add2", whereas the next 21-bit are passed directly to the input of the second-stage integrator. None of the bits is tapered off. Two's complement arithmetic is used within the adder "Add2". The same approach is applied to the second and third integrator stage.

In the tapered version, the next block is an 8-level 4-bit quantizer. The quantizer takes 4-MSBs from the third integrator (bits 9 to 6). For the non-tapered version, the quantizer takes 4-MSBs (bits 23 to 20).

The 3-bit output signal from the quantizer is fed back to all three integrator stages. This signal represents the fractional part of the dividing ratio.

6.5.1.2 Experimental Results

We used the same MASH frequency synthesizer that was implemented in Chapter 5 in the bypass mode, and both the tapered and non-tapered architectures were implemented and simulated with Verilog with the 3-bit output stream stored in an HP8180A data generator. To evaluate the performance of the tapered architecture, we conducted a series of experiments. First, the Verilog output was compared with the Simulink output to make sure that each block was operating properly. After that, the VCO output spectrum and phase noise for both the tapered and

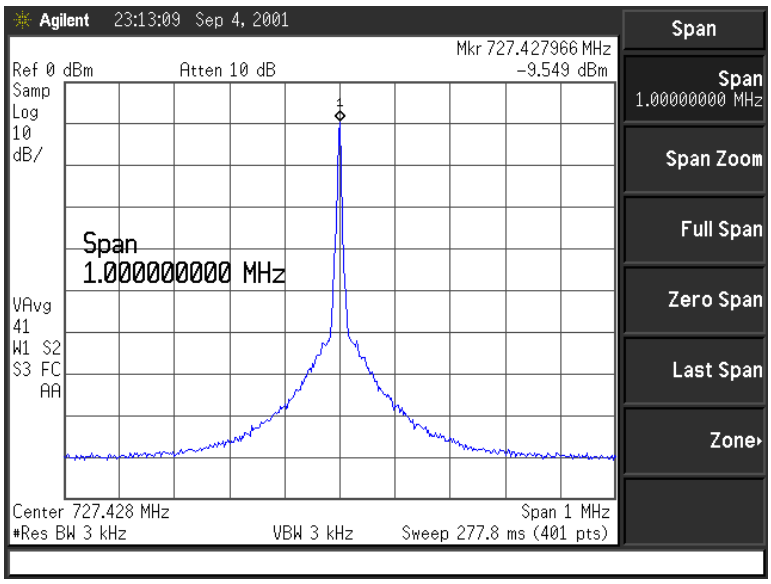


Figure 6.15: VCO output spectrum for the tapered single-stage multiple feedback delta-sigma modulator

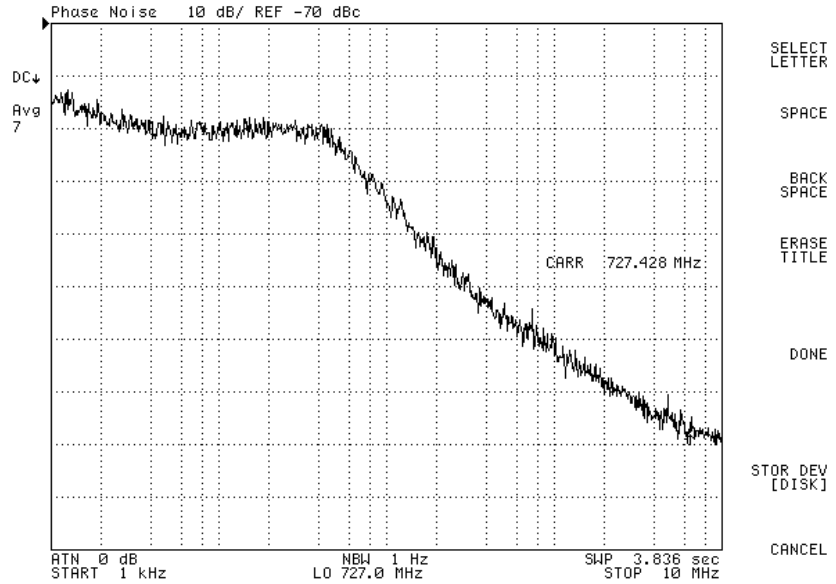


Figure 6.16: Output phase noise for the tapered single-stage multiple feedback delta-sigma modulator

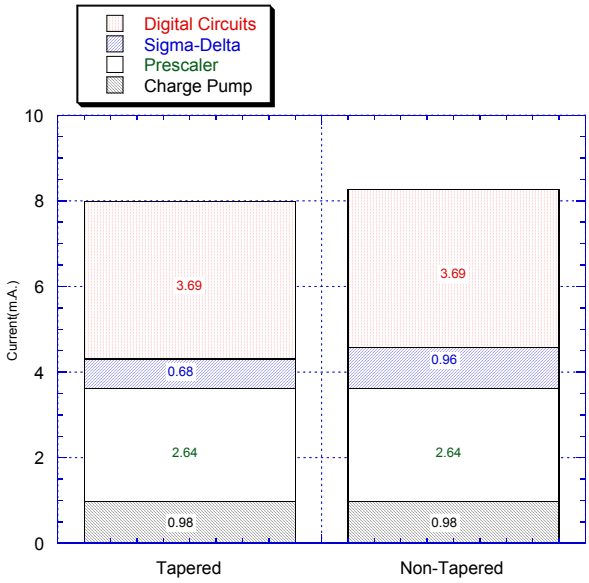


Figure 6.17: Current distribution for tapered and non-tapered single-stage multiple feedback delta-sigma modulator

non-tapered structures were measured. Measurements were done for a fractional channel $\frac{4}{65}$, corresponding to a 400KHz spacing with a 6.5MHz reference frequency. Figure 6.15 reflects the output VCO spectrum from an Hewlett-Packard E4407B spectrum analyzer; Figure 6.16 models the phase noise spectrum, measured by an HP4352B PLL/VCO analyzer. The results shown here are for the tapered version. Both versions indicate comparable performances except for a higher noise floor for the tapered version.

Now, to calculate the power saving in the delta-sigma modulator, as well as the total saving in the frequency synthesizer, we can assume that the total capacitance of the accumulators is directly proportional to the number of bits, as well as the power dissipation [53]. If we calculate the total number of bits in the accumulator in both designs, we obtain 72-bit for the non-tapered version, and 51-bit for the tapered version. This translates to a power saving of 29% in the delta-sigma modulator, or a 3.5% saving in the whole frequency synthesizer. The current distribution is reflected in Figure 6.17.

6.5.2 MASH 1-2 Delta-Sigma Modulator Structure

Figure 6.18 shows the block diagram of the MASH 1-2 delta-sigma modulator. The MASH 1-2 structure is a two-stages modulator. The first stage modulator is made up of one integrator. The second stage modulator consists of two cascaded integrators, which is a second-order modulator. In this structure, the quantization error from the first stage is fed forward so that it can be converted by the second modulator. The MASH 1-2 structure has some advantages over the MASH 1-1-1 structure in Chapter 5. For example, the MASH 1-2 structure has better spurious performance [54]. The biggest disadvantage of the architecture is that it only allows the input to operate within 75% of the whole fractional range because of stability issues [55]. That means that in our design, the attainable fractional channels for normal behaviour range from $\frac{9}{65}$ to $\frac{56}{65}$.

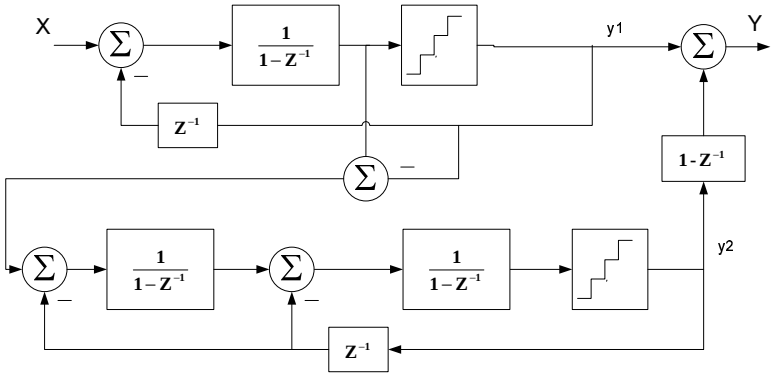


Figure 6.18: MASH 1-2 delta-sigma modulator structure

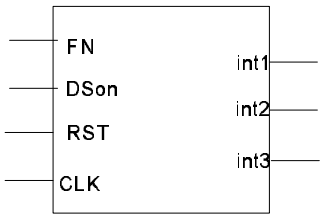


Figure 6.19: I/O interface of MASH 1-2 delta-sigma modulator

The top level I/O interface of the MASH 1-2 structure is shown in Figure 6.19. The used I/O pins are detailed as follows:

- The input signal, FN, is 21-bit wide. It represents the fractional part of the divide value that the fractional-N frequency synthesizer is required to create.

- The input signal, DSon, is used to enable or disable the whole delta-sigma block.
- The input signal, RST, is used to reset all the flip-flops within the integrators.
- The input signal, CLK, is the input clock, nominally set at 26MHz.
- The output signal, int1, is the output of the first integrator stage.
- The output signal, int2, is the output of the second integrator stage.
- The output signal, int3, is the output of the third integrator stage.

6.5.2.1 Top-Level Description of MASH 1-2 Delta-Sigma Modulator

In this section, the architectures of the MASH 1-2 delta-sigma modulator are described. Figure 6.20 shows the details of the non-tapered (regular) version. Figure 6.21 shows the tapered version.

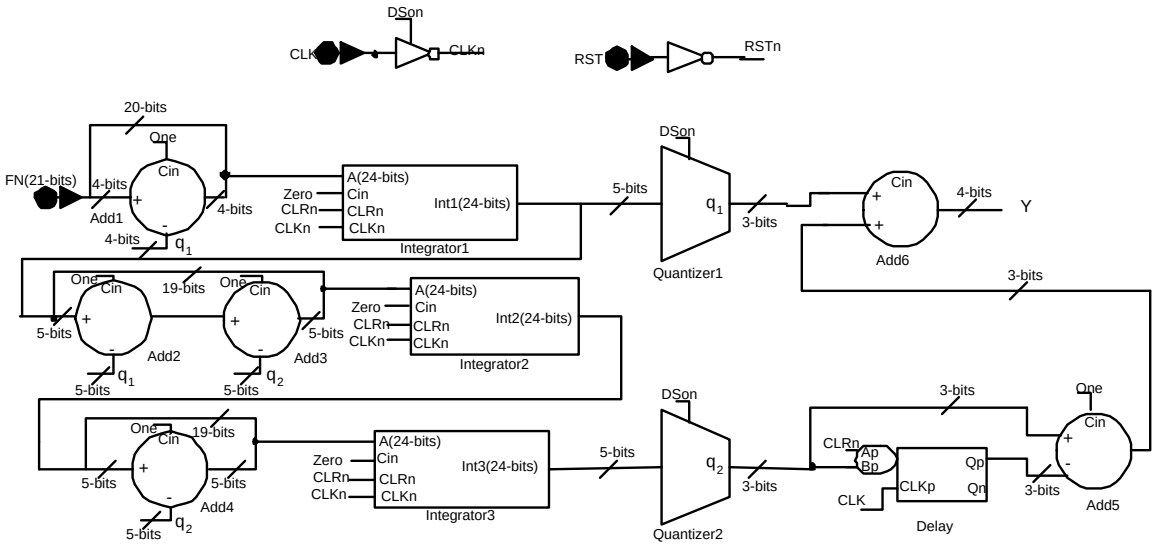


Figure 6.20: Regular MASH 1-2 delta-sigma modulator schematic

The MASH 1-2 delta-sigma modulator structure has two stages with three integrators. For the tapered version, the word widths are 24-bit, 12-bit, and 10-bit for the first, second and last integrator, respectively. The non-tapered version has 24 bits in width for all three integrators.

At the first stage, the MSB of the input signal, FN, is bit extended four times before passing to the adder "Add1". The feedback quantization signal, q1, is also bit extended to 4-bit and passed to this adder.

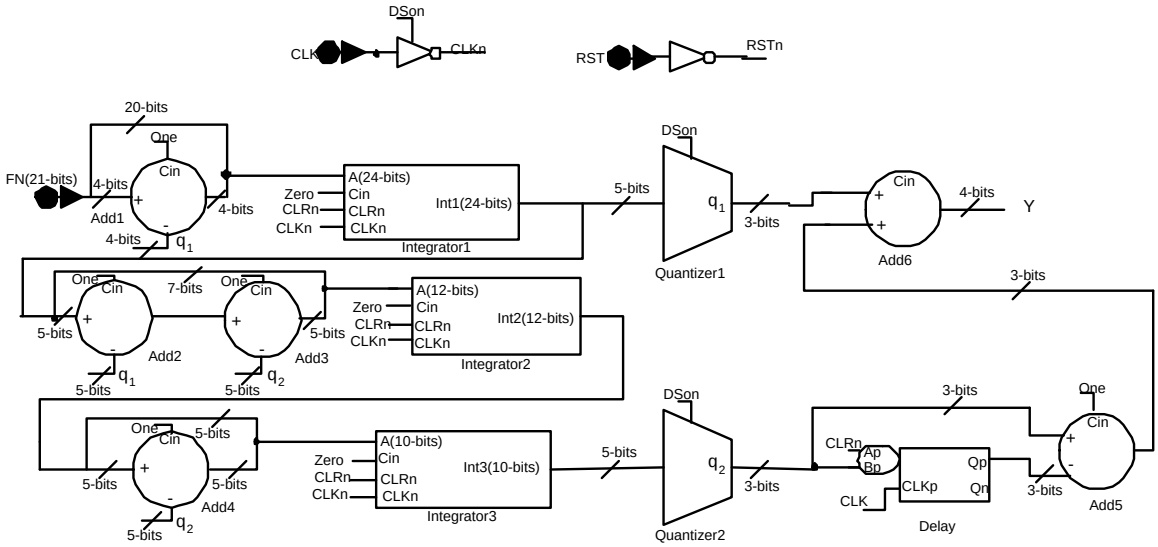


Figure 6.21: Tapered MASH 1-2 delta-sigma modulator schematic

We note that the C_{in} bit is set to HIGH. This indicates that 2's complement arithmetic is used in the adder "Add1". The rest of the FN bits, are not altered by the addition operation; thus, they are passed directly to the input of the first-stage integrator.

For the tapered version, the first-stage integrator passes 5-MSBs (bits 23 to 19) to the adder "Add2", whereas the next seven bits are passed directly to the input of the second-stage integrator. It is noteworthy that the first 12-bit (LSBs) are tapered off. For the non-tapered version, the first stage integrator passes the 5-MSBs (bits 23 to 19) to the adder "Add2", whereas the next 19-bit are passed directly to the input of the second stage integrator. None of the bits is tapered off. Two's complement arithmetic is used within the adder "Add2". The same approach is applied to the second-stage and third-stage of the integrator.

In the tapered version, the next block is an 8-level 5-bit quantizer. The quantizer "Quantizer1" takes 5-MSBs from the first integrator output (bits 23 to 19); the quantizer "Quantizer2" takes 5-MSBs from the third integrator output(bits 9 to 5). For the non-tapered version, the quantizer "Quantizer1" takes 5-MSBs from the first integrator output (bits 23 to 19), and the quantizer "Quantizer2" takes 5-MSBs from the third integrator output (bits 23 to 19).

The signals q_1 and q_2 are fed back into the integrator stages (Figure 6.21 and Figure 6.20). The two signals are combined to obtain the fractional part of the dividing ratio.

6.5.2.2 Experimental Results

The same procedure in Section 6.5.1.2 has been followed. We used the MASH frequency synthesizer from Chapter 5 in the bypass mode, and both the tapered and non-tapered architectures were implemented and simulated with Verilog with the 3-bit output stream that was stored in an HP8180A data generator. To evaluate the performance of the tapered architecture a series of experiments were conducted. First, the Verilog output was compared to the Simulink output to make sure that each block was functioning properly. Next, the VCO output spectrum and phase noise were measured for both the tapered and non-tapered structures. Measurements were conducted on a fractional channel $\frac{4}{65}$ which corresponded to a 400KHz spacing with a 6.5 MHz reference frequency. Figure 6.22 models the output VCO spectrum from a Hewlett-Packard E4407B spectrum analyzer. Figure 6.23 illustrates the phase noise spectrum taken from an HP4352B PLL/VCO analyzer. The results that are shown here are for the tapered version. Figure 6.24 shows the VCO output spectrum for both the tapered and non-tapered version. We can see that there is a reduction of about 15 dB in the fractional spur level at the expense of a higher noise floor. This may be explained by an internal dithering characteristic of the proposed tapered structure.

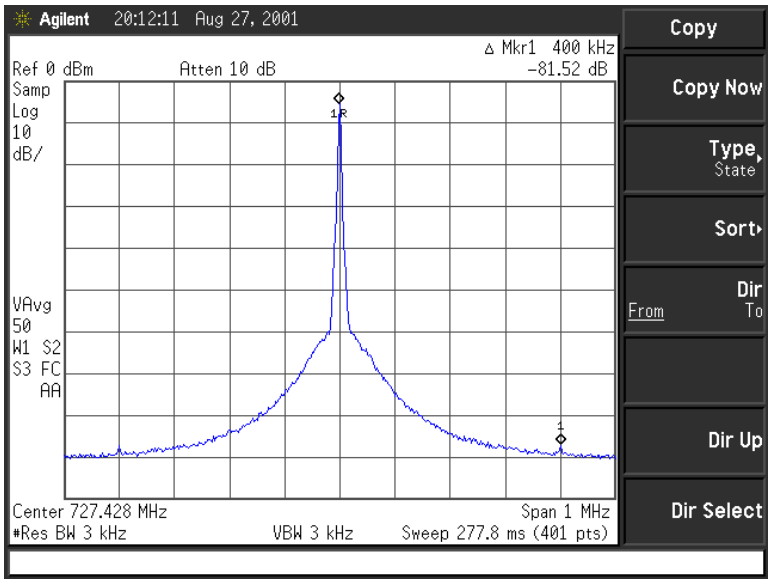


Figure 6.22: VCO output spectrum for tapered MASH 1-2 delta-sigma modulator

To calculate the power saving in the delta-sigma modulator and the total saving in the fre-

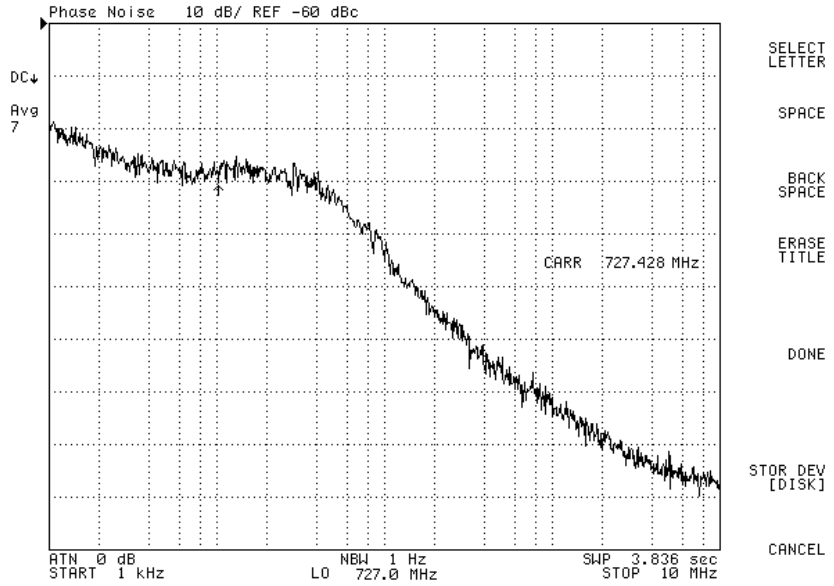


Figure 6.23: Output phase noise for tapered MASH 1-2 delta-sigma modulator

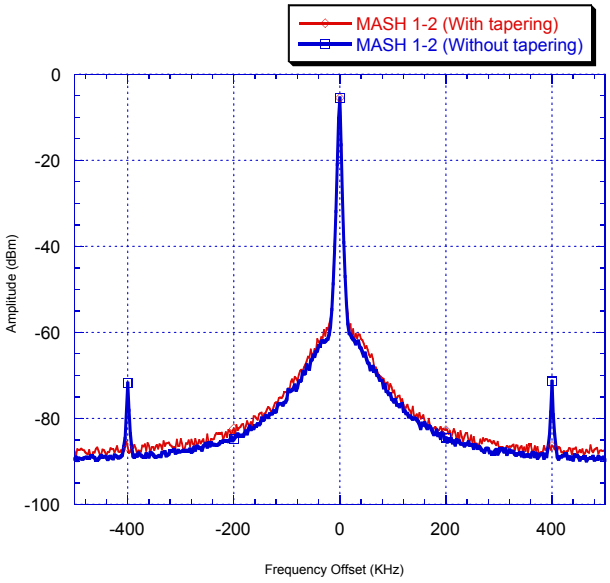


Figure 6.24: Output spectrum for tapered and non-tapered MASH 1-2 delta-sigma modulator

quency synthesizer, we can assume that the total capacitance of the accumulators is directly proportional to the number of bits, as well as the power dissipation. If we calculate the total number of bits in the accumulator in both designs, we obtain 72-bit for the non-tapered, and 46-bit for the tapered version. This translates into a 36% power saving in the delta-sigma modulator, or a 4.2% saving in the whole frequency synthesizer. The current distribution is displayed in Figure 6.25.

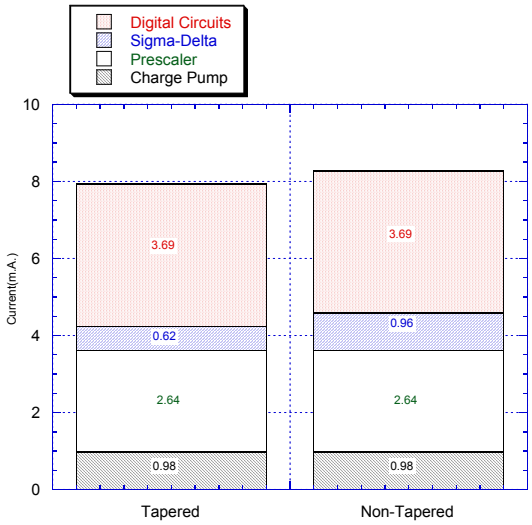


Figure 6.25: Current distribution for tapered and non-tapered MASH 1-2 delta-sigma modulator

6.6 Conclusion

In this chapter, alternate fractional-N frequency synthesizer architectures have been proposed, three different architectures have been presented. The first architecture addressed the spur reduction through the use of the delta-sigma modulator output as a dithering signal. An improvement of 14dB was measured for the third-order modulator at $\frac{1}{65}$ fractional channel, which corresponded to a 100kHz channel-spacing at f_s=6.5MHz. The second architecture targeted the speed and stability issue, as well as the power dissipation, by replacing the delta-sigma block with a pre-calculated ROM. The last architecture deals with both the power dissipation and the spur level by using a proposed tapered architecture. A spur reduction of 15dB was measured for the third-order modulator at a $\frac{4}{65}$ fractional channel, which corresponds to a 400kHz channel-spacing at f_s=6.5MHz. An estimated 36% power reduction for the third-order MASH 1-2 is achieved.

Chapter 7

A Memory-Based Analog to Digital Converter

7.1 Introduction

With the explosive growth of wireless communication systems and portable devices, the power reduction of integrated circuits has become a major issue. In applications such as PCSs (personal communication systems), cellular phones, camcorders, and portable storage devices, low energy dissipation, and in turn, longer battery lifetime, is a must. With the rapid growth of the Internet and information-on-demand, handheld wireless terminals are becoming increasingly popular. With limited energy in a reasonably sized battery, minimum energy dissipation in integrated circuits is a necessity.

Today, many of the communication systems utilize digital signal processing (DSP) to resolve the transmitted information. Therefore, between the received analog signal and DSP system, an analog-to-digital interface is necessary. This interface provides a digitization of the received waveform subject to a sampling rate requirement of the system. Being part of a communication system, the analog-to-digital interface must also adhere to the low power constraint.

The trend to increase the integration level for integrated circuits has forced the analog-to-digital converter interface to reside on the same silicon with large DSP or digital circuits. If the same supply voltage between the analog-to-digital and the digital circuit is shared, the overhead cost for extra DC-DC converters to generate multiple supply voltages is reduced. Therefore, an

analog-to-digital converter operating at the same voltage as the digital circuit is desirable.

With the increased traffic on the Information Superhighway today, large amounts of data are stored in storage devices and accessed frequently. In order to transmit large amounts of data in a short period of time, a high transfer rate in the storage devices is required. This translates directly into a higher data conversion rate in the read channels of magnetic storage devices such as a SCSI hard drive. In the commercial market today, a transfer rate of 100MS/s can be commonly found with resolutions of six to eight bits. However, in order to achieve an even higher transfer rate for some multimedia applications, the speed of the analog-to-digital converter needs to improve.

To achieve the goals of low power, and high speed, we propose a new memory-based analog-to-digital architecture. In this architecture, the last sample is used to predict the current one, resulting in both power dissipation and energy reduction. The low-power dissipation is a vital factor when we consider chip reliability and integrity. The low energy consumption is a critical factor, when we deal with battery operated devices such as PCSs. In addition, this technique may be used to extend the attainable flash converter resolution by pre-calculating the most significant bits.

In this chapter, we will derive an approximate formula for the power dissipation in an analog-to-digital converter, and suggest two figures of merit for both power and speed. The new architecture will be developed, and a high level simulation will be conducted to validate the architecture. After we review some of the recently published work on analog-to-digital converter architectures, we will compare them to the proposed architecture, and then draw some conclusions.

7.2 Power Consumption in an Analog-to-Digital Converter

To achieve our ultimate goal of low-power analog-to-digital converters, we must examine the dependence of power dissipation on both sampling frequency and resolution.

Figure 7.1 represents the architecture of a 1-bit/stage pipelined analog-to-digital converter. Each stage compares the input to a reference, and then amplifies the residue for further resolution by the next stage. A circuit diagram of each stage is also shown in the figure. The two critical, power consuming components of this circuit are the comparators and the sample and hold (S/H) amplifier. The comparator of the first stage must have an n-bit accuracy where n is the number

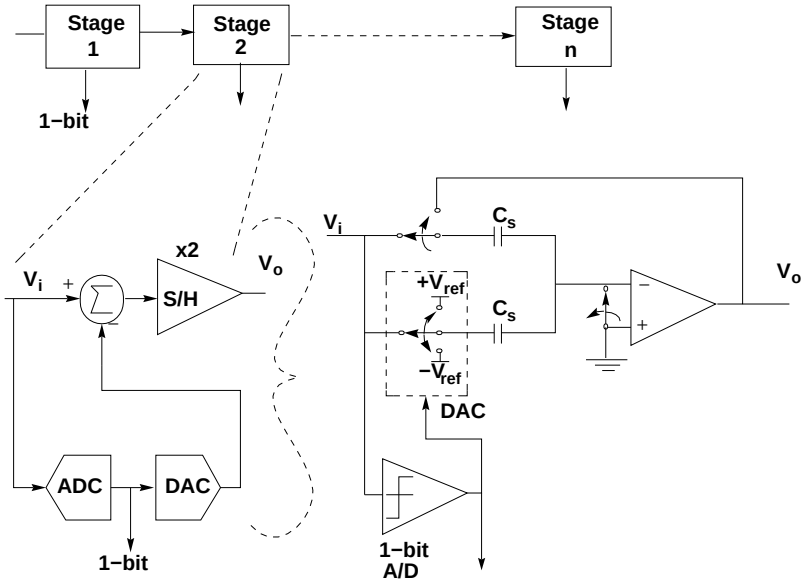


Figure 7.1: 1-bit pipelined analog-to-digital converter

of bits of the analog-to-digital converter. This consumes a large amount of power due to the need for several pre-amplification stages. The requirements of the subsequent comparators are relaxed, progressively, due to inter-stage amplification. However, one way of relaxing the requirements on the comparator is to use digital error correction, whereby each stage resolves additional bits that can be used to correct the errors of the previous stage [56] [57]. In that way, dynamic comparators that have large offsets could suffice and no static power is consumed in the pre-amplification stages. As a result, the main power drain in the pipelined analog-to-digital converter is the S/H opamp.

The S/H opamp must meet the settling time requirement, which is proportional to the operating frequency. The time constant of the opamp is equal to

$$\tau = \frac{C_{tot}}{G_m} f \tag{7.1}$$

where G_m is the equivalent transconductance of the opamp, C_{tot} is the total Capacitance seen at the output of the opamp, and f is the feedback factor, which is equal to the ratio of the feedback capacitor to the total capacitance at the virtual ground.

If we neglect the input capacitance of the opamp, and the other parasitic capacitances, the time constant is

$$\tau = \frac{C_s}{G_m} \tag{7.2}$$

or equivalently,

$$G_m \propto f_s.C_s \tag{7.3}$$

where f_s is the sampling frequency.

This relation determines the power consumption of the opamp, since G_m is directly proportional to the bias current. Hence, the power consumption of the whole analog-to-digital converter is

$$P \cong n.I_{bias}.V_{dd} \propto n.G_m.V_{dd} \propto n.f_s.V_{dd}.C_s \tag{7.4}$$

where the factor n is included to account for the total number of stages. The value of C_s is determined by the required resolution. For an n-bit analog-to-digital converter with full scale voltage of V_{FS}, the SNR is [57]

$$SNR = 10log\left(\frac{V_{FS}^2/2}{\frac{1}{12}.\left(\frac{2.V_{FS}}{2^n}\right)^2 + \frac{k.T}{C_s}}\right) \tag{7.5}$$

where the first term in the denominator represents the quantization noise, and the second term represents the thermal noise (Nyquist sampling is assumed, i.e., all thermal noise lies in the band of interest). Clearly, if the sampling capacitance is not high enough, the thermal noise may dominate the quantization noise, yielding a smaller equivalent number of bits. If kT/C is equal to the quantization noise, a 3dB SNR degradation results. Thus, the value of the capacitor is limited by the noise requirement. Assuming that the full-scale voltage is proportional to V_{dd}, we can deduce from (7.5) that

$$C_s \propto \frac{2^{2n}}{V_{dd}^2} \tag{7.6}$$

Substituting this relation in (7.4), we find that the power consumption of the analog-to-digital converter is related to the dynamic range, the sampling frequency, and the supply through

$$P \propto \frac{n.f_s.2^{2n}}{V_{dd}} \tag{7.7}$$

This expression is valid for a large number of bits (n > 10). For a fewer number of bits, the thermal noise is much smaller than the quantization noise and the lowest possible capacitor is no longer limited by the noise requirement, but by the parasitic capacitors in the circuit [57]. The relation of the power to the sampling frequency and resolution is apparent in Figure 7.2. Although the relation has been deduced for a 1-bit/stage analog-to-digital converter, the same orders of proportionality hold for larger bits/stage [57]. Another factor in power reduction is scaling, where the sampling capacitors are progressively scaled down along the pipeline with the relaxing noise constraint [56]. This method has an appreciable effect for a high resolution analog-to-digital converter where the size of the sampling capacitor is limited by the thermal noise that is allowed.

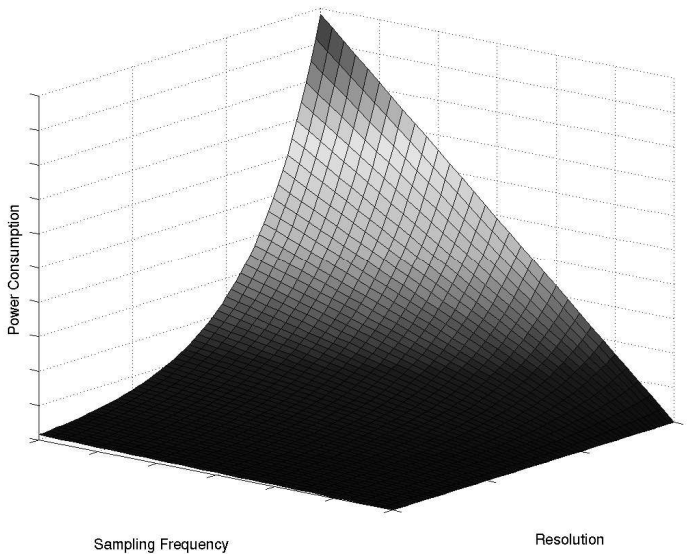


Figure 7.2: Power of pipelined analog-to-digital converter vs. sampling rate and resolution

7.2.1 Power and Speed Figure of Merit

To compare the various analog-to-digital converter designs for both speed and power efficiency, many parameters must be considered.

For the speed figure of merit (SFM) the technology that is adopted has a major role. Therefore,

we may normalize the obtainable speed for a certain design to the cut off frequency of that technology. This relation may be written as

$$SFM = \frac{SR}{f_c}.10^3 \tag{7.8}$$

where SR is the sampling rate, and f_c is the technology cutoff frequency

The multiplication factor "10^3" is included, since the sampling frequency is given in MSPS, while the cut off frequency is given in GHz.

For the power figure of merit (PFM), in addition to the technology role in the power dissipation variation, both the resolution and sampling rate may affect the obtained power dissipation. We can express the power dissipation figure of merit as

$$PFM = \frac{2^N.SR}{P.f_c} \tag{7.9}$$

where N is the total resolution bits, and P is the Power dissipation.

7.3 A New Memory-Based ADC Architecture

Over the last two decades, several analog-to-digital converter architectures have been devised. Among these architectures, the flash analog-to-digital converter is considered to be the fastest one that is available. However, the flash analog-to-digital converter is a large power consumer, and isn't practical for resolutions higher than eight bits. Pipelined analog-to-digital converter is a wise choice when the latency isn't a critical parameter. It has the same throughput as the flash with a considerable lower power dissipation, and a higher attainable resolution. Oversampling analog-to-digital converter is the best choice for low frequency signals such as audio signals, for its power and hardware efficiency, as well as its high dynamic range. But for high frequency signals, oversampling analog-to-digital converter isn't the appropriate choice.

In this section, we investigate the possibility of satisfying the speed, resolution, and power constraints for analog-to-digital converters. In order to achieve this goal, a new memory-based analog-to-digital converter architecture is proposed. This architecture is memory-based because we use the last sample to predict the current one, which results in reducing both the power

and the energy. Analog-to digital converters that use this architecture are capable of converting wide band signals with high sampling rates. However, the high frequency components of these signals should have small amplitudes. In other words, the signal value variation between any two consecutive samples should be limited to a small portion of the full scale. This technique may also be used to extend the attainable flash converter resolution by pre-calculating the most significant bits.

7.3.1 Block Diagram

Figure 7.3 presents this architecture, which uses the Most Significant Bits (MSBs) of the previous sample to predict the current sample MSBs.

As explained in the algorithm flow chart, we carry two comparisons, one with "X" and the other with "X+D". The results of these comparisons are used to predict the current MSBs. Table 7.1 is the truth table for the MUX, which has two controls SL and SH. SL is high when the input signal level is greater than "X", and SH is high when the input signal level is greater than "X+D". This indicates that the maximum allowable change between two successive samples is "D"; this may be used to determine the ratio between the predicted number of bits to the total resolution (M/N).

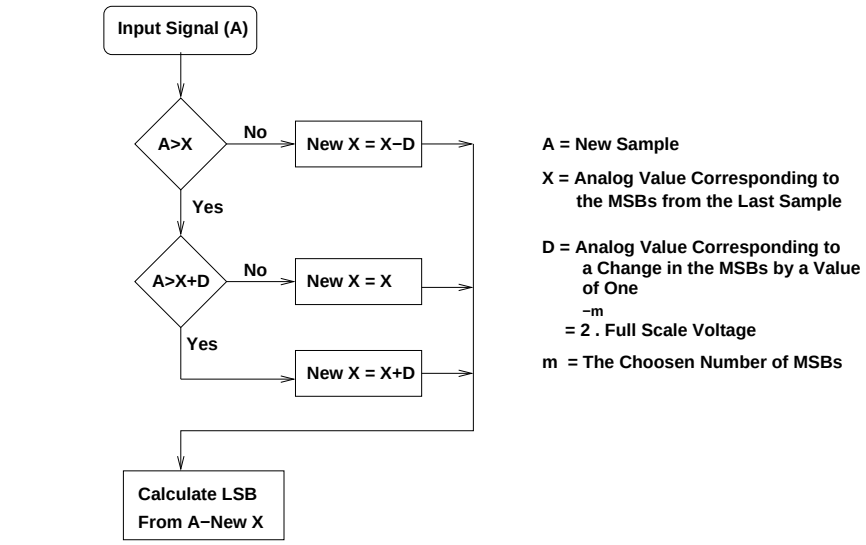
SH	SL	New X
0	0	X-D
0	1	X
1	1	X+D

Table 7.1: Truth table for the MUX in Figure 7.3

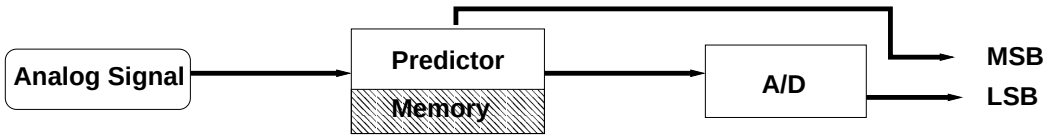
The main advantage of this architecture is the reduction of power and energy dissipation, as well as increasing the attainable resolution. This architecture does not degrade the speed, because we calculate the MSBs in the predictor, whereas we calculate the LSB in the pipelined or flash analog-to-digital converter.

7.3.2 Results

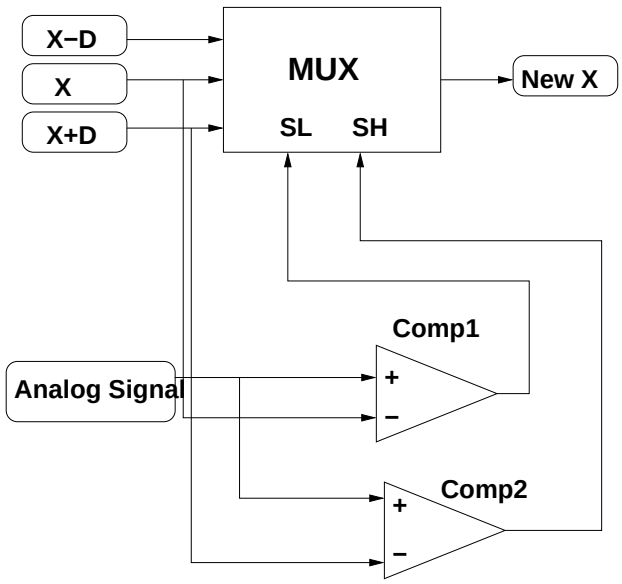
The validity of this algorithm is examined on the architectural level using Matlab and Simulink. Figure 7.4 represents the results of this simulation; Figure 7.4(a), the input signal, Figure 7.4(b),



(a)



(b)



(c)

Figure 7.3: Proposed analog-to-digital (A/D) converter architecture: (a) the algorithm flow chart, (b) the proposed architecture, and (c) the predictor

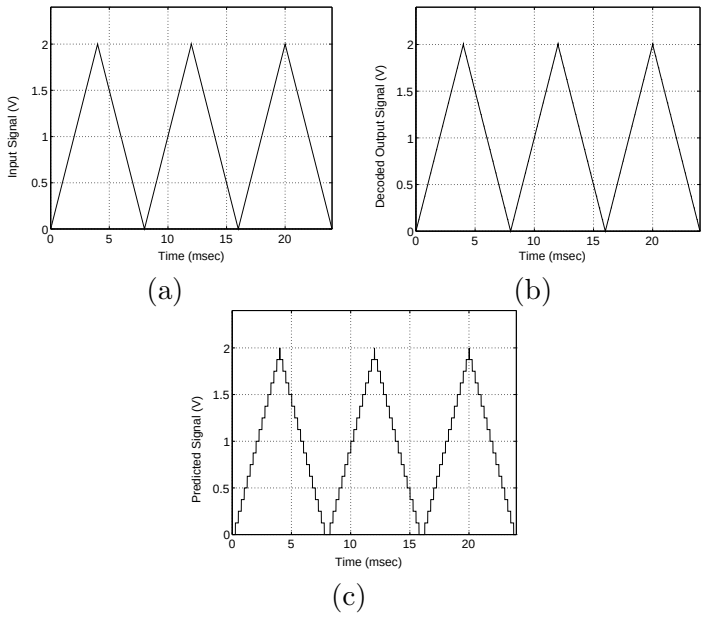


Figure 7.4: Simulink simulation results: (a) input signal, (b) decoded output signal, and (c) predicted signal

the output signal from the analog-to-digital converter after decoding; and Figure 7.4(c), the predictor stored value (i.e., the analog value for the MSB calculated by the predictor).

To check the stability of this algorithm, we use an input signal with a nonzero start, and the simulation is carried with a zero value in the predictor memory. Figure 7.5 presents the simulation results. From Figure 7.5(c), it is clear that the predictor value increase linearly, until it captures the correct signal value. Adaptive methods may be used to decrease the time that is required for the predictor to capture the signal MSB.

Finally, the simulation results for sinusoidal input are presented in Figure 7.6

7.3.3 Power Saving

The major issues with portable communication systems are the power and energy dissipation. To find out the power saving when we use the proposed architecture in Section 7.3 we can compare the hardware complexity with the currently used architectures such as flash and pipelined. Table 7.2 summarizes the hardware complexity in these architectures when they used for the whole analog-to-digital converter or when they are modified by the architecture in Section 7.3.

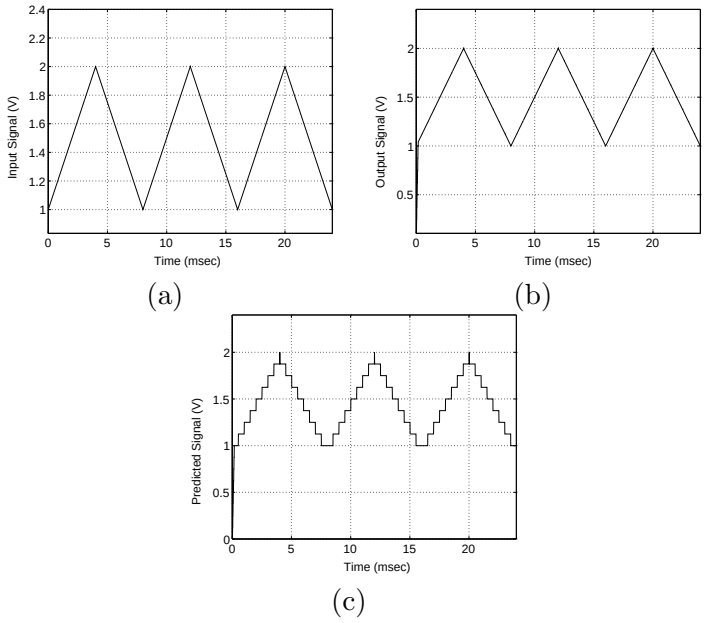


Figure 7.5: Algorithm stability results: (a) input signal, (b) decoded output signal, and (c) predicted signal

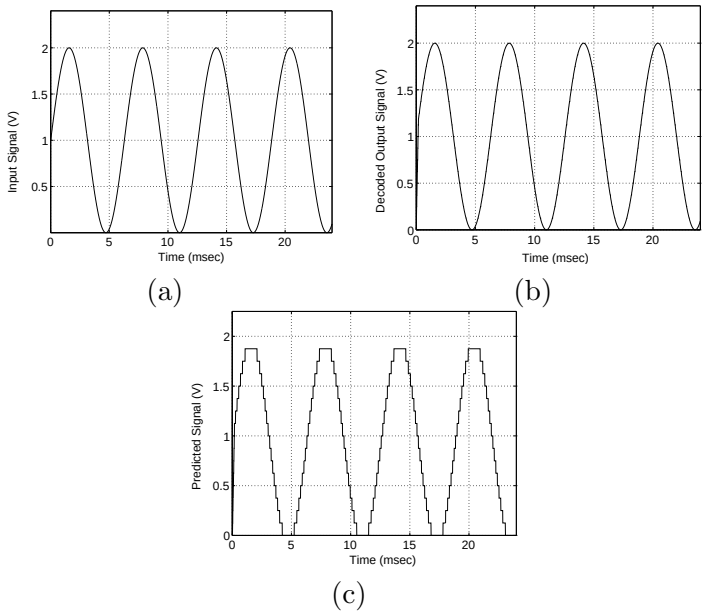


Figure 7.6: Simulink simulation results with sinusoidal input: (a) input signal, (b) decoded output signal, and (c) predicted signal

Architecture	Hardware Complexity
Flash	$2^N - 1$ [58]
Modified Flash	$2 + 2^{N-M}$
Pipelined	$\frac{N}{K}(2^K + a)$ [59]
Modified Pipelined	$2 + \frac{N-M}{K}(2^K + a)$

Table 7.2: Hardware requirements for different analog-to-digital converter architectures

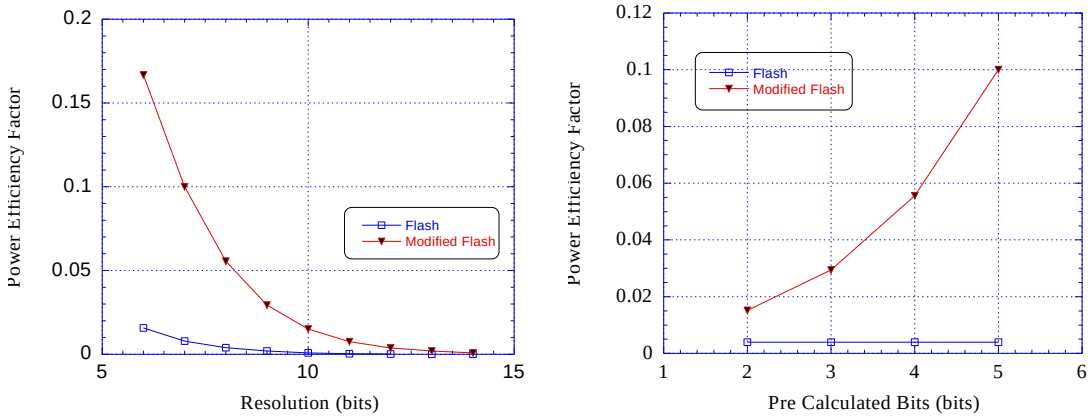


Figure 7.7: Power efficiency comparison between flash and modified flash architectures: (a) different resolutions(M=4), and (b) different pre-calculated bits (N=8)

where N is the number of bits of overall resolution, K is the number of bits per stage, M is the number of predicted MSBs, and a is the ratio of stage hardware to comparator hardware.

Figures 7.7, and 7.8 represent the power efficiency factor for the different architectures in Table 7.2. The power efficiency factor is considered to be equal to the reciprocal of the hardware factor, which is directly proportional to the power dissipation. The factor "a" in the pipelined architecture is taken to equal 0.5.

From these results, we can see that a better performance is obtained from the new architecture when the ratio (M/N) increases. This depends on the nature of the signal itself (i.e., how fast its variation is).

One of the possible modifications to this technique is to use programmable pre-calculated bits, and programmable resolution analog-to-digital converter to match the signal under conversion. Recent work in programmable resolution analog-to-digital converter is published by Texas Instruments [60]

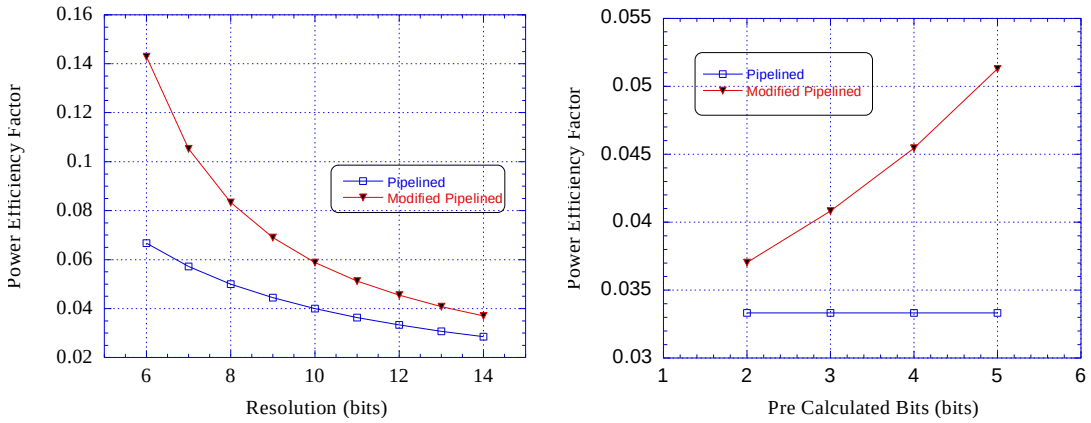


Figure 7.8: Power efficiency comparison between pipelined and modified pipelined architectures: (a) different resolutions(M=4), and (b) different pre-calculated bits (N=8)

7.3.4 Power Saving Comparison with Recently Published Work

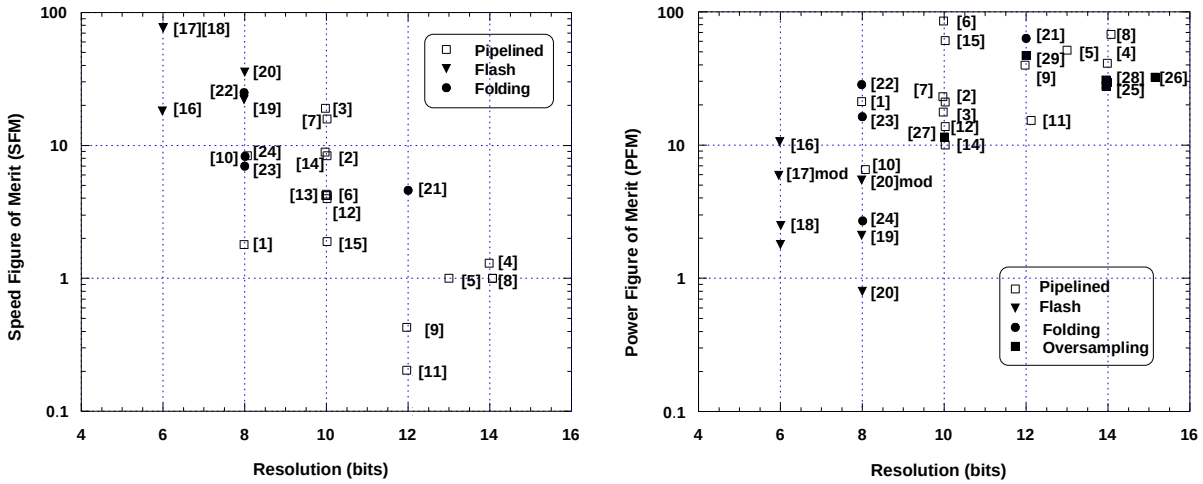
Figure 7.9(a) presents SFM for recently published analog-to-digital converter using different architectures; Figure 7.9(b), the power figure of merit (PFM) for these architectures; and Table 7.3, the available data.

We can conclude that at a low resolution (fewer than 8 bits), flash analog-to-digital converter is the fastest available design. However, from the power dissipation perspective, it has the worst performance due to its high power dissipation. Pipelined analog-to-digital converter is a good candidate for higher resolution; performs well in both speed and power dissipation, provided that its associated latency is accepted. At high resolution, oversampling is a good choice from the power point of view. However, due to the oversampling operation, it can be used only with low frequency signals.

To measure the effectiveness of the proposed memory-based architecture, we used it with two architectures [61], [62]. The choice of these architectures was based on the fact that they have the best SFM at a 6-bit resolution and 8-bit resolution, respectively, but they have the worst PFM. The pre-calculated bits are taken to equal 3-bit in the 8-bit architecture, and 2-bit in the 6-bit architecture. The pre-calculated bits may be increased according to the statistical properties of the analog signal. From Figure7.9(b), the modified architecture is showing an improvement factor of 7.5 compared with [62], and 3.5 compared with [61].

Ref.	Type	SR (MHz)	N (Bits)	Technology	PSV (V)	Power (W)	SFM	PFM
1. [63]	Pipelined	20	8	0.5 μm CMOS	2.4	22m	1.82	21.16
2. [64]	Pipelined	40	10	4.5 GHz BiCMOS	5	0.395	8.89	23.04
3. [65]	Pipelined	95	10	1 μm BiCMOS	5	1.1	19.00	17.69
4. [66]	Pipelined	2.5	14	2 μm BiCMOS	5	0.5	1.25	40.96
5. [67]	Pipelined	5	13	1.2 μm CMOS	5	0.166	1.04	51.41
6. [68]	Pipelined	20	10	1.2 μm CMOS	5	0.05	4.17	85.33
7. [69]	Pipelined	50	10	3 GHz Bipolar	5	0.75	16	21.8
8. [70]	Pipelined	10	14	0.8 μm CMOS	5	0.235	1.0	69.72
9. [71]	Pipelined	4	12	0.8 μm CMOS	4	0.045	0.40	36.40
10. [72]	Pipelined	50	8	0.9 μm CMOS	5	0.25	8.34	8.54
11. [73]	Pipelined	1	12	1.2 μm CMOS	2	60m	0.20	14.22
12. [74]	Pipelined	20	10	1 μm CMOS	5	0.3	4.0	13.6
13. [56]	Pipelined	20	10	1.2 μm CMOS	3.3	35m	4.16	121.9
14. [75]	Pipelined	100	10	12 GHz Bipolar	5	0.8	8.34	10.66
15. [76]	Pipelined	20	10	0.8 μm CMOS	5	30m	2.00	68.26
16. [77]	Flash	200	6	0.5 μm CMOS	3	0.11	18.18	10.58
17. [61]	Flash	1000	6	13 GHz Bipolar	5	2.8	76.92	1.76
18. [78]	Flash	2000	6	26 GHz Bipolar	5	2	76.92	2.46
19. [79]	Flash	400	8	18 GHz Bipolar	5	2.7	22.22	2.11
20. [62]	Flash	250	8	7 GHz Bipolar	5	12	35.71	0.76
21. [80]	Folding	60	12	1 μm BiCMOS	5	0.3	4.62	63.02
22. [81]	Folding	125	8	1 μm CMOS	5	0.225	25.00	28.44
23. [82]	Folding	70	8	0.8 μm CMOS	5	0.11	7.00	16.29
24. [83]	Folding	100	8	12 GHz Bipolar	5	0.8	8.33	2.67
25. [84]	Oversampling	0.5	14	1.2 μm CMOS	5	58m	0.10	29.43
26. [85]	Oversampling	0.2	15	1.2 μm CMOS	5	40m	0.04	34.14
27. [86]	Oversampling	0.384	10	0.5 μm CMOS	2	1.56m	0.04	22.92
28. [87]	Oversampling	0.156	14	1.2 μm CMOS	5	15m	0.04	35.5
29. [88]	Oversampling	0.016	12	1.2 μm CMOS	2	0.34m	0.00	40.16

Table 7.3: Figure of merit for recently published analog-to-digital converters



(a) (b)

Figure 7.9: Figure of merit For different architectures: (a) speed, and (b) power

7.3.5 Conclusion

The efficient use of previous signal samples reduced the power dissipation in the analog-to-digital converter. A new architecture was devised. It is a memory-based; in that is, the current sample is predicted from the previous sample value. The high level simulations prove the functionality of the new architecture, and the power dissipation reduction has been demonstrated. A power reduction of more than 86% is obtained, when the architecture is implemented with an 8-bit flash analog-to-digital converter.

Chapter 8

Discussion, Conclusions, and Future Work

8.1 Discussion

The design and simulation of a fractional-N frequency synthesizer and simulation are complex tasks, which involve many fields such as control theory (PLL), micro-electronic (low-power CMOS design), ASIC design (PFD, DSM) , high frequency components (VCO, frequency divider), and system simulations.

The frequency synthesizer implementation has evolved due to the reduction of device geometry and the addition of more digital signal processing. For example, this has been achieved by using the delta-sigma modulator in the fractional-N frequency synthesizer. For now, there are few fractional-N frequency synthesizers on the market which are based on delta-sigma modulation, but this will change in the near future. Many companies such as Synergy Microwave, and Philsar are developing their own products [35].

In this competitive context, we have attempted to clarify the concept and choices available for the design of a delta-sigma based fractional-N frequency synthesizer. In addition, we have calculated system parameters, simulated a MASH fractional-N PLL with a high level abstract model in Verilog, and shown how it can facilitate a dual-mode/multi-mode design.

Before we conclude this work, we would like to summarize the choices that are available to the designer of a single-mode/dual-mode fractional-N frequency synthesizer, based on the delta-sigma

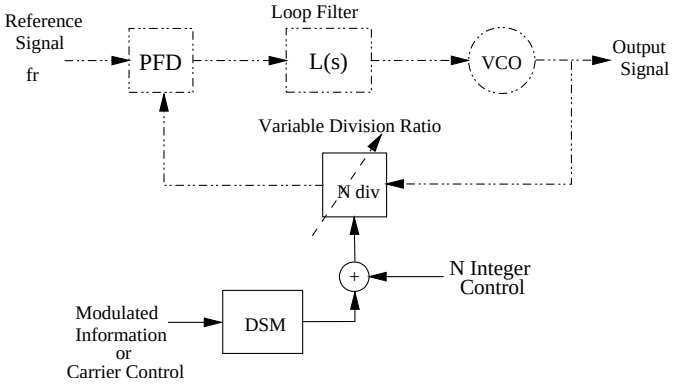


Figure 8.1: Frequency synthesizer using multi-modulus divider

modulation in Figure 8.1.

First, the designer may consider the variable divider architecture. In general, for fractional-N frequency synthesizers, we can choose between a dual-modulus divider (DMD) and a multi-modulus divider (MMD). The DMD design is much simpler than the MMD. However, it presents several drawbacks. The first problem of the DMD is that it needs only one control bit. This limits the choice of the DSM architecture to a single-stage high-order DSM, which requires scaling factors to ensure the stability of the DSM architecture. The DMD is not a good fit for multi-mode operation, which is the current trend in wireless communications design. Finally, the output frequency range of this method is limited to the reference frequency span.

If we use a multiple-bit output DSM (such as the MASH 1-1-1 architecture) with the dual-modulus divider, it can be followed by a second DSM to concentrate the multi-bit output from the first DSM to a single-bit output [89]. The second DSM is referred to as a DSM concentrator. However, the noise transfer function at the output is dominated at low frequencies by the second DSM. Therefore, the concentration of the multi-bit output from the MASH 1-1-1 implies the requirement of third-order noise shaping in the DSM concentrator so that the noise shaping from the first DSM is not degraded. In other words, when the MASH is followed by a DSM concentrator, there is a redundancy of the DSM and an increased difficulty in the design of the concentrator, which must be a single-loop high-order DSM.

The other available divider is the multi-modulus divider such as the one introduced by Perrott [14]. His divider has a control word of 6-bits to select each integer division ratio in the range between 64 and 127. In this technique, it is necessary that we have all the division ratios required

to cover the desired output range.

The design of the MMD is more complicated than that of the DMD, but a major advantage is that we can use a multi-bit output DSM to control the required channel. This provides more flexibility in the selection of the DSM.

The second step is to choose the proper DSM to control the variable divider. Even though some recent fractional-N PLLs are still based on a single-stage DSM, we believe that it is preferable to consider a MASH structure to control the fractional value of the division ratio. A MASH structure offers unconditional stability. We also believe that the use of a DSM as a concentrator should be avoided to limit the complexity of design; complexity and a solution that is based on a MMD is preferred to a DMD.

The cascade of first-order DSMs (digital accumulators) in a MASH structure is the easiest implementation of the DSM to control the fractional division ratio. This stable structure is easy to pipeline, but dithering is necessary for the DC inputs due to the idle tones in the first-order DSM. The excursion range ΔN is small which renders this type of DSM well suited for multi-mode frequency synthesizers.

The MASH, based on combining both first-order and second-order DSMs, is a more robust alternative to the MASH DSM, based on first-order only for which idle tones are a concern. However, the introduction of pipelining inside each second-order DSM is difficult, and poles and scaling factors are required to obtain a stable DSM.

Multi-Mode Frequency Synthesizer

The use of a multi-modulus divider such as the one reported by Perrot in [14] may ease the operation of the frequency synthesizer for a multi-mode operation. The division ratios in the divider are selected so that the excursion ΔN of the division ratio is limited to a few integer values around the range of interest for each mode . For example, if we want to design a frequency synthesizer for both GSM and DECT the required ΔN and N can be calculated as follows: For GSM, the integers values of N= 71, 72, 73 and 74 are selected with $\Delta N = 4$ to generate the fractional values in the range [71, 74], if a reference frequency, f_r of 13MHz to cover the range from 925MHz to 960MHz is assumed. For DECT, the integers values of N= 90, 91 and 92 are selected with $\Delta N = 3$ to generate the fractional values in the range [90, 92], if f_r of 18*1.152MHz=20.736MHz to cover the range from 1880MHz to 1900MHz is assumed.

For a given value of N, the output frequency bandwidth of the PLL is $BW_{out} = [N.f_r, (N + 1).f_r]$. In some cases, it is not possible to cover the whole spectrum with a single value of N (i.e., the desired output spectrum is larger than BW_{out}). Therefore, we must choose several values for N (i.e., N, N+1, N+2, ..., N+p , where $64 + \Delta N < N < 127 - \Delta N$) so that the output spectrum is included in the summation $BW_{out}|_N + BW_{out}|_{N+1} + ... + BW_{out}|_{N+p}$. It is convenient if we can select different central values of N, independent of the variation in the range ΔN that is introduced by the DSM. If some of the division ratios that are selected are integers, it can also be advantageous to de-select the delta-sigma modulator, and set it in an idle mode to save power.

8.2 Conclusions

The design and analysis of a fractional-N frequency synthesizers have been detailed in this thesis. The frequency synthesizer designs have all been based on the phase-locked loop (PLL) structure. This has led to three new frequency synthesizer structures. The first architecture addresses the spur reduction, the second architecture targets the speed and stability issue, as well as the power dissipation, and the last architecture reduces both the power dissipation and the spur level.

In the theoretical analysis of the DSM, a state representation model is derived in Chapter 3 for different delta-sigma, modulators and used to analyze the stability issue in the modulators. Closed form expressions to predict the phase noise in fractional-N MASH architectures are given in Chapter 4.

In the design of the first frequency synthesizer, a conventional MASH $\Sigma\Delta$ fractional-N PLL was developed. The design was optimized for GSM and GPRS wireless communications standards. We demonstrated that delta-sigma modulation has succeeded in significantly reducing the spurs, but not completely eliminating them. However, the spur levels meet the GSM and GPRS specifications. The power consumption of the architecture has been dominated by the divider. In future designs, lower power can be achieved by using less current in the prescaler. Also, we investigated the effect of using a constant seed. A constant seed did not succeed in eliminating the spurs as anticipated. To completely eliminate the spurs generated by the fractional-N divider, different architectures were explored.

The first proposed architecture addresses the spur reduction through the use of the sigma-

delta modulator output as a dithering signal. An improvement of 14dB was measured for the third-order modulator at a $\frac{1}{65}$ fractional channel which corresponds to a 100kHz channel-spacing at f_s=6.5MHz. The second architecture targets the speed and stability issue, as well as the power dissipation, by replacing the sigma-delta block with a pre-calculated ROM. The last architecture deals with both the power dissipation and the spur level by using a proposed tapered architecture. A spur reduction of 15dB was measured for the third-order modulator at a $\frac{4}{65}$ fractional channel which corresponds to 400kHz channel-spacing at f_s=6.5MHz. An estimated 36% power reduction for the third order MASH 1-2 was achieved.

Another contribution of this work is a new low-power analog-to-digital converter architecture. This architecture is memory-based: the current sample is predicted from the previous sample value. The high level simulations prove the functionality of the proposed architecture, and the power dissipation reduction has been demonstrated. A power reduction by more than 86% is obtained when implementing an 8-bit flash A/D.

8.3 Future Work

Fractional-N frequency synthesis is the most promising application of delta-sigma modulation in the transmitter. Since the beginning of our research, we have observed a rising interest in the third generation of fractional-N frequency synthesizers, based on delta-sigma modulation, both in Europe and North America.

The main trend in mobile wireless communications is towards a multi-standard solution. We have demonstrated how to use the frequency divider in the frequency synthesizer to achieve this requirement. The phase detector is also well suited for several standards, because it does not depend on the system parameters. In order to obtain a more efficient solution, an efficient solution for the phase reference, VCO, and loop filter needs to be investigated.

During our work, we have focused on the GSM and GPRS standards, especially on the aspects of phase noise and spurious performance. Less attention has been directed to power dissipation. Although power dissipation reduction has been achieved through architectural solutions, more emphasis on circuit level issues is needed in order for our proposed architectures to comply with wireless communication devices that are battery operated.

Appendix A

Theoretical SNR from Linear Model Approximation

The signal to noise ratio (SNR) is a convenient estimate to quantify the noise introduced by the modulator. We present briefly a few concepts used in the calculation of the SNR.

The variance of the signal at the output of the delta sigma modulator σ_{xy}^2 is given by

$$\sigma_{xy}^2 = \int_{-f_B}^{f_B} P_x(f)df = \int_{-f_B}^{f_B} |N_x(f)|^2 \, df.scale \tag{A.1}$$

(The power density spectra $P_x = |N_x(f)|^2$).

The variance of the noise at the output σ_{ey}^2 is given by

$$\sigma_{ey}^2 = \int_{-f_B}^{f_B} P_{ey}(f)df = \int_{-f_B}^{f_B} |N_{ey}(f)|^2 \, df. \tag{A.2}$$

The SNR is given by the ratio σ_{xy}^2 over σ_{ey}^2 as expressed in

$$SNR|_{dB} = 10log_{10}(\frac{\sigma_{xy}^2}{\sigma_{ey}^2}). \tag{A.3}$$

The noise power at the output in the range [0, f_B] is obtained by the integration of the noise power density $2\frac{\sigma_e^2}{f_s} |H_{ntf}|^2$ over the band of interest from 0 to f_B.

The SNR, ratio between the signal power and the noise power is defined as

$$SNR = 10log(\frac{\sigma_{xy}^2}{2\frac{\sigma_{ey}^2}{f_s}\int_0^{f_B}|H_{ntf}|^2\,df}) \tag{A.4}$$

with f_s the sampling frequency, f_B the highest frequency component of the input signal with $f_B \ll \frac{f_s}{2}$.

It is difficult to integrate over f a function of the form $sin^N(f)$[1] present in the expression of the noise power ($2\frac{\sigma_{ey}^2}{f_s}\int_0^{f_B}|H_{ntf}|^2\,df$). An approximation of $sin^N(f)$ can be obtained as f_B is small compared to the oversampled sampling frequency ($f_B \ll \frac{f_s}{2}$). The limited development of the $sin(x)$ function gives $sin(x) \approx xforx \to 0$.

For the first order DSM the expression of H_{ntf} is rewritten as

$$|H_{hntf}| = 2sin(\frac{\pi f}{f_s}) \approx 2(\frac{\pi f}{f_s}) \tag{A.5}$$

The replacement of H_{ntf} from (A.5) into (A.4) leads to the approximate SNR for a first order DSM given by

$$\begin{aligned} SNR &\approx 10log(\frac{\sigma_{xy}^2}{2\frac{\sigma_{ey}^2}{f_s}\int_0^{f_B}\left|\frac{2\pi f}{f_s}\right|^2 df}) \\ &\approx 10log(\frac{\sigma_{xy}^2}{2\sigma_{ey}^2\frac{\pi^2}{3}(\frac{2f_B}{f_s})^3}) \end{aligned} \tag{A.6}$$

To avoid saturation of the DSM, the input amplitude should be kept smaller than $\frac{\Delta}{2}$. When the quantization noise variance σ_{ey}^2 is fixed, the only way to improve the SNR is to increase the oversampling ratio either by reducing f_B or by increasing f_s, when we consider a first-order DSM.

The expression of the SNR for higher order DSM is obtained in a similar manner. For example, if we consider a sinusoidal input of amplitude 1, a 2-level quantizer and a uniform white noise

[1]For the first order N=2

source for the quantization noise, the expression of the SNR becomes:

$$\begin{aligned} SNR|_{dB} &= 10log_{10}(\frac{0.5scale^2}{\frac{1}{12}\int_0^{\frac{2f_B}{f_s}} |H_{ntf}|^2 \, df}) \\ &\approx 10log_{10}(\frac{6.scale^2}{\frac{\pi^{2N}}{2N+1}(\frac{2f_B}{f_s})^{2N+1}}) \end{aligned} \tag{A.7}$$

Figure A.1 shows the theoretical signal to noise ratio for several orders versus the associated scaling factor.

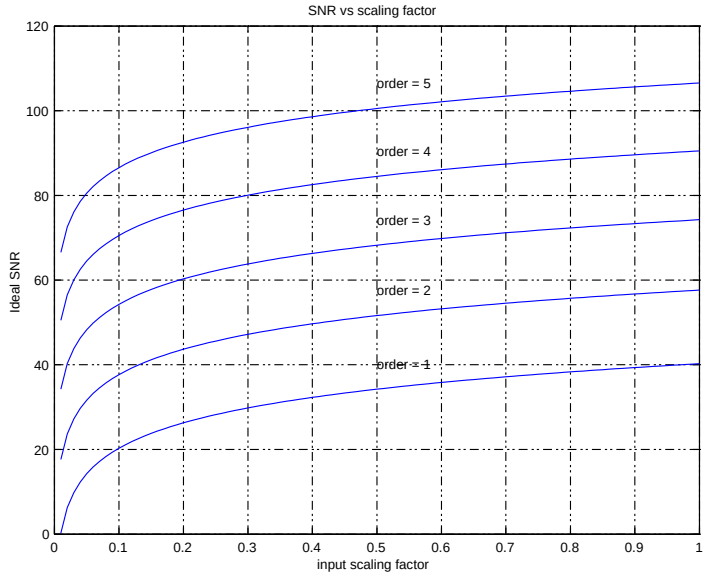


Figure A.1: SNR vs. input scaling factor, for an oversampling ratio of 18 and DSM of several orders

Appendix B

Serial Interface Programming

The serial control hardware input consists of a standard 3-wire serial port interface bus, comprised of DATA, CLK and STROBE signals. These signals are used to input 24-bit control words to the chip. The control words contain information for programming the synthesizer, according to the protocol described in this appendix.

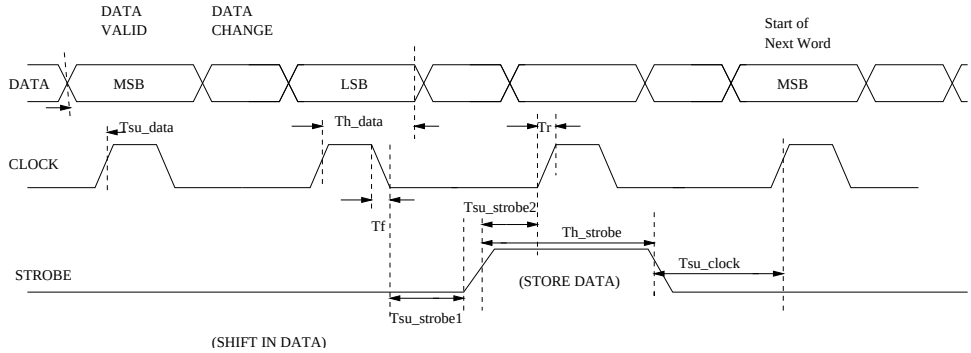


Figure B.1: Serial programming timing

Figure B.1 describes the timing diagram for the serial input. When STROBE is low, data present on the DATA line is shifted into the integrated circuits (IC) serial register on the positive edges of the CLK signal. When STROBE goes high, data present in the serial register is latched and remains stable for any further clock cycles as long as STROBE remains high. Depending upon address bits formatted into each control word, the other data in the control word is routed into different working registers in the IC. Data is entered into the serial register in MSB first format.

At power up, the IC working Registers shall be in a default state (according to the tables described in this appendix) and shall not change until new control data is clocked in on the serial bus.

	MSB																							LSB
	FIRST IN																							LAST IN
BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Table B.1: Data definition

BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	A	FN																						
DEF	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
FN	Fractional division ratio. Default set to 2/65 fractional ratio. Program 23 bits from 24 bits (LSB not programmed and set to 0, A=FN/2)																							
A	A word select																							

Table B.2: "A" word (Delta-sigma input)

BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Address				Not used				Seed				NMU									CTL		SU
DEF	1	0	0	0	X	X	X	X	0	0	1	1	0	0	1	0	0	1	0	1	1	1	0	1
Address	B word select																							
SED	Seed of delta-sigma. This number is decoded into a 16 bits number (2^{16}) and added to FN																							
NMU	Main divider division ratio (Default=75 → A=3, B=9 when the prescaler division ratio is 8)																							
CTL	Mode control for digital compensation scheme: "00"=external bypass, "01"=accumulator, "10"=2^{nd} order delta-sigma, and "11"=3^{rd} order delta-sigma																							
SU	Main loop speed up mode: "0"=disable, "1"=enable																							

Table B.3: "B" word (Main loop update)

BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Address				Not used						RD		PRD		P1	SD	PB	CPM					MP	PE
DEF	1	0	0	1	X	X	X	X	X	X	0	0	0	0	1	0	1	1	1	0	0	X	1	1

Address	C word select
CPM	Main charge pump Current ratio setting. See Table B.7
MP	Main prescaler setting: “1”=8/9, and “0”=16/17
RD	Main reference divider setting: “00”=divide-by-1, “01” or “10”=divide-by-2, and “11”=divide-by-4
P1	Main charge pump DC power: “0”=power down, and “1”=power up
SD	Speedup charge control: “0”=software control, and “1”=STRB pin control
PE	Main prescaler DC power: “0”=power down, and “1”=power up
PB	Reference input buffer amplifier power up/down: “1”=power up, and “0”=Power down
PRD	Main PFD reset delay: “00”=6ns, “01”=8ns, “10”=10ns, and “11”=12ns

Table B.4: “C” word (Main loop setup)

BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Address					TE	TG	HM									TM							
DEF	1	0	1	0	X	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0

Address	D word select
TM	Counter value for speedup mode (default=100μs $\rightarrow$ TM=1300 for 13MHz reference)
HM	Hold main loop in speedup mode: HM=“1”=forever, and HM=“0”=use timer “TM”
TE	Toggle enable: “1”=Enable toggle mode, and “0”=Use Main PFD lock detector LD
TG	Toggle mode. If “TE” = “Toggle mode”, and “TG” = “1” then LD pin puts out a logic high state, if “Tg”$\neq$“Toggle mode” then LD pin puts out a logic low state. If the “TE” bit is not set to “1” then the “TG” bit is ignored.

Table B.5: “D” word (Main loop setup 2)

BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Address				Test mode																			
DEF	1	1	1	0	X	X	X	X	X	X	X	X	X	1	1	X	X	X	X	0	0	X	X	X

ADDRESS	E word select
E[4]	If E[4]=1, external seed value to delta-sigma is written through the DATA pin. If E[4]=0, external seed value from DATA pin is inhibited
E[3]	If E[3]=1, reset the delta-sigma each time a new channel is selected. If E[3]=0, reset delta-sigma only on power up

Table B.6: “E” word (Test mode word)

BIT		I_{PHP}	BIT		I_{PHPSU}
6	5		4	3	
0	0	$16xI_{SET}$	0	0	$64xI_{SET}$
0	1	$12xI_{SET}$	0	1	$48xI_{SET}$
1	0	$8xI_{SET}$	1	0	$32xI_{SET}$
1	1	$4xI_{SET}$	1	1	$16xI_{SET}$

Table B.7: Charge pump current ratio (I_{SET}=V_{SET}/R_{SET}) bias current for charge pumps

#	Test Name	Test Description	Test Vector F[9:0]
1	NORMAL MODE	Regular operating mode	000xx 01000
2	RESET MODE	Software RESET	1xxxx xxxxx
3	LD	Directs internal LD net to LD_OUT pin	0xxxx 01000
4	M_IN	Directs Main Prescalar Output to TEST PIN	000xx x0000
5	M_REF_DIV	Directs Main Ref Divided Output to the TEST PIN	0xxxx x0001
6	M_CNTB	Directs Main B Counter (6 bits) Output to TEST PIN	0xxxx x0010
8	M_CNTA	Directs Main A Counter (3 bits) Output to TEST PIN	0xxxx x0011
9	M_LD	Directs Main LD output to TEST PIN	0xxxx x0100
10	M_UP	Directs Main PFD UP output to TEST PIN	0xxxx x0101
11	M_DN	Directs Main PFD DN output to TEST PIN	0xxxx x0110
12	M_SPU_EN	Directs MAIN Speed Up enable signal to TEST PIN	0xxxx x0111
13	TEST_PIN_HIGH	Sets the TEST PIN to high to set voltage levels during DC test	0xxxx x1010
14	TEST_PIN_LOW	Sets the TEST PIN to low to set voltage levels during DC test	0xxxx x1011
15	REF_IN	Directs Ref Output to the TEST PIN	0xxxx x1001
16	MSPU_PULSE	Directs Main Loop Speedup Enable Pulse to the TEST PIN	0xxxx x11x0
17	M_INSEL	Allows override of Main prescalar and uses DATA pin signal injected into main counter	010xx xxxxx
18	REF_SEL	Allows override of Main Ref clock by DATA pin signal.	011xx xxxxx
19	M_LDSEL	Allows input from the DATA pin to test Main LKDET circuit which includes the pulse filter and the delay counter to show that it's in lock.	0xxxx 11000
20	CPUMP_NORM_BOTH	Allows all pumps to be in their normal operating state and in both up and down pumping mode. This allows ability to test current matching	0xx11 11110
21	CPUMP_NORM_UP	Allows all pumps to be in their normal operating state and up pump mode.	0xx01 11110
22	CPUMP_NORM_DN	Allows all pumps to be in their normal operating state and down pump mode	0xx10 11110

Table B.8: Different test modes

#	Test Name	Test Description	Test Vector F[9:0]
23	CPUMP_NORM_Z	Allows all pumps to be in their normal operating state and high Impedance. This allows ability to test CPUMP leakage.	0xx00 11110
24	CPUMP_SPU_BOTH	Allows main pump to be in speed up operating state and in both up and down pumping mode. This allows ability to test current matching	0xx11 11111
25	CPUMP_SPU_UP	Allows main pump to be in speed up operating state and up pump mode.	0xx01 11111
26	CPUMP_SPU_DN	Allows main pump to be in speed up operating state and down pump mode	0xx10 11111
27	CPUMP_SPU_Z	Allows main pump to be in speed up operating state and high Impedance. This allows ability to test CPUMP leakage.	0xx00 11111
28	TST_SD_BIT0	Allows bit0 of delta-sigma output to be routed to the TEST PIN	0xxxxx 01101
	Bits other than F[9:0] are used in the following test modes		
50	PFD_R_SEL	Allows bypassing main loop PFD reference signal by bit F< 10 > and using DATA pin input as the reference signal for main loop PFD	F< 10 > = 1 (enable)
52	SD_OUT_SEL	Allows selection of either external data (through pins SD_BIT0, SD_BIT1, and SD_BIT2) or an n^{th} order delta-sigma output (where n=1,2,3)	B< 2 : 1 > = 00:bypass SD by SD_BP 01: accumulator 10: second order SD 11: third order SD
53	SD_RESET	Allows the delta-sigma modulator to be reset either whenever channel switches, or only on power-up.	E< 3 > = 0 (reset on power-up only)
54	SD_EXT_SEED	Allows an external dynamic seed to be fed into the delta-sigma.	E¡4¿ = 1 (enable)

Table B.8 cont.: Different test modes

Numerator	**Binary Equivalent (24 bits)**
1	000000111111000000111111
2	000001111110000001111110
3	000010111101000010111101
4	000011111100000011111100
5	000100111011000100111011
6	000101111010000101111010
7	000110111001000110111001
8	000111111000000111111000
9	001000110111001000110111
10	001001110110001001110110
11	001010110101001010110101
12	001011110100001011110100

Table B.9: Fractional channel number, denominator is 65

Numerator	Binary Equivalent (24 bits)
13	001100110011001100110011
14	001101110010001101110010
15	001110110001001110110001
16	001111110000001111110000
17	010000101111010000101111
18	010001101110010001101110
19	010010101101010010101101
20	010011101100010011101100
21	010100101011010100101011
22	010101101010010101101010
23	010110101001010110101001
24	010111101000010111101000
25	011000100111011000100111
26	011001100110011001100110
27	011010100101011010100101
28	011011100100011011100100
29	011100100011011100100011
30	011101100010011101100010
31	011110100001011110100001
32	011111100000011111100000
33	100000011111100000011111
34	100001011110100001011110
35	100010011101100010011101
36	100011011100100011011100
37	100100011011100100011011
38	100101011010100101011010
39	100110011001100110011001
40	100111011000100111011000
41	101000010111101000010111
42	101001010110101001010110
43	101010010101101010010101
44	101011010100101011010100
45	101100010011101100010011
46	101101010010101101010010
47	101110010001101110010001
48	101111010000101111010000
49	110000001111110000001111
50	110001001110110001001110
51	110010001101110010001101
52	110011001100110011001100
53	110100001011110100001011
54	110101001010110101001010
55	110110001001110110001001
56	110111001000110111001000
57	111000000111111000000111
58	111001000110111001000110
59	111010000101111010000101
60	111011000100111011000100
61	111100000011111100000011
62	111101000010111101000010
63	111110000001111110000001
64	111111000000111111000000

Appendix C

Complete Measured Spur Results

FN	O	100k	200k	300k	400k	500k	600k	700k	800k	900k	1M
1	1	-13.33	-33.66	-45	-52.15	-58.33	-63.33	-66.66	-70.32	-73.5	
1	2	-34.33									
1	3	-38.33									
2	1	-40	-25.34	-62	-45.17	-70	-55.5	-76	-63.67	-81.5	-71.17
2	2		-45.7								
2	3		-50								
3	1	-40	-53	-35	-66.63	-68.83	-51.5	-74.15	-73.5	-60.16	
3	2	-62		-56.3							
3	3			-58							
4	1	-45.15	-63	-68.5	-46	-76	-83	-83.8	-63.3	-84	-89.33
4	2				-56.34						
4	3				-60.66						
5	1					-42.33					-61.16
5	2					-65					
5	3					-64					
6	1	-31.5	-50.67	-60.67	-62.34	-60.67	-45.17	-68.84	-78.17	-79.67	-76.17
6	2						-66.66				
6	3						-70.17				
7	1	-38	-42	-55	-61.5	-58	-71.5	-46.33	-75	-66.5	-76.5
7	2							-69			
7	3							-73			
8	1	-31	-50.5	-59	-63	-65	-68	-68	-49.5	-69	-75
8	2								-72.5		
8	3								-72.5		

Table C.1: Spurs for Different Fractions and Orders
Test Conditions: Fref=6.5MHz, SEED=1, RBW=VBW=3KHz, I_{cp}=0.8 m.A, and PRD=6ns

FN	O	100k	200k	300k	400k	500k	600k	700k	800k	900k	1M
9	1	-37	-39	-53	-58	-61	-66	-61	-73.5	-50.33	-76.5
9	2									-70.3	
9	3									-74.5	
10	1					-53					-55
10	2										-77.3
10	3										-78
11	1	-31.15	-50	-60.67	-63.5	-68.33	-71.8	-76	-75.5	-72.5	-69.33
11	2										
11	3										
12	1	-36	-40.5	-52	-51.8	-51.5	-65.5	-58	-70	-73	-72
12	2										
12	3										
13	1	spur only at 1.3MHz → -53.5									
13	2	spur only at 1.3MHz → -77.5									
13	3										
14	1	-35.5	-51.5	-58.5	-58.5	-55.8	-69	-73.5	-75.3	-64	-75
14	2										
14	3										
15	1					-52.5					-65.33
15	2										
15	3										
16	1	-26.83	-40.33	-50.83	-60.33	-65.33	-67.33	-71.5	-73.7	-78.5	-77.5
16	2										
16	3										
17	1	-41.5	-53.3	-49.5	-66.5	-66.3	-66.3	-76.3	-72.2	-74.5	-82.2
17	2										
17	3										
18	1	-39	-53	-55	-55	-65.6	70.5	-61.5	-71.5	-76.5	-75.5
18	2										
18	3										
19	1	-41.33	-52	-52	-64.5	-65	-67.5	-74.5	-61	-79	-79.5
19	2										
19	3										
20	1					-49					-62.5
20	2										
20	3										
21	1	-40.5	-36	-61	-54.5	-66.5	-63.5	-74	-72	-76.4	-76.5
21	2										
21	3										
22	1	-22	-42.5	-52.5	-57.5	-63.5	-69	-73	-75	-78	-81.5
22	2										
22	3										
23	1	-39	-52	-53	-44.2	-66.5	-70	-67	-65.3	-79	-78.5
23	2										
23	3										

Table C.1 cont.:Spurs for Different Fractions and Orders **Test Conditions:** Fref=6.5MHz, SEED=1, RBW=VBW=3KHz, I_{cp}=0.8 m.A, and PRD=6ns

FN	O	100k	200k	300k	400k	500k	600k	700k	800k	900k	1M
24	1	-37.5	49.5	-48	-59	-64.5	-66	-56	-74	-74.5	-67.5
24	2										
24	3										
25	1					-56					-65
25	2										
25	3										
26	1	spurs: (1.3MHz,-69.5) , (2.6MHz, -75) , (3.9MHz, -80)									
26	2										
26	3										
27	1	-34	-52.33	-58.5	-60	-54	-63.33	-71.7	-74.5	-75.5	-72
27	2										
27	3										
28	1	-31	-48.5	-58	-64.5	-68.5	-70	-70.5	-69	-59	-68
28	2										
28	3										
29	1	-32.8	-50	-58.5	-64.3	-66	-64.5	-53.5	-66	-76	-80
29	2										
29	3										
30	1					-47.5					-65
30	2										
30	3										
31	1	-38	-49.5	-37.5	-60	-65	-55	-69	-74.5	-66.5	-75.3
31	2										
31	3										
32	1	-20.5	-35.5	-46.3	-54	-60	-64.5	-69	-71.5	-75.5	-78
32	2										
32	3										
33	1	-20.5	-35.5	-46.3	-54	-60	-64.5	-69	-71.5	-75.5	-78
33	2										
33	3										
34	1	-38	-49.5	-37.5	-60	-65	-55	-69	-74.5	-66.5	-75.3
34	2										
34	3										
35	1					-48					-64
35	2										
35	3										
36	1	-32.8	-50	-58.5	-64.3	-66	-64.5	-53.5	-66	-76	-80
36	2										
36	3										
37	1	-31	-48.5	-58	-64.5	-68.5	-70	-70.5	-69	-59	-68
37	2										
37	3										
38	1	-34	-52.33	-58.5	-60	-54	-63.33	-71.7	-74.5	-75.5	-72
38	2										
38	3										

Table C.1 cont.:Spurs for Different Fractions and Orders **Test Conditions:** Fref=6.5MHz, SEED=1, RBW=VBW=3KHz, I_{cp}=0.8 m.A, and PRD=6ns

FN	O	100k	200k	300k	400k	500k	600k	700k	800k	900k	1M
39	1	spurs: (1.3MHz → -71) , (2.6MHz → -74) , (3.9MHz → -79)									
39	2										
39	3										
40	1					-56					-65
40	2										
40	3										
41	1	-37.5	49.5	-48	-59	-64.5	-66	-56	-74	-74.5	-67.5
41	2										
41	3										
42	1	-39	-52	-53	-44.2	-66.5	-70	-67	-65.3	-79	-78.5
42	2										
42	3										
43	1	-22	-42.5	-52.5	-57.5	-63.5	-69	-73	-75	-78	-81.5
43	2										
43	3										
44	1	-40.5	-36	-61	-54.5	-66.5	-63.5	-74	-72	-76.4	-76.5
44	2										
44	3										
45	1					-49					-62.5
45	2										
45	3										
46	1	-41.33	-52	-52	-64.5	-65	-67.5	-74.5	-61	-79	-79.5
46	2										
46	3										
47	1	-39	-53	-55	-55	-65.6	70.5	-61.5	-71.5	-76.5	-75.5
47	2										
47	3										
48	1	-41.5	-53.3	-49.5	-66.5	-66.3	-66.3	-76.3	-72.2	-74.5	-82.2
48	2										
48	3										
49	1	-26.83	-40.33	-50.83	-60.33	-65.33	-67.33	-71.5	-73.7	-78.5	-77.5
49	2										
49	3										
50	1					-52.5					-65.33
50	2										
50	3										
51	1	-35.5	-51.5	-58.5	-58.5	-55.8	-69	-73.5	-75.3	-64	-75
51	2										
51	3										
52	1	spur only at 1.3MHz → -59									
52	2	spur only at 1.3MHz → -85.5									
52	3	spur only at 1.3MHz → -76.5									
53	1	-41.5	-46	-54	-61	-55	-71	-60.5	-72.5	-73.3	-73.5
53	2										
53	3										

Table C.1 cont.:Spurs for Different Fractions and Orders **Test Conditions:** Fref=6.5MHz, SEED=1, RBW=VBW=3KHz, I_{cp}=0.8 m.A, and PRD=6ns

FN	O	100k	200k	300k	400k	500k	600k	700k	800k	900k	1M
54	1	-27.5	-47	-57	-61	-68	-73	-70	-71	-70	-65
54	2										
54	3										
55	1					-54.5					-55.5
55	2										-80.5
55	3										-78
56	1	-39.33	-42.5	-59	-61.3	-63	-68.5	-65	-74	-54	-80
56	2									-77	
56	3									-75	
57	1	-33	-52	-63.5	-67.3	-69	-70.5	-68.5	-54.35	-68.33	-77.1
57	2								-71.33		
57	3								-73.5		
58	1	-44.17	-45.5	-58.5	-64	-62	-72.5	-50	-79	-73	-79.33
58	2							-72.67			
58	3							-70			
59	1	-34.67	-51.5	-62.5	-67.67	-63.83	-48.67	-68.5	-76.5	-82.33	-80.33
59	2						-66.17				
59	3						-70.17				
60	1					-41.33					-42.5
60	2					-64					
60	3					-67.5					
61	1	-36.5	-53.5	-54.5	-35.5	-62.5	-71.66	-72.15	-72.2	-53.5	-54
61	2		-65		-59						
61	3				-59.5						
62	1	-40	-51	-34.5	-62.33	-65	-50	-70	-71.33	-59.16	
62	2			-58							
62	3			-59							
63	1	-41	-26.17	-56.67	-42.83	-66	-54.83	-73.83	-62.17	-79	-70
63	2		-46.64								
63	3		-50								
64	1	-14.33	-28.33	-38.33	-46.33	-52.5	-58.5	-63.5	-67	-70.8	-74.5
64	2	-38.15									
64	3	-38.33									

Table C.1 cont.:Spurs for Different Fractions and Orders **Test Conditions:** Fref=6.5MHz, SEED=1, RBW=VBW=3KHz, I_{cp}=0.8 m.A, and PRD=6ns

Bibliography

[1] R. Schneiderman, *Future Talk: The Changing Wireless Game*, IEEE Press, 1997.

[2] S. H. Ardalan and J. J. Paulos, "An Analysis of Nonlinear Behavior in the Delta-Sigma Modulator," *IEEE Transactions on Circuits and Systems*, vol. 34, pp. 593–603, June 1987.

[3] M. Perrott, T. Tewksbury, and C. Sodini, "A 27-mW CMOS Fractional-N Synthesizer Using Digital Compensation for 2.5-Mb/s GFSK Modulation," *IEEE Journal of Solid State Circuits*, vol. 32, pp. 2048–2059, Dec. 1997.

[4] J. C. Candy and G. C. Temes, *Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation*, IEEE Press, 1992.

[5] W. Bax, T. Riley, C. Plett, and M. Copeland, "A Sigma-Delta Frequency Discriminator Based Synthesizer," *International Symposium on Circuits and Systems*, pp. 1–4, 1995.

[6] F. Gourgue, M. Bellanger, S. Azrouf and V. Bruneau, "A Bandpass Subsampled Delta-Sigma Modulator for Narrow-band Cellular Mobile Communications," *International Symposium on Circuits and Systems*, vol. 5, pp. 353–356, 1994.

[7] B. Razavi, "Challenges in Portable RF Transceiver Design," *Optoelectronics Magazine*, vol. 12, no. 5, Sept. 1996.

[8] P. Lin, J. Lou, and J. Kuo, "A CMOS Quadrature Modulator for Wireless Communication IC," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, pp. 559–561, June 1997.

[9] Bar-Giora Goldberg, *Digital Techniques in Frequency Synthesis*, McGraw Hill, 1996.

[10] L. Hernandez, "Frequency Synthesis Based on Bandpass Sigma-Delta Modulation," *IEEE Electonic Letters*, pp. 1642–1643, August 1996.

[11] B. Miller and R. J. Conley, "A Multiple Modulator Fractional Divider," *IEEE Transactions on Instrumentation and Measurment*, June 1991.

[12] T. A. Riley and M. A. Copeland, "A Simplified Continuous Phase Modulator," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, pp. 321–328, May 1994.

[13] T. A. Riley, M. A. Copeland, and T. A. Kwasniewski, "Delta-Sigma Modulation in Fractional-N Frequency Synthesizer," *IEEE Journal of Solid State Circuits*, pp. 553–559, May 1993.

[14] M. H. Perrott, T. L. Tewksbury, and C. G. Sodini, "A 27mW CMOS Fractional-N Synthesizer/Modulator IC," *IEEE International Solid-State Circuits Conference*, pp. 366–367, 1997.

[15] J. Craninckx and M. S. Steyaert, "A 1.75-GHz/3-V Dual-Modulus Divide-by-128/129 Prescaler in 0.7-μm CMOS," *IEEE Journal of Solid State Circuits*, pp. 890–897, July 1996.

[16] N. M. Filiol, T. A. Riley, C. Plett, and M. A. Copeland, "An Agile ISM Band Frequency Synthesizer with Built-In GMSK Data Modulation," *IEEE Journal of Solid State Circuits*, pp. 998–1008, July 1998.

[17] Y. Matsuya, K. Uchimura, A. Iwata and T. Yoshitome, "A 16-bit Oversampling A-to-D Conversion Technology Using Triple-Integration Noise Shaping," *IEEE Journal of Solid State Circuits*, pp. 921–929, Dec. 1987.

[18] W. Bax and M. Copeland, "A GSM Modulator using a Delta-Sigma Frequency Discriminator Based Synthesizer," *International Symposium on Circuits and Systems*, pp. 498–501, 1998.

[19] Industry implementation of international standard ISO/IEC, *Recommendation H.262*, IEEE Standards, 1993.

[20] J. Zhanh et. al, "MPEG-2 Video Services for Wireless ATM Networks," *IEEE Journal on Selected Areas in Communications*, vol. 15, pp. 119–128, January 1997.

[21] T. Ojanpera and R. Prasad, *Wideband CDMA for Third Generation Mobile Communications*, Artech House, 1998.

[22] K. Park, *Personal and Wireless Communications: Digital Technology and Standards*, Kluwer Acadmic, 1996.

[23] M. Catedra and J. Perez-Arriage, *Cell Planning for Wireless Communications*, Artech House, 1999.

[24] C. Wuensch, "Fractional-N Synthesizers meet HSCSD and GPRS demands," *Microwave & RF*, pp. 105–121, August 1999.

[25] A. V. Oppenheim, *Discrete-time signal processing*, Prentice Hall, 1989.

[26] S. R. Northworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Converter: Theory, Design, and Simulation*, IEEE Press, 1996.

[27] J. Sophocles Orfanidis, *Introduction to Signal Processing*, Prentice Hall, 1996.

[28] P. Steiner and W. Yang, "Stability Analysis of the Second-Order Σ-Δ Modulator," *International Symposium on Circuits and Systems*, vol. 5, pp. 365–368, May 1994.

[29] S. C. Pinault and P. Lopresti, "On the Behaviour of the Double-Loop Sigma-Delta Modulator," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 40, pp. 467–479, August 1993.

[30] S. Hein and A. Zakhor, "Stability and Scaling of Double-Loop $\Sigma\Delta$ Modulators," *International Symposium on Circuits and Systems*, vol. 3, pp. 1312–1315, 1992.

[31] S. Hein and A. Zakhor, "On the Stability of the Sigma-Delta Modulators," *IEEE Transactions on Signal Processing*, vol. 41, pp. 2322–2348, July 1993.

[32] Roland E. Best, *Phase-Locked-Loop: Design, Simulation, and Applications*, McGraw Hill, 1997.

[33] F. M. Gardner, "Charge-pump phase lock loops," *IEEE Transactions on Communications*, pp. 1849–1858, November 1980.

[34] A. Hajimiri and T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," *IEEE Journal of Solid State Circuits*, pp. 179–194, Feb. 1998.

[35] Bar-Giora Goldberg, "Analog and Digital Fractional-n PLL Frequency Synthesis: A Survey and Update," *Applied Microwave and Wireless*, pp. 32–42, June 1999.

[36] V. F. Kroupa, "Noise Properties of PLL Systems," *IEEE Transactions on Communications*, pp. 2244–2252, October 1982.

[37] B. Razavi, F. L. Kwing, and H. Ran, "Design of High-Speed, Low-Power Frequency Dividers and Phase-Locked Loops in Deep Submicron CMOS," *IEEE Journal of Solid State Circuits*, pp. 101–109, Feb. 1995.

[38] P. V. Brennan, *Phase-Locked Loops: Principles and Practice*, MacMillan, 1996.

[39] Bar-Giora Goldberg, "The Evolution and Maturity of Fractional-N PLL Synthesis," *Applied Microwave and Wireless*, pp. 124–134, September 1996.

[40] H. Sorensen P. Aziz and J. V. del Spiegel, "An Overview of Sigma-Delta Converter. How a 1-bit ADC Achieves More Than 16-bit Resolution," *IEEE Signal Processing Magazine*, pp. 61–84, Jan. 1996.

[41] Ping Wu and Kai He, "A CMOS Triple-band Fractional-N Frequency Synthesizer for GSM/GPRS/EDGE Applications," *International Symposium on Circuits and Systems*, vol. 4, pp. 706–709, 2001.

[42] H. Sato, K. Kato, and T. Sase, "A Fast Pull-In PLL IC Using Two-Mode Pull-In Technique ," *Electronics and Communications in Japan, Part 2*, vol. 75, pp. 41–50, 1992.

[43] P. Larsson, "High-Speed Architecture for a Programmable Frequency Divider and a Dual-Modulus Prescaler," *IEEE Journal of Solid State Circuits*, pp. 744–748, May 1996.

[44] Motorola Inc., "The Technique of Direct Programming by Using a Two-Modulus Prescaler," *Application Note AN827*, 1995.

[45] W. Rhee, "Design of High-Performance CMOS Charge-Pumps in Phase-Locked Loops," *International Symposium on Circuits and Systems*, pp. 545–548, 1999.

[46] A. Hill and J. Surber, "The PLL Dead Zone and How to Avoid It," *RF Design*, pp. 131–134, March 1992.

[47] W. Lindsey and C. Chie, "A Survey of Digital Phase-Locked Loops," *Proceedings of the IEEE*, vol. 69, April 1981.

[48] A. Bellaouar and M. I. Elmasry, *Low-Power Digital VLSI Design: Circuits and Systems*, Kluwer Academic Publishers, 1995.

[49] J. F. Wakerly, *Digital Design: Principles and Practices*, Prentice-Hall, 1994.

[50] John N. Wells, "US Patent No. US4609881," *Marconi Instruments Limited*, Sept. 1986.

[51] J. Crawford, *Frequency Synthesizer Design Handbook*, Artech House, 1994.

[52] Ching-Rong Chang and Jinn-Shyan Wang, "A New High-Speed/Low-Power Dynamic CMOS Logic And Its Application to the Design of an AOI-Type ROM," *International Symposium on Circuits and Systems*, vol. 1, pp. 254–257, 1999.

[53] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-Power CMOS Digital Design," *IEEE Journal of Solid State Circuits*, pp. 473–484, April 1992.

[54] K. Shu, E. Sanchez-Sinencio, F. Maloberti, and U. Eduri, "A Comparative Study of Digital Sigma-Delta Modulators for Fractional-N Synthesis," *ICECS'01*, pp. 1391–1394, September 2001.

[55] L. Sun, T. Lepley, F. Nozahic, A. Bellissant, T. Kwasniewski, and B. Heim, "Reduced Complexity, High Performance Digital Delta-Sigma Modulator for Fractional-N frequency synthesis," *International Symposium on Circuits and Systems*, vol. 2, pp. 152–155, May 1999.

[56] T. Cho and P. Gray, "A 10-bit, 20MS/s, 35mW Pipelined A/D Converter," *IEEE Journal of Solid State Circuits*, vol. 30, no. 3, March 1995.

[57] T. Cho, "Low-Power Low-Voltage ADC Techniques Using Pipelined Architectures," *Ph.D. Thesis, University of California, Berkeley*, 1995.

[58] Kevin M. Daugherty, *Analog-To-Digital Conversion, A Practical Approach*, McGraw-Hill, 1995.

[59] P. Gray, "High speed CMOS A/D converters," *Presentation Slides, University of California, Berkeley*, 1995.

[60] Texas Instruments, "Industry's First Programmable Resolution Communications ADC," *Integration*, p. 8, Dec. 1998.

[61] A. Matsuzawa et al., "A 6b 1GHz Dual-Parallel A/D Converter," *IEEE ISSCC Digest of Technology*, pp. 174–175, 1991.

[62] B. Peetz et al., "An 8-bit 250 Msamples/s Analog-to-Digital Converter: Operation without a Sample and Hold," *IEEE Journal of Solid State Circuits*, vol. 21, pp. 997–1002, December 1986.

[63] R. Hui et al., "A CMOS Current-Mode Pipeline ADC Using Zero-Voltage Sampling Technique," *International Symposium on Circuits and Systems*, May 1998.

[64] T. Shu et al., "A 10bit 40MS/s BiCMOS A/D Converter," *IEEE Journal of Solid State Circuits*, vol. 31, no. 10, pp. 1507–1510, Oct. 1996.

[65] K. Kim et al., "A 10-b, 100-MS/s CMOS A/D Converter," *IEEE Journal of Solid State Circuits*, vol. 32, pp. 302–311, March 1997.

[66] D. Mercer, "A 14-b 2.5 MSPS Pipelined ADC with On-Chip EPROM," *IEEE Journal of Solid State Circuits*, vol. 31, pp. 70–76, January 1996.

[67] D. Cline et al., "A Power Optimized 13-b 5 Msamples/s Pipelined Analog-to-Digital Converter in 1.2 μm CMOS," *IEEE Journal of Solid State Circuits*, vol. 31, pp. 294–303, March 1996.

[68] W. Song et al., "A 10-b 20-Msamples/s Low-Power CMOS ADC," *IEEE Journal of Solid State Circuits*, vol. 30, pp. 514–521, May 1995.

[69] P. Vorenkamp et al., "A 10b 50MS/s Pipelined ADC," *IEEE ISSCC Digest of Technology*, pp. 32–33, 1992.

[70] L. Singer and T. Brooks, "A 14bit 10MHz Calibration-Free CMOS Pipelined A/D Converter," *Symp. of VLSI Circuits Dig. of Tech. Papers*, pp. 94–95, 1996.

[71] J. Yang et al., "A CMOS 12-bit 4MHz Pipelined ADC with Commutative Feedback Capacitor," *IEEE Custom Integrated Circuits Conference*, pp. 427–430, 1996.

[72] K. Nagaraj et al., "An 8-bit 50MS/s Pipelined A/D Converter with an Area and Power Efficient Architecture," *Custom IC Conf.*, pp. 423–26, 1996.

[73] L. Zhang et al., "A 12-bit 2V Current-Mode Pipelined ADC Using Digital CMOS Process," *International Symposium on Circuits and Systems*, pp. 369–372, 1996.

[74] H. Lewis et al., "10b 20Msample/s Analog-to-Digital Converter," *IEEE Journal of Solid State Circuits*, vol. 27, pp. 351–358, March 1992.

[75] W. Colleran et al., "A 10b 100MS/s Pipelined A/D Converter," *IEEE ISSCC Digest of Technology*, pp. 68–69, Feb. 1993.

[76] K. Kusumoto et al., "A 10b 20MHz 30mW Pipelined Interpolating CMOS ADC," *IEEE ISSCC Digest of Technology*, pp. 62–63, Feb. 1993.

[77] S. Tsukamoto et al., "A CMOS 6-b, 200 MSamples/s, 3 V-supply A/D Converter for a PRML Read Channel LSI," *IEEE Journal of Solid State Circuits*, vol. 31, pp. 1831–1836, November 1996.

[78] T. Wakimoto et al., "Si Bipolar 2GS/s 6b Flash A/D Conversion LSI," *IEEE ISSCC Digest of Technology*, pp. 232–233, 1988.

[79] Y. Akazawa et al., "A 400 MSPS 8b Flash AD Conversion LSI," *IEEE ISSCC Digest of Technology*, pp. 98–99, 1987.

[80] P. Vorenkamp et al., "A 12-b, 60-MSamples/s Cascaded Folding and Interpolating ADC," *IEEE Journal of Solid State Circuits*, vol. 32, pp. 1876–1886, December 1997.

[81] M. Flynn et al., "CMOS Folding A/D Converters with Current-Mode Interpolation," *IEEE Journal of Solid State Circuits*, vol. 31, pp. 1248–1257, September 1996.

[82] B. Nauta et al., "A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter," *IEEE Journal of Solid State Circuits*, vol. 30, pp. 1302–1308, December 1995.

[83] R. Van de Plassche et al., "An 8b 100MHz Folding ADC," *IEEE ISSCC Digest of Technology*, pp. 222–223, 1988.

[84] R. Baird et al., "A Low Oversampling Ratio 14-b 500-kHz $\Delta\Sigma$ ADC with a Self-Calibrated Multibit DAC," *IEEE Journal of Solid State Circuits*, vol. 31, pp. 312–320, March 1996.

[85] I. Dedic, "A 6th-Order Triple-Loop Sigma-Delta CMOS ADC with 90dB SNR and 100kHz Bandwidth," *IEEE ISSCC Digest of Technology*, pp. 188–189, Feb. 1994.

[86] Y. Matsuya and J. Yamada, "1V Power Supply 384kS/s 10b ADC and DAC with Swing-Suppression Noise Shaping," *IEEE ISSCC Digest of Technology*, pp. 192–193, Feb. 1994.

[87] C. Thanh et al., "A 2nd-Order Double Sampled Sigma-Delta Modulator with Individual-Level Averaging," *Symposium on VLSI Circuits Digest of Technology*, pp. 100–101, 1996.

[88] S. Au and B. Leung, "A 1.95V 0.34mW 12bit Sigma-Delta Modulator Stabilized with Local Feedback Loops," *IEEE Custom Integrated Circuits Conference*, pp. 411–414, 1996.

[89] T. P. Kenny, T. A. Riley, N. M. Filiol, and M. A. Copeland, "Design and Realization of a Digital Sigma Modulator for Fractional-N Frequency Synthesis," *IEEE Transactions on Vehicular Technology*, pp. 510–521, March 1999.

List of Publications

1. A. E. Hussein and M. I. Elmasry, "A ROM Based Fractional-N Frequency Synthesizer for Wireless Communication," *in Proc. of Midwest Symposium on VLSI*, to be published, August 2002.

2. A. E. Hussein and M. I. Elmasry,"A Fractional-N Frequency Synthesizer for Wireless Communications," *in Proc. of IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 513-516, May 2002.

3. A. E. Hussein and M. I. Elmasry, "Low Power Analog-to-Digital Converter for Wireless Communication," *in Proc. of 10th ACM Great Lakes Symposium on VLSI*, pp. 113-116, March 2000.

4. A. E. Hussein, M. A. Hasan, and M. I. Elmasry, "A New Algorithm for the Division in the Residue Number System (RNS) For Low Power Applications," *in Proc. of CCECE98*, vol. 1, pp. 205-208, May 1998.

5. A. E. Hussein and M. I. Elmasry,"A Novel Fractional-N Frequency Synthesizers for Wireless Communications," *IEEE Journal of Solid-State Circuits* (in preparation).

6. A. E. Hussein and M. I. Elmasry, A Low Power Analog-to-Digital Converter for Wireless Communication," *IEEE Transactions on Circuits and Systems II* (in preparation).