King Fahd University of Petroleum and Minerals

Electrical Engineering Department

EE200: Digital Logic Circuit Design
Fall Semester 2014 (141)

A. Course Information

Text Book:	**Digital Design (5th Edition) by M. M. Mano**				
Educators	**Details**		**Office**	**Phone**	
Instructor	Name: Dr. Saad Al-Abeedi Email: alabeedi@kfupm.edu.sa Office Hours: Sun & Tue: 10:00-10:50AM and 12:20-1:00PM		59-0075	7833	
Course Coordinator	Name: Dr. Hassan Ragheb Email: hragheb@kfupm.edu.sa		59-2084	2792	
Lab Coordinator:	Name: Mr.Ali Al-Beladi Email: albleladi@kfupm.edu.sa		59-0016	--	
Grading:	Assignments, attendance, Quizzes	Laboratory	Major 1	Major 2	Final
	20%	20%	15%	15%	30%
Exams	**1st Major**	**2nd Major**	**Final**		
Exams Dates:	**First Major** **Tue. October 21, 2014**	**Second Major** **Tue. Nov. 25, 2014**	Per the schedule from the registrar's office		
Exams Times:	7 – 9 PM	7 – 9 PM			
Exams Places:	To be announced	To be announced			
Important Dates:	Last day to drop the course without a permanent record	Last day to drop the course with "W" grade	Last day to drop all courses with "WP/WF" Thru Registrar's office.		
	Thu. Sept. 11, 2014	Thu. October 23, 2014	Thu. Dec. 18, 2014		

Note #1: All exams (**1st Major**, **2nd Major** and **Final Exam**) are **coordinated** (i.e. it is common for all sections). The Final Exam is **comprehensive** (covers chapters 1-7 as described in the syllabus and class notes). Lab Final will be given by the Lab instructor in the Lab during a normal Lab session.

Note #2: According to the rules and regulations of KFUPM, attendance is **MANDATORY**. More than **8** unexcused absences will be reported to the registrar office and result in a **GRADE of DN** regardless of the student's performance.

Note #3: It is your responsibility to solve the ***practice problems*** as soon as the material is covered in the class. Solution will be posted on **Blackboard (**https://blackboard.kfupm.edu.sa**)**. The ***practice problems*** set will not be collected.

Note #4: Your instructor will give you other home work assignments which will be collected and graded. Quizzes will be given regularly based on the homework and the ***practice problems***...

Note #5: Class notes, announcements and HW solutions will be posted on the class webpage on Blackboard (or WebCT)
It is your responsibility to check announcements regularly.

B. Course Details.

1. **Course (Catalog) Description**

   Number systems & codes. Logic gates. Boolean Algebra. Karnaugh maps. Analysis and synthesis of combinational systems, decoders, multiplexers, adders and subtractors, PLA's. Types of flip-flops. Memory concept. Registers. Introduction to sequential circuit design.

2. **Prerequisites(s)**

   Calculus I (MATH 101)
   General Physics I (PHYS 101)

3. **Course objectives** are to

   - Introduce the students to the digital principles with emphasis on logic design.
   - Familiarize the students with the necessary mathematical tools such as number systems, codes, and Boolean algebra.
   - Learn the principles of analysis and design of combinational logic circuits
   - Learn the principles of analysis and design of sequential logic circuits.

4. **Learning Outcomes**

   After successfully completing the course, the students will be able to

   Outcome1: apply knowledge of number systems, codes and Boolean algebra to the analysis and design of digital logic circuits.

   Outcome 2: identify, formulate, and solve engineering problems in the area of digital logic circuit design.

   Outcome 3: use the techniques, skills, and modern engineering tools such as logic works, necessary for engineering practice.

   Outcome 4: to function on multi-disciplinary teams through digital circuit experiments and projects.

   Outcome 5: to design a digital system, components or process to meet desired needs within realistic constraints.

5. **Topics Covered**

   - Binary Numbers, Number Base Conversions,
   - Complements, Signed Binary Numbers, Binary Codes,
   - Binary Logic, Boolean Algebra and digital logic gates,
   - Forms of logic functions and K-map simplification,
   - Analysis and design of combinational logic circuits,
   - Adders, Multipliers, Magnitude Comparator, Decoders, Multiplexers,
   - Programmable logic devices,
   - Flip-flops and sequential circuits,
   - Registers and counters.

6. **References.**
   - *Logic and Computer Design Fundamentals*, M. Morris Mano and C. R. Kime, 5th Edition, Prentice Hall, 2008.
   - *Fundamentals of Digital Logic with Verilog Design*, S. Brown and Z. Vranesic, 2nd Edition, McGraw Hill, 2008.

C. Tentative Course Outline and Schedule

Week	Date	Topics	Sections	Labs/Prob. Sessions
1	Aug. 31-Sept. 4	Digital Systems, Binary Numbers, Number Base Conversions, Octal & Hexadecimal Numbers	1.1-1.4	No Lab
2	Sept. 7-11	Complements, Signed Binary Numbers, Binary Codes, Binary Logic	1.5-1.7 1.9	No Lab
3	Sept. 14-18	Boolean Algebra: Axioms, Theorems & Properties. Boolean functions, Digital Logic Gates	2.1-2.4 2.7-2.8	Exp#1: Getting Started with the Laboratory Equipment
4	Sept. 21-25	Canonical & Standard Forms Simplification of Boolean functions Using K-Maps, Product of Sums Simplification.	2.5-2.6 3.1-3.5	No Lab.
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5	Oct. 12-16	Don't-care Conditions, NAND, NOR, and Other Two Level Implementations, Exclusive-OR Function. Introduction to HDL	3.6-3.9	Exp#2: Building logic functions using traditional ICs
6	Oct. 19-23	Combinational Logic: Analysis and Design Procedures, Code Conversion, Adder circuits.	4.1-4.4	Exp#3: Introduction to Verilog HDL
7	Oct. 26-30	Subtractors, Decimal Adder, binary multiplier, Magnitude Comparator, Decoders.	4.5-4.8	Exp#3a: programming with Verilog HDL (part I)
8	Nov. 2-6	Encoders and Multiplexers Sequential Circuits, Latches,	4.9-4.11 5.1-5.3	Exp#3b: programming with Verilog HDL (part I)
9	Nov. 9-13	Flip-flops, Analysis of Clocked Sequential Circuits.	5.4-5.5,	Exp#4: Combinational Logic Circuits (Part I)
10	Nov. 16-20	State Reduction and Assignment, Flip-flop Excitation Tables, Design Procedure, Synthesis using different flip flops	5.7-5.8	Exp#5: Combinational Logic Circuits (Part II)
11	Nov. 23-27	Registers and Shift Registers	6.1, 6.2	Exp#6: Combinational Logic Circuits (Part III)
12	Nov. 30-Dec. 4	Ripple Counters, Synchronous Counters and other counters.	6.3-6.5	Exp#7: Sequential Logic Circuits (Part I)
13	Dec. 7-11	Random Access Memory	7.2-7.3	Exp#8: Sequential Logic Circuits (Part II)
14	Dec. 14-18	Programmable Logic, PLD'S, ROM, Programmable Logic Array, Programmable Array Logic.	7.5-7.7	Exp#9: Final Lab Project
15	Dec. 21-25	Revision		Lab Final
	Dec. 28	Revision		

D. Practice Problems

Chapter 1: 5, 7, 9, 18, 20, 29, 35
Chapter 2: 2, 8, 12, 15, 18, 20
Chapter 3: 2, 7, 12, 15, 19, 24
Chapter 4: 5, 11, 13, 20, 25, 29, 31, 35
Chapter 7: 15, 18, 19, 21, 25
Chapter 5: 2, 6, 9, 12, 19
Chapter 6: 5, 7, 8, 12, 21