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STATE MACHINE SYNTHESIS WITH WEINBERGER ARRAYS
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Abstract

The development of a digital circuit synthesis program is described. The program accepts the transition table of a state machine and returns equations for an implementation that assumes a sum-of-product next-state and output functions. From the equations for the next-state and output functions, nMOS VLSI layout for a Weinberger array is generated. D flip-flops are assumed for memory elements. Using this tool, tedious manual calculations can be avoided and layouts can be generated automatically from state table descriptions.

Keywords: design