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AUTOMATIC WEINBERGER ARRAY SYNTHESIS FROM UAHPL DESCRIPTION
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Abstract

A Weinberger array (WA) (Weinberger 1967) synthesis system is described that automatically generates WAs for combinational logic circuits modelled in Universal Hardware Programming Language (UAHPL) (Masud and Sait 1986). The system also minimizes the area required by the WA by performing row compaction. An algorithm similar to that used for channel routing is employed for compaction (Hashimoto and Stevens 1971). This convenient tool for designing combinational logic circuits models at a high level of abstraction and much of the procedure is automated.

Descriptors: logic circuits