A High Compliance Input and Output Regulated Body-Driven Current Mirror for Deep-Submicron CMOS

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Abstract—A current mirror circuit that uses body-driven MOSFETs to achieve an ultra-low input and output voltage is presented. High-gain amplifiers, suitable for a deep submicron process, are used to provide matching as well as input and output regulation. Simulation results were verified with measurements performed on a fabricated chip using the 90-nm CMOS process from ST-Microelectronics.

Index Terms—Analog integrated circuits, CMOS, mirrors.

I. INTRODUCTION

The current mirror (CM) remains a critical building block of analog VLSI circuits. In accordance with Moore’s Law, MOSFET feature sizes continue to be reduced, which in turn increase the difficulties in designing high-performance analog circuits in deep-submicron technologies [1]. Supply voltage scaling reduces the amount of signal swing, with a lower limit being imposed by the threshold voltage, $V_{TH}$ (which does not scale down at the same rate), further decreasing signal swing. In addition, channel-length modulation is increased as channel-length is reduced, leading to a low output resistance, $r_{o}$, and a low open-circuit gain [2]. Traditional cascode CM structures may improve $r_{o}$, but at the expense of signal swing, with $V_{out,min} = 2V_{DS,SAT}$. Low voltage (LV) operation is critically important, for example, when the CM is used as a built-in current sensor, e.g. IDDQ testing [3].

The use of body-driven (BD) techniques allows the minimum signal voltage imposed by $V_{TH}$ to be circumvented [4]. In this paper, the BD technique is exploited to produce a high-compliance body-driven CM (BDCM) that employs input and output regulation for low and high output impedances, respectively. The BDCM architecture presented is suitable for use with deep-submicron (DSM) CMOS processes. A test chip was fabricated using the 90-nm process from ST-Microelectronics. The theoretical analysis, simulation results, and measured results are presented.

II. BODY-DRIVEN CURRENT MIRROR

A. Operating Principles

An ideal current mirror is characterized by low input impedance ($R_{in}$), high output impedance ($R_{out}$), and low voltage requirements on the input and output, i.e. high-compliance. Voltage regulation has been used to improve CM input [5] and output [6] impedances. High output-compliance regulated CMs can be achieved with various architectures [7].

A regulated BDCM topology removes the input voltage $V_{TH}$ limitation while providing high output impedance [8]. However, input regulation can be used to further approach the ideal CM characteristics. The authors in [8] reduced the $V_{DS}$ mismatch between a pair of triode-transistors, but the amplifier suggested did not provide a suitably high gain for a DSM process; this is addressed in the design described herein.

The proposed BDCM topology shown in fig. 1, uses BD MOSFETs $M_1$ and $M_2$ to provide the current mirroring. The typical gate-drain connected MOSFET seen in a CM is replaced by the body-drain connected one seen with $M_1$. For a given input current, $I_{IN}$, $V_{GS}$ of $M_{1,2}$ can be set high enough for triode operation. The required $V_{DS,1,2}$ is thus low. The body terminal is slightly forward-biased and is only required to be at the low $V_{DS}$ value to bias the CM. The $V_{GS}$ of the BDMOSFETs is higher than $V_{TH}$ yet is removed from the input path, whereas $V_{DS}$ and $V_{BS}$ remain in the input path but do not have any $V_{TH}$ constraint. This is the key to the low input and output voltage capability.

For BD designs, the substrate typically has a forward-bias on the order of a few to tens of millivolts; conduction is in the PA range. $M_{1,2}$ were implemented in their own p-wells, via a deep n-well.

![Fig. 1. A body-driven current mirror (BDCM) schematic.](image)

The required $V_{BS}$, given by (4) for $M_{1,2}$ can be solved for using the triode-region $I_{DS}$ equation and well-known body-effect equations, which are (1), (2), and (3) respectively. That is:

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Amplifier A1 regulates the gate of M4 to equalize $V_{DS1.2}$. This provides voltage matching, and thus better current mirroring. In addition, output impedance is increased, since $V_{DS2}$ is held constant as $V_{out}$ varies. Amplifier A2 regulates the gate of M3 in order to set $V_{in}$ equal to $V_{in,ref}$, keeping $V_{in}$ constant as $I_{in}$ changes equates to a lowered input resistance.

For a given $I_{DS}$ as $V_{DS4,4}$ decreases, the required $V_{GS4,4}$ increases as given by (6), eventually causing the amplifiers to reach their saturation output voltage, $V_{sat}$ regulation is lost.

$$V_{sat} > V_{DS} = \frac{I_{DS}}{\mu C_{ox} W / L \cdot V_{th}} + V_{th}$$

The minimum output voltage is given as:

$$V_{out,min} = V_{DS} + V_{DS,4}$$

However, the output voltage can be decreased until A1 saturates. Referring to (6), if $M4$ is sized such that $V_{GS4}$ remains less than $V_{sat}$ as $V_{out}$ decreases, the amplifier doesn’t saturate and a high $R_{out}$ is maintained. In (12), a large $A$ can compensate for a lower $r_{in}$.

The minimum input voltage, $V_{in, min}$, is given by:

$$V_{in, min} = V_{GS4} + V_{DS,4,2sat}$$

where $V_{DS4,2sat}$ is the $V_{DS}$ that causes A2 to saturate. $V_{in, ref}$ is chosen such that $V_{DS3} < V_{DS4,2sat}$. Note that in (8) a $V_{DS4, sat}$ is not required since a lower $V_{th4}$ actually decreases $R_{out}$.

Using (1), the DC current transfer error, $\varepsilon = I_{sat} - I_{in}$, is:

$$\varepsilon = \beta (V_{GS1} - V_{th1}) V_{DS1} + (V_{DS1} - V_{th1}) / 2$$

where $\beta = \mu C_{ox} W / L$ and $C_{ox}$ is the capacitance of the oxide. It is assumed that $V_{GS1} = V_{GS2}$ and $V_{TH1} = V_{TH2} = V_{TH4}$. Any difference in $V_{DS}$ increases mismatch, and a reduction in $V_{GS}$ reduces mismatch.

### B. Small-signal Analysis

The small-signal analysis of the BDCM is straightforward. Without regulation, the input current delivered by a PMOS current source the small-signal current transfer ratio is:

$$\frac{i_{o}}{i_{in}} = \frac{r_{in}}{r_{in} + (1/g_{m}) \cdot r_{on}}$$

where $i_{o}$ is the current source current and $i_{in}$ is the current delivered to the mirror. Using realistic DC parameters for our process ($r_{on} = 100 k\Omega$ and $1/g_{m} = 30 k\Omega$) the current transfer ratio is 0.81, but ideally it would be 1 if $r_{on} = 0$.

The output resistance, $R_{out}$, is given by:

$$R_{out} = g_{sat} r_{on} r_{ox} (A + 1) + g_{sat} r_{ox} + r_{ox}$$

which improves the input resistance by a factor of $A$. Revisiting (10) and assuming $A=100$, the new $R_{out} = 0.3 \Omega$ which gives $I_{out}/I_{source} \approx 1$. Compared to [8], $R_{in}$ is reduced by a factor of $A$. This is a vast reduction in the loading effect of the BDCM on previous stages.

### C. Amplifier Design Criteria

M1,2 are in triode, and have a low $r_{in}$ therefore any difference in $V_{DS,2}$ will cause a large and linear current mismatch. Therefore, a high-gain amplifier with minimal offset is critical for good mirroring. For DSM devices, this is a problem because they have a low open-circuit gain, $g_{sat}/r_{in}$, around 10 for the 90-nm devices used.

$V_{DS,2}$ also operate near ground and so the input common-mode range (ICMR) must satisfy this requirement.

Lastly, the compliance can be maximized if the amplifiers have a maximized output voltage, $V_{DD}$.

The criteria above lead to the use of a gain-enhanced (GE), folded-cascade differential amplifier with a PMOS input stage and rail-to-rail output buffer. The GE amplifiers use a cascode structure to further improve the gain. However, due to their limited gain, a systematic offset is introduced. The amplifiers designed had a gain of 110 dB, phase margin of 108 degrees, $f_{max}$ of 86 MHz, and a systematic offset of 127 $\mu$V.

### III. SIMULATION RESULTS

Simulation was performed using Spectre and the 90-nm device models provided in the MOSIS-90 design-kit. To further decrease the required input and output voltages for a given $I_{DS}$, the MOSFET sizes were made relatively large. There is a trade-off between area and compliance. For PMOS, the ratio, in microns, was 26.88:0.2, and for NMOS, 11.52:0.2. The minimum $W$ and $L$ are 0.12 and 0.1 $\mu$m, respectively. The supply voltage, $V_{dd}$, is 1 V. A p-well/n-well diode representing the BDMOSFET well junction capacitance was included.

The plot of $I_{out}$ vs. $V_{out}$ is shown in Fig. 2. Current source behavior begins at an ultra-low voltage of 1.4 mV. The output resistance, $R_{out}$, rapidly enters the $\Omega$ range and reaches 360 $\Omega$, as shown in fig. 3.

Fig. 2 shows also a comparison between the proposed BDCM, a prior regulated output BDCM [8], and a simple CM all designed with 90-nm devices. The performance of [8] in a 90-nm process is severely degraded due to the very low-gain amplifier used, with an approximate gain of $A = g_{sat} r_{in}/2$. $R_{out}$ is improved by over 3 orders of magnitude.
The DC current transfer curve, shown in fig. 4, indicates that there is an 8.8 µA offset in current. There is a high degree of linearity (i.e. a variation in $I_{in}$ causes an equal change in $I_{out}$); the average slope of fig. 4 is 1.0012. The drain voltages of the BDMOSFETs, $M_1$ and $M_2$ are 1.16 mV and 660.5 µV, respectively. For $M_{1,2}$, the sensitivity to $V_{GSU,2}$ is 17 µA/mV.

Fig. 5 shows $R_{in}$ vs. $I_{in}$. An ultra-low $R_{in}$ of approximately 20 mΩ is maintained until the amplifier saturates, at which point, $R_{in}$ approaches 120 Ω. The saturation point can be increased by increasing $V_{in,ref}$. For simulations purposes $V_{in,ref}$ is set to 20 mV.

The frequency response, shown in fig. 6, indicates that the 3dB roll-off is 83 kHz. The AC reference current has a value of 1, which sets the input branch current, which is then mirrored by the output branch. There is a small current gain due to the channel-length modulation between the bias reference and input branch currents; the current is not applied directly.

IV. FABRICATION RESULTS

The BDCM was fabricated with the ST-Microelectronics CMOS090 platform. This is a 7-metal, single-poly process. The area of the die is 0.7151 X 0.7266 mm². Testing was carried out on the packaged (24-pin DIP) parts. A 24 kΩ external resistor is used to set all internal bias voltages and currents. The total power consumption is 2.3 mW. Core and I/O circuitry have separate supplies. Current mirror and differential-amplifier transistor pairs were split and laid out in a common centroid configuration to reduce mismatch due to doping and thermal gradients. For multi-fingered devices, dummy poly strips are used.

The input and output current is shown in Fig. 7. The compliance is 40 mV and a reverse current of 4.3 µA occurs at $V_{in} = 0$ V. With a non-zero ground voltage for $M_3$, a reverse current flows. The non-zero voltage is caused by $IR$ drop on the ground line.

Current mismatch was mitigated by using $V_{GSU,2} = 0.32$ V. There is a trade-off between compliance and the mirroring offset. The reduced $V_{GSU,2}$ increases $R_{out}$, since the devices are not as heavily in the triode region. The average $R_{out}$ is 10 GΩ.

The peak-to-peak current fluctuation is 1.4 uA and the RMS value is 0.23 uA. This is a deviation from the mean value (22.7 uA) of 1.01%.
Fig. 7. \( I_{\text{out}} \) vs. \( V_{\text{in}} \) – Output current characteristic.

Fig. 8. \( I_{\text{out}} \) vs. \( I_{\text{in}} \) – DC current transfer characteristic.

Fig. 9. \( V_{\text{in}} \), \( I_{\text{in}} \) vs. \( I_{\text{off}} \) – Input voltage regulation.

The current transfer curve is shown in Fig. 5. The slope of curve is 1.02. The average value of \( I_{\text{out}} \) - \( I_{\text{in}} \) is 0.7 \( \mu \text{A} \). The bias current \( I_{\text{off}} \) is used to modulate \( I_{\text{in}} \) as shown in Fig. 6, and the resulting average input resistance is 0.5 m\( \Omega \).

Fig. 10. Large-signal stability test.

Large-signal stability is tested by applying a 110 kHz, 1 V square wave, as shown in Fig. 10. The output load is 17 k\( \Omega \). The same load was used to yield a frequency response with a 3dB rolloff of 300 kHz. Finally, a photograph of the fabricated packaged chip is shown in Fig. 11 along with the bonding wires.

Fig.11. Photo of 90-nm CMOS BDCM test chip.

V. CONCLUSION

The regulated input, regulated output CM topology implemented with high-gain amplifiers offers low input and high output impedance. Also, the input and output voltage requirements are lowered via body-driven MOSFETs.

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