# Introduction to Computer Architecture

COE 308 – Computer Architecture

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## Welcome to COE 308

- Instructor: Dr. Muhamed F. Mudawar
- Office: Building 22, Room 328
- Office Phone: 4642
- Schedule and Office Hours:
  - http://faculty.kfupm.edu.sa/coe/mudawar/schedule/
- Course Web Page:
  - http://faculty.kfupm.edu.sa/coe/mudawar/coe308/
- Email:
  - mudawar@kfupm.edu.sa

## Grading Policy

- Quizzes 10%
- MIPS Programming 15%
- CPU Design Project 20%
- Midterm Exam I 15%
- Midterm Exam II 20%
- Final Exam 20%



## Late Policy, Attendance, & Makeup

- Late project is accepted up to 3 days late
  - But will be penalized 5% for each late day
- Attendance will be taken at the beginning of each lecture
  - Official / medical excuses must be presented within one week
- Late attendance is counted as half presence
  - Two late attendances are counted as one absence
- No makeup exam will be given for missing exam or quiz

# Software Tools

- MIPS Simulators
  - MARS: MIPS Assembly and Runtime Simulator
    - Runs MIPS-32 assembly language programs
    - Website: http://courses.missouristate.edu/KenVollmar/MARS/
- CPU Design and Simulation Tool
  - Logisim
    - Educational tool for designing and simulating CPUs
    - Website: http://ozark.hendrix.edu/~burch/logisim/



# Why Study Computer Architecture?

- You want to be called "Computer Engineer or Scientist"
- You want to become an "expert" on computer hardware
- You want to become a "computer system designer"
- You want to become a "software designer" and need to understand how to improve code performance
- Technology is improving rapidly ⇒ new opportunities
- Has never been more exciting!
- Impacts Electrical Engineering and Computer Science

# Which Books will be Used?

- Computer Organization & Design
  The Hardware/Software Interface
  - David Patterson and John Hennessy
  - Morgan Kaufmann Publishers
  - Third Edition (2005)
  - Read the textbook in addition to the course slides


- References: MIPS32 Architecture
  - Volumes I, II, and III are available online


- Course webpage
  - http://faculty.kfupm.edu.sa/coe/mudawar/coe308/



# Course Objectives

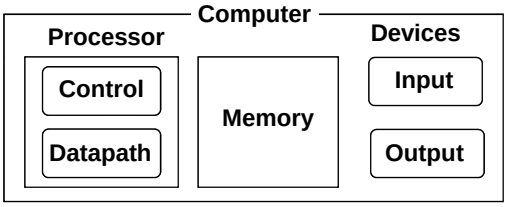
- Understand modern computers, their evolution, and trade-offs at the HW/SW interface
  - Instruction Set Architecture
  - Computer Arithmetic
  - Performance and Metrics
  - Pipelining
- Understand the design of a modern computer system
  - Datapath design
  - Control design
  - Memory System Design
  - I/O System Design

# Five Classic Components

- Since the 1940's, computers have 5 classic components
- Input devices
  - Keyboard, mouse, …
- Output devices
  - Display, printer, …
- Storage devices
  - Volatile memory devices: DRAM, SRAM, …
  - Permanent storage devices: Magnetic, Optical, and Flash disks, …
- Datapath
- Control

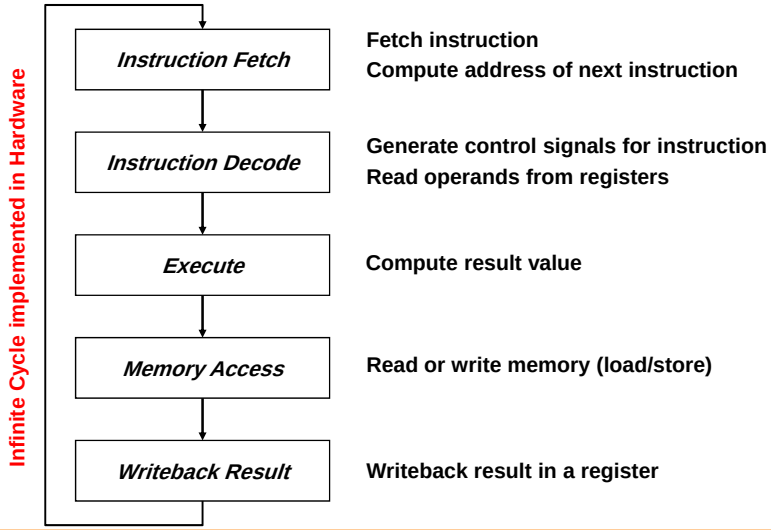
  } **Together, they are called the Processor**

- Newly added 6th component: Network
  - Essential component for communication in any computer system



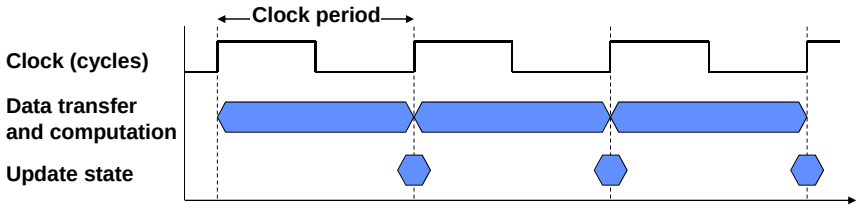



# Fetch - Execute Cycle



# CPU Clocking

Operation of digital hardware is governed by a clock




- **Clock period: duration of a clock cycle**
  - **e.g., 250 ps = 0.25 ns = 0.25 ×$10^{-9}$ sec**
- **Clock frequency (rate) = 1 / clock period**
  - **e.g., 1/ 0.25 ×$10^{-9}$ sec = 4.0×$10^{9}$ Hz = 4.0 GHz**



# What is "Computer Architecture" ?

- Computer Architecture =

  Instruction Set Architecture +
  Computer Organization

- Instruction Set Architecture (ISA)
  - WHAT the computer does (logical view)
- Computer Organization
  - HOW the ISA is implemented (physical view)
- We will study both in this course

# Instruction Set Architecture (ISA)

- Is a subset of Computer Architecture
- Definition by Amdahl, Blaaw, and Brooks – 1964

  *"… the attributes of a [computing] system as seen by the programmer, i.e. the conceptual structure and functional behavior, as distinct from the organization of the data flows and controls the logic design, and the physical implementation."*

- An ISA encompasses …
  - Instructions and Instruction Formats
  - Data Types, Encodings, and Representations
  - Programmable Storage: Registers and Memory
  - Addressing Modes: Accessing Instructions and Data
  - Handling Exceptional Conditions



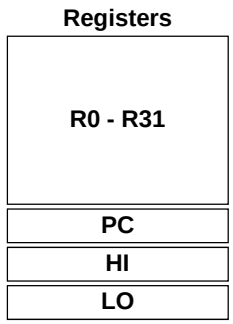
# Instruction Set Architecture – cont'd

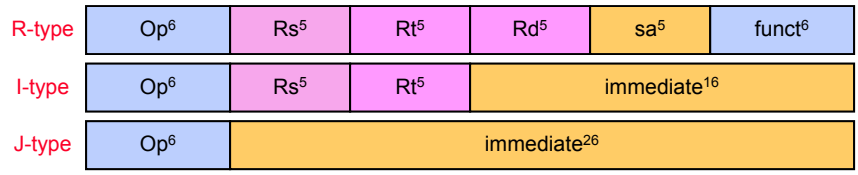
- Critical interface between hardware and software
  - Standardizes instructions, machine language bit patterns, etc.
  - Advantage: different implementations of the same architecture
  - Disadvantage: sometimes prevents using new innovations

| Examples | (versions) | Introduced in |
|---|---|---|
| Intel | (8086, 80386, Pentium, ...) | 1978 |
| IBM Power | (Power 2, 3, 4, 5) | 1985 |
| HP PA-RISC | (v1.1, v2.0) | 1986 |
| MIPS | (MIPS I, II, III, IV, V) | 1986 |
| Sun Sparc | (v8, v9) | 1987 |
| Digital Alpha | (v1, v3) | 1992 |
| PowerPC | (601, 604, …) | 1993 |

# Overview of the MIPS ISA

- All instructions are 32-bit wide
- Instruction Categories
  - Load/Store
  - Integer Arithmetic
  - Jump and Branch
  - Floating Point
  - Memory Management
- Three Instruction Formats



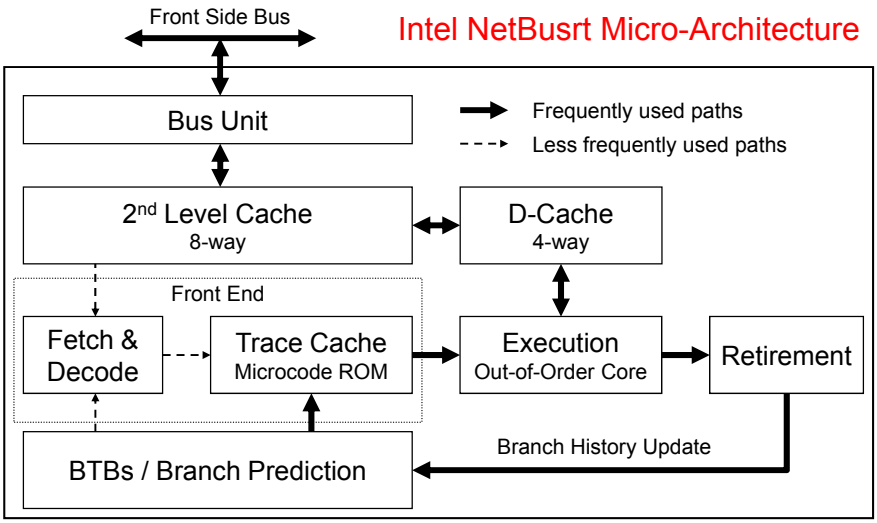






# Computer Organization

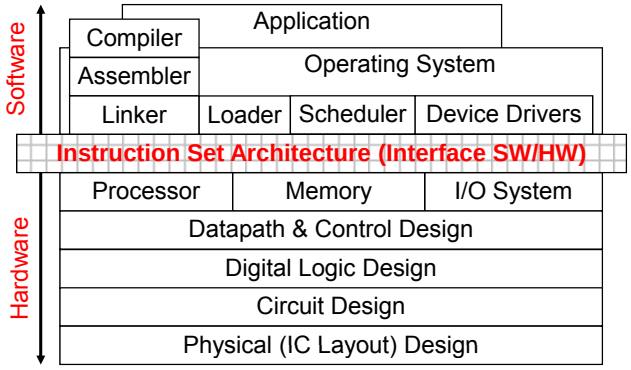
- Realization of the Instruction Set Architecture
- Characteristics of principal components
  - Registers, ALUs, FPUs, Caches, ...
- Ways in which these components are interconnected
- Information flow between components
- Means by which such information flow is controlled
- Register Transfer Level (RTL) description

# Microprocessor Organization






# Abstraction Layers




- Abstraction hides implementation details between levels
- Helps us cope with enormous complexity
- ISA is at the interface between software and hardware

# Technology Improvements

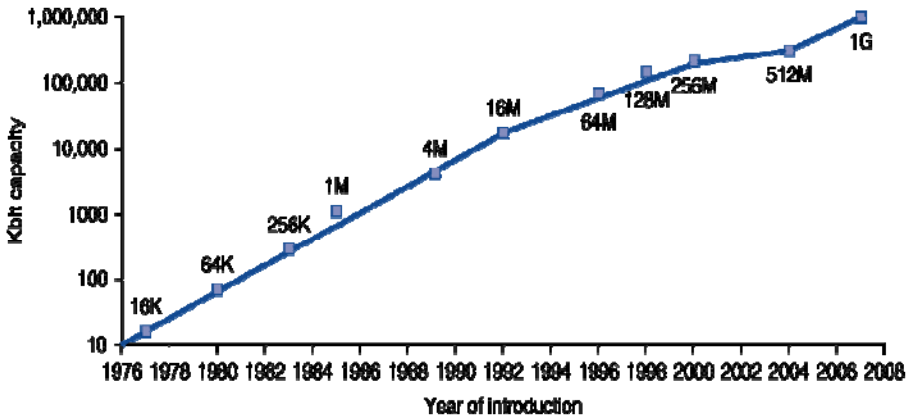
| Year | Technology | Relative performance/cost |
|---|---|---|
| 1951 | Vacuum tube | 1 |
| 1965 | Transistor | 35 |
| 1975 | Integrated circuit (IC) | 900 |
| 1995 | Very large scale IC (VLSI) | 2,400,000 |
| 2005 | Ultra large scale IC | 6,200,000,000 |

- Processor transistor count: about 30% to 40% per year
- Memory capacity: about 60% per year (4x every 3 years)
- Disk capacity: about 60% per year
- Opportunities for new applications
- Better organizations and designs

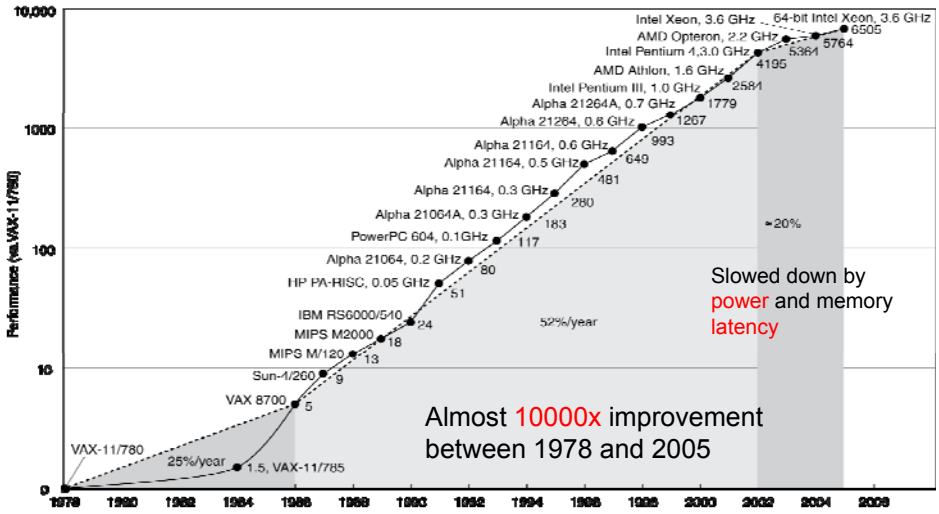


# Growth of Capacity per DRAM Chip

- DRAM capacity quadrupled almost every 3 years
  - 60% increase per year, for 20 years



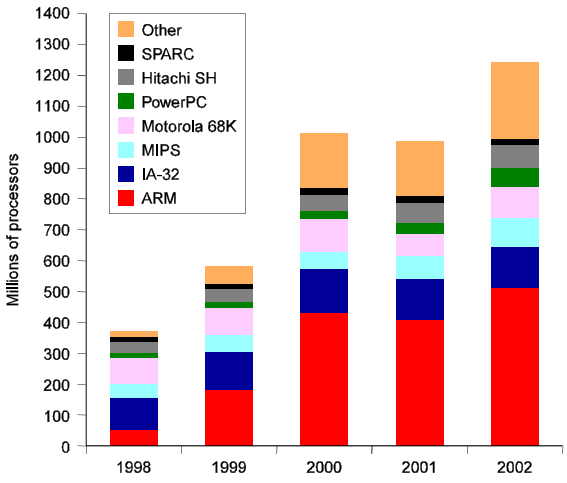
# Processor Performance (1978-2005)






# Microprocessor Sales (1998 - 2002)

- ARM processor sales exceeded Intel IA-32 processors, which came second
- ARM processors are used mostly in cellular phones
- Most processors today are embedded in cell phones, digital TVs, video games, and a variety of consumer devices

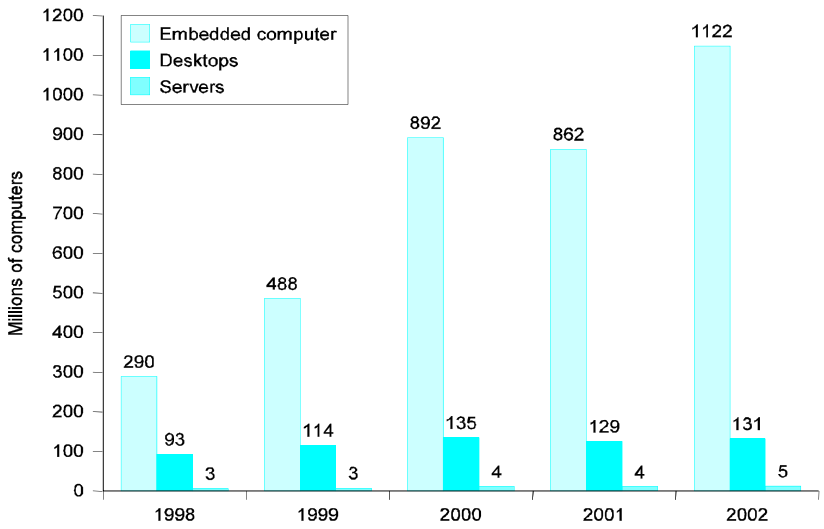


# Classes of Computers

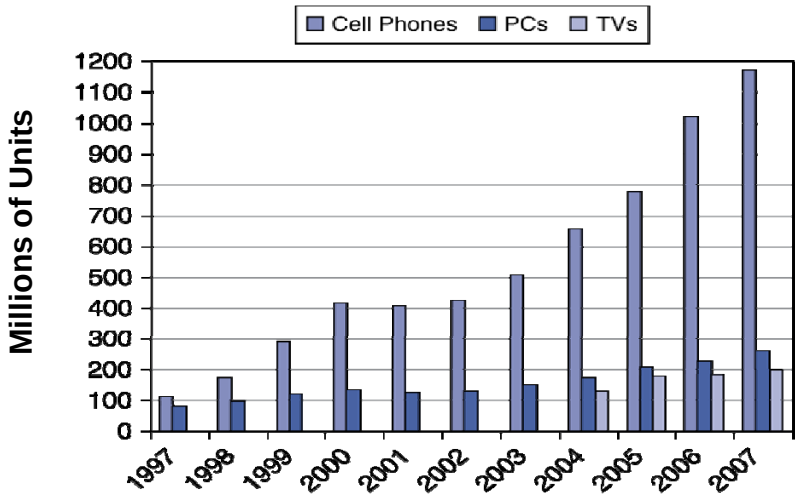
- Desktop / Notebook Computers
  - General purpose, variety of software
  - Subject to cost/performance tradeoff
- Server Computers
  - Network based
  - High capacity, performance, reliability
  - Range from small servers to building sized
- Embedded Computers
  - Hidden as components of systems
  - Stringent power/performance/cost constraints



# Computer Sales (1998 - 2002)

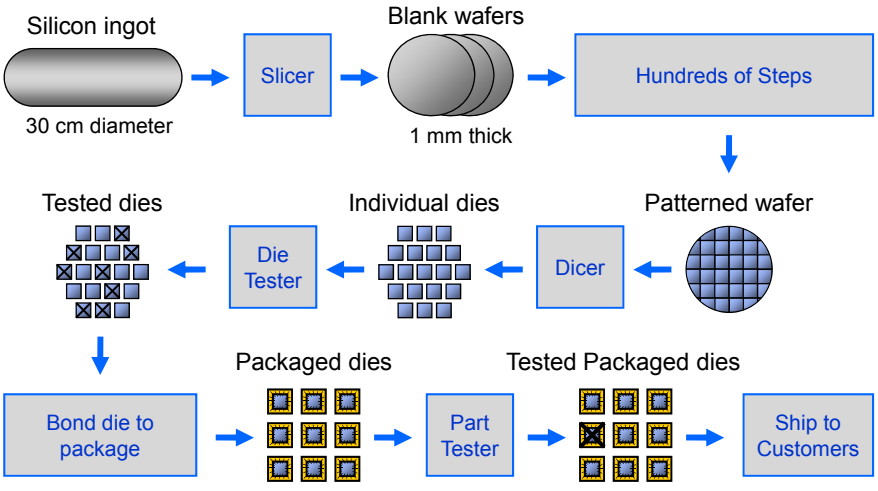


# The Processor Market (1997-2007)



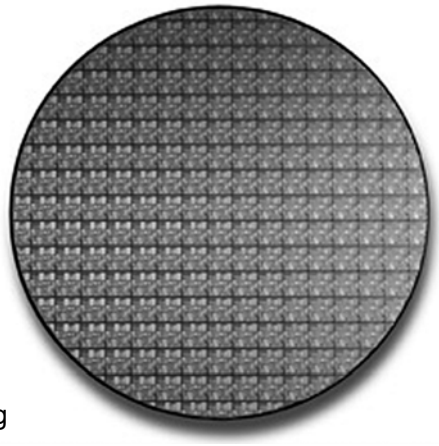



# Chip Manufacturing Process



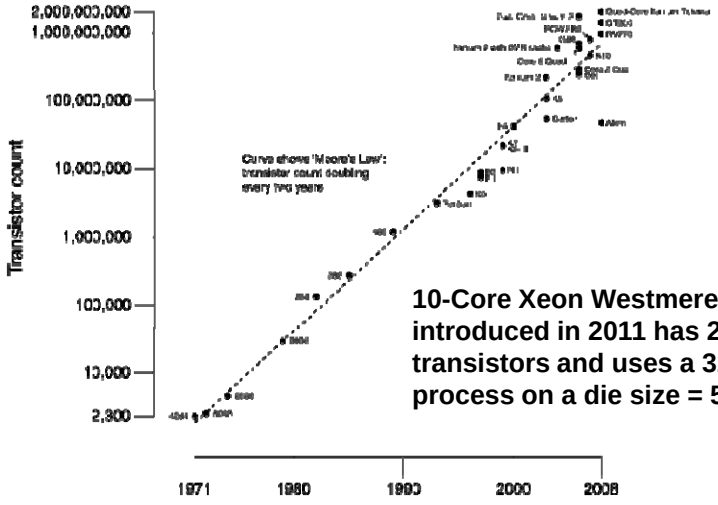
# Wafer of Pentium 4 Processors

- 8 inches (20 cm) in diameter
- Die area is 250 $mm^2$
  - About 16 mm per side
- 55 million transistors per die
  - 0.18 µm technology
  - Size of smallest transistor
  - Improved technology uses
    - 0.13 µm and 0.09 µm
- Dies per wafer = 169
  - When yield = 100%
  - Number is reduced after testing
  - Rounded dies at boundary are useless



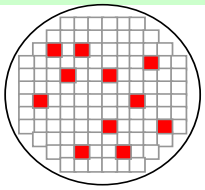


# CPU Transistor Count (1971 – 2008)

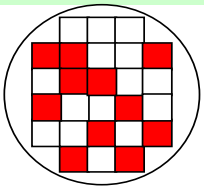



**10-Core Xeon Westmere-EX introduced in 2011 has 2.6 billion transistors and uses a 32 nm process on a die size = 512 $mm^2$**

# Effect of Die Size on Yield



120 dies, 109 good



26 dies, 15 good

Good Die

Defective Die

Dramatic decrease in yield with larger dies

Yield = (Number of Good Dies) / (Total Number of Dies)

$$\text{Yield} = \frac{1}{(1 + (\text{Defect per area} \times \text{Die area} / 2))^2}$$

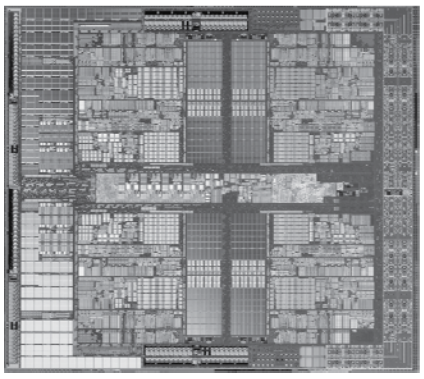
Die Cost = (Wafer Cost) / (Dies per Wafer × Yield)

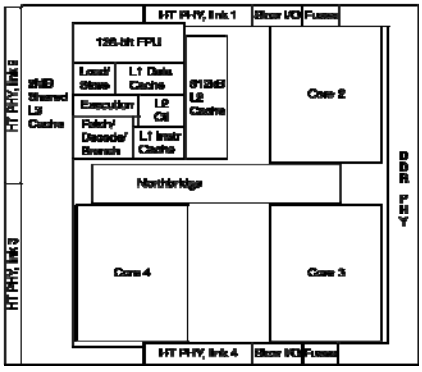


# Inside a Multicore Processor Chip

AMD Barcelona: 4 Processor **C**ores

**3 Levels of Caches**





# Course Roadmap

- Instruction set architecture (Chapter 2)
- Computer arithmetic (Chapter 3)
- Performance issues (Chapter 4)
- Constructing a processor (Chapter 5)
- Pipelining to improve performance (Chapter 6)
- Memory: caches and virtual memory (Chapter 7)
- Introduction to Parallel Architectures

Key to obtain a good grade: read the textbook!