COE 205 Computer Organization & Assembly Language – Spring 2008

Assignment 1: IA-32 Processor Architecture

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Due Date: Wednesday, March 12, 2008

Q1. (1 pt) What is the duration of a single clock cycle (in nanoseconds) in a 3.4 GHz processor?

Q2. (1 pt) In an 8-stage non-pipelined processor, how many clock cycles would it take to execute 10 instructions?

Q3. (1 pt) In an 8-stage pipelined processor, how many clock cycles would it take to execute 5 instructions?

Q4. (1 pt) Suppose an 8-stage pipelined processor has one stage that requires two cycles to execute, how many clock cycles would it take to execute 4 instructions?

Q5. (1 pt) A hard disk rotates at 4200 RPM (rotations per minute). What is the time of one rotation in milliseconds?

Q6. (0.5 pt) Which Intel processor was the first member of the IA-32 family?

Q7. (0.5 pt) Which Intel processor first introduced superscalar execution?

Q8. (1 pt) Name all 32-bit general-purpose registers

Q9. (1 pt) Name all six CPU status flags in the Intel processor

Q10. (0.5 pt) Which flag is set when an arithmetic or logical instruction produces a negative result?

Q11. (1 pt) In real-address mode, convert the following hexadecimal segment-offset address to a 20-bit physical address: 8AF3:C91D.

Q12. (0.5 pt) What is the range of addressable memory in protected mode?