King Fahd University of Petroleum and Minerals
Department of Computer Engineering

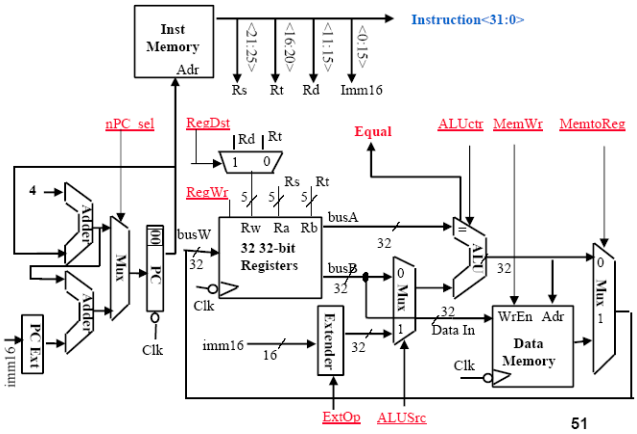
COMPUTER ARCHITECTURE COE 308

Homework 3

Problems	Grading
1	
2	
3	
4	
TOTAL	

QUESTION 1: ANALYSIS OF SINGLE CYCLE DATAPATH

Consider the MIPS single-cycle data path (MIPS-SCDP).



Answer each of the following questions:

1. Is the instruction memory used in MIPS-SCDP is combinational or sequential logic circuit! Why!
   The memory is a combinational circuit (asynchronous). We have no clock for intermediate states during the single cycle.

2. For what reason the Registers of MIPS-SCDP must have two reads ports and one write port. What control is needed for Registers

   The instruction groups R, I-Lw, and I-Sw require fetching two source registers. Reading in not-destructive as opposed to write, thus, the registers need only to control the Register write.

3. A MUX is used in MIPS-SCDP to select between two options: (1) PC + 4, or (2) PC + 4 + Ext(Imm16).
   Specify all instruction types that require each of the following options:

   (PC + 4) is selected for instructions: R type like Add r1,r2,r3, I-Lw, I-Sw, and I-Beq when NT
   (PC + 4 Ext(Imm16)) is selected for instructions: Type B and I-Beq when T

4. A MUX is used in MIPS-SCDP to select the register address for reading the Registers as shown in the diagram. Specify all instruction types that require each of the following options:

   Rd is selected for instructions: R type like Add r1,r2,r3
   Rt is selected for instructions: I-Lw and I-Sw

5. A MUX is used in MIPS-SCDP to select either of: (1) ALUout, or (2) MEMout to be written back in the Registers. Specify all instruction types that require each of the following options:

   ALUout is selected for instructions: R type like Sub r1,r2,r3
   MEMout is selected for instructions: I-Lw

QUESTION 2: DESIGN OF SINGLE CYCLE DATAPATH

A RISC processor has the following instruction set:

1. R-type or register type defined as: **register-d = register-t op register-s**, where register-x denotes one of 32 user registers, and op is an operation that is supported by following two datapath components: (1) an Arithmetic and Logic Module (ALU), or (2) a Floating-Point Module (FPM).

2. L/S-type or load and store defined as: **register-t = DM(register-s)** and **DM(register-s) = register-t**, where DM is the data memory.

3. I-type or integer type defined as: **register-t = register-s op imm**, where register-x denotes one of 32 user registers, op denotes an integer arithmetic or logic operation, and imm denotes a signed 16-bit immediate data or address.

4. B-type or branch type: **PC = (PC + Ext(imm-16) + 4) if condition is True, or (PC + 4) else,** where condition denotes the result of a comparison of two registers in the ALU such as Beq r1, r2, offset, where Beq is branch-on-equal and offset is a 16-bit signed immediate offset.

Note that we have three main modules which are the ALU, FPM, and DM. To design a single-cycle data path we use a read-only combinational memory as Instruction Memory (IM), where each word (instruction) is 32-bit.

Answer each of the following questions by carefully addressing each step (a, b, c, etc.):

1. Design the Fetch Unit (FU) by using one ALU for incrementing the PC by 4 and another for adding a branch offset to meet the requirement of above Branch type:
    a. How the single-cycle clock is used to update PC!
    b. What is the use of the updated PC value!
    c. Design the path for updating the PC and the interface from PC-out to IM-in. Show the IM-out instruction fields. Indicate all needed control and interface to IM.
    d. Explain why a multiplexer is needed
    e. Do you need to buffer IM-out for single-cycle datapath! Justify your answer.

2. The register File (RF) consists of 32 registers each can hold a 32-bit data operand. Given the above instruction set, answer the following:
    a. Identify the address of source and destination registers and determine the multiplexer (s) needed to satisfy the requirement of a given instruction type (above R, I, L/S, and B types) for both source registers and destination registers.
    b. How many data write-back operand RF must have! How to select the address of a destination register for RF!
    c. What control is needed to write back RF.
    d. Design the RF module with it source and destination registers and indicate the corresponding data buses and includes all the multiplexers and their control (read and write) needed for the RF to satisfy the requirements of the above instruction set.

3. Assume the instruction is fetched from IM and data fields Rs, Rt, Rd, and imm-16 are already available at the output of IM. For this address the following questions:

    a. Indicate the modules to which the fetched register data is to be forwarded for each of R-type, L/S-type, I-type, and B-type. Denote by A and B the RF data buses.

b. Determine the logic, multiplexers, and their control needed at the input of ALU, FPM, and DM to satisfy the requirements of each of R-type, L/S-type, I-type, and B-type. For this indicate all MUXes to be used and link the value of their control to specific instruction types.

c. Determine the multiplexers and their control needed at the output (write-back) of ALU, FPM, and DM to satisfy the requirements of each of R-type, L/S-type, I-type, and B-type.

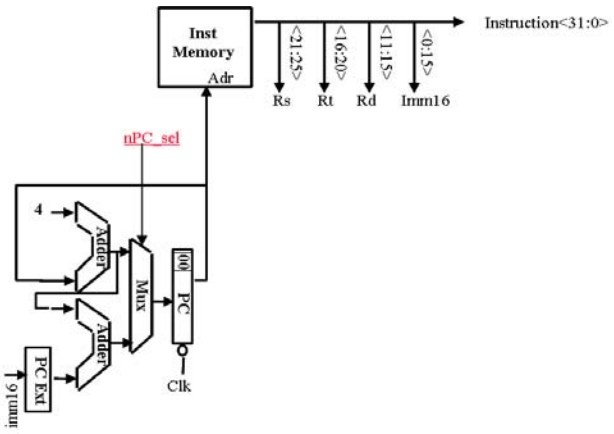
d. Determine the control needed for ALU, FPM, and DM and indicate based on which information control must be generated for each type.
e. Assemble the single-cycle datapath that meets the requirements of above instruction set and draw the datapath with its multiplexers and control.
f. Based on the diagram of your datapath, provide the following tables:
    - Build table where the columns are the used multiplexer controls and the rows represents the instruction types as R-type, L/S-type, I-type, and B-type. Fill-in the table.
    - Build table where the columns are the control of ALU, FPM, and DM and the rows represents the instruction types as R-type, L/S-type, I-type, and B-type. Fill-in the table.

4. Suppose the above data path is to be redesigned as a multi-cycle datapath. Answer each of the following questions:

    a. Describe each of the IF, OF, EX, and WB stages by referring to components of the single-cycle datapath. Identify the location and function of the inter-stage buffers for the multi-cycle datapath.
    b. In which stage decoding and control are to be generated for the above multi-cycle processor.

Answer-1:

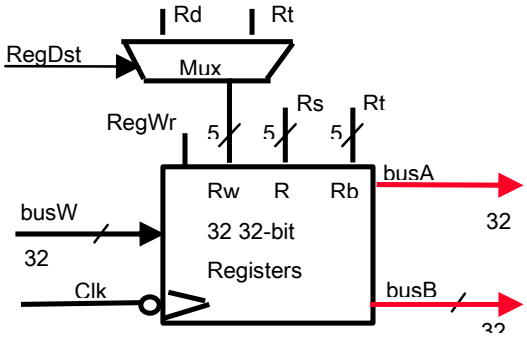
a. The falling edge of the single-cycle clock is used to update PC at the beginning of each cycle.
b. The updated value of PC is used as address input to IM.
c. The updated value of PC is either PC +4 or PC+4+Ext(imm). For this two ALUs are used: (1) special ALU to increment PC by 4, and (2) another ALU to add to PC the sign-extended branch offset. We need NPC_sel to control a MUX for selecting either PC + Sign_Extended(imm)+ 4 if IU condition is ON, or PC + 4 if IU condition is False.



d. To select either PC +4 for all instructions except for an unconditional branching or a taken conditional branching, or PC+4+Ext-32(imm-16) else.
e. We do not need to buffer IM_out (the instruction) for proper operation of the single-cycle datapath because PC is already buffered and IM is a purely combinational logic circuit.

Answer-2:

a. The instruction source registers are Rs and Rt (A and B as data buses) and destination register is Rd (busW as the bus). We need a MUX for selecting the destination address as being Rd (R type) or Rt (Load or I types) with control RegDst = (0 for Rt (I or L types), or 1 for Rd (R type)).
b. We need one register write back as one destination register (R, I, or load types) that is Rd (R-type) or Rt (I or load).
c. A write bus (busW) is needed for RF to Write-Back the outcome of R and L types. We also need one control (Clk: last operation of single cycle) and RegWr to control the write to RF.
d. The RF unit:



Answer-3:

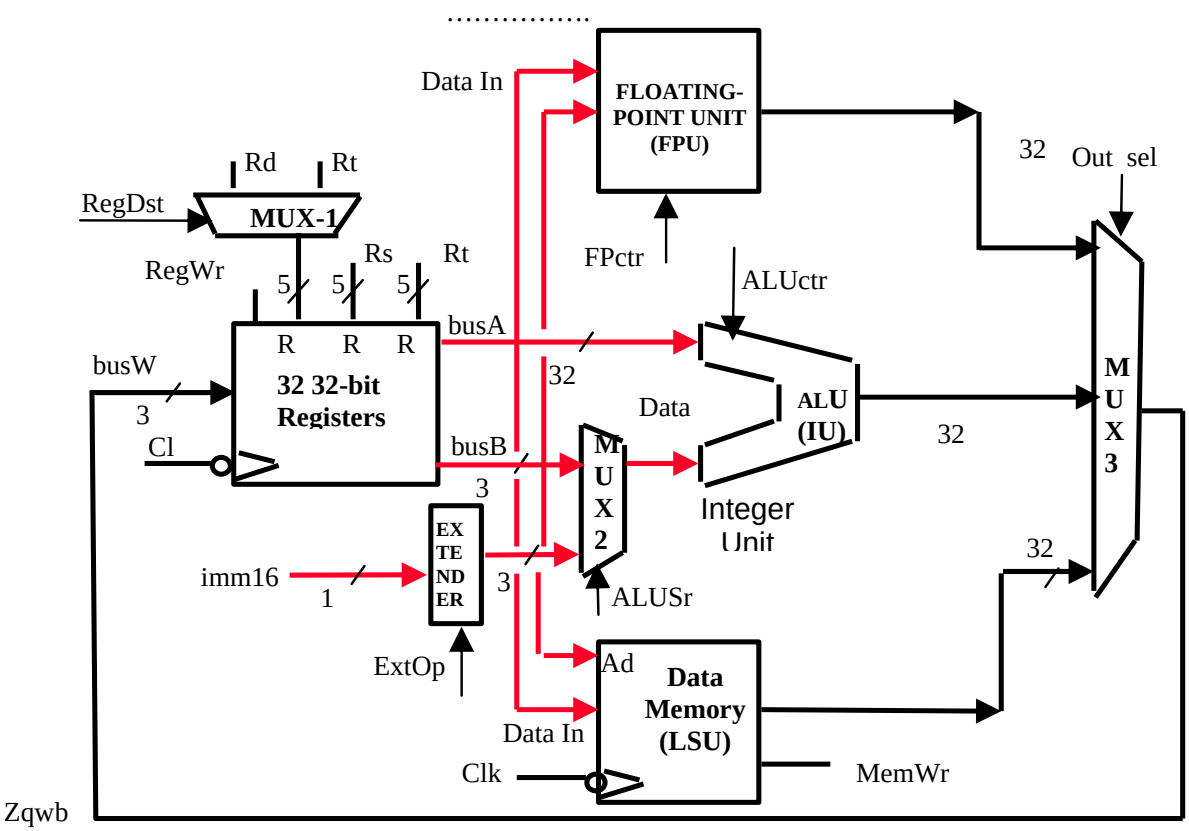
a) The fetched register data feeds (1) the ALU or the FPM for R-type, (2) the DM for L/S type, (3) ALU for I-type, and (4) NA for B-type. The register output buses A and B must both be connected to ALU, FPM, and DM (address and data).

b) The MUXes are as follows. An extender is used to extend the immediate data (I type) and the offset (B type) from 16 bit to 32 bit with sign extension. It is controlled using ExtOp (0 for idle, 1 to carry out extension). Also, a MUX is needed to select the data operand from bus B or the extender output which is controlled by ALUSrc (0 for bus b and 1 for extender).

c) Finally we need one MUX for write back the result of either ALU, FPM, or DM back to the register file. Its control is 2-bit Out_sel. See control below.

d) The ALU, FPM, and DM use the controls ALUctr, FPctr, and MemWr and Clk, respectively. A control unit must generate these controls upon examination of OPCODE. LSU needs MemWr and Clk to specify store operation and its time, respectively. The IU has a Boolean nPC_sel that states the outcome of comparing two operands to support branch-on-zero comparison. nPC_sel takes (1 if compared operands are equal, and 0 else).

e) The datapath is as follows:



	MUX-1	MUX-3	MUX-2	MUX-0 (PC)
R	1	00(ALU) or 01(FPU)	0 (B)	0 (PC+4)
L/S	0 (L)	10 (MEM)	x (L or S)	0(PC+4)
I	0	00 (ALU)	1 (Ext)	0(PC+4)
BR	x	xx	x	1 (B and T)

	ALU	MEM	FPU
R-ALU	1	x	x
R-FPU	x	x	1
L/S	x	1	x

I	1	X	x
BR	x	x	x

Answer 4:

a) We need to use four inter-stage buffers:
   a. The IF stage is for updating the PC (+4 or +4+ext(imm)) where PC represents the first clocked buffer.
   b. The second stage is (1) the decode logic and (2) operand fetch in which the data register buses are buffered (clocked) as well as the extended immediate register.
   c. The third stage represent the execute for which each of the output of ALU, FPM, and DM are clocked and buffered.
   d. The write back stage consists of updating the RF based on data accessed during execute. The buffer is being the clocked register file write control.

b) Instruction decoding is done in the second stage. One approach to implement control is to determine all needed controls as this is done in the single cycle datapath. Controls (Clk, NPC_sel, RegDst, Reg_W, Ext-Op, ALUsrc, FPctr, Mem_wr, Out_sel) and forwardeding to subsequent stages. This requires buffering of the controls for each of MUXs, ALU, FPM, DM, and RF in a similar way to the instruction data buffering described above.