King Fahd University of Petroleum and Minerals
Department of Computer Engineering

COMPUTER ARCHITECTURE COE 308

Homework 1

Problems	Grading
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TOTAL	

QUESTION 1: Trends in Computer Technology

Shortly summarize the growth rate in computer performance every year and provide justification. Refer to annual: (1) microprocessor clock rate, (2) chip density (transistor), (3) DRAM and Disk access times, (4) DRAM and Disk memory capacity, and (5) usage of address bits. Determine the new trends in computer architecture with respect to Internet, networking and multimedia requirements.

Solution:
The rate of growth is: (1) 50% for the peak MIPS speed, (2) 66% for the number of transistors (chip density), (3) 5 times a year for the memory and disk capacity, and (4) 7% for the memory access time, (5) usage of address bits is increased by 20% per year. The CPU architecture is shifting from the traditional computing computer to the multimedia and internet computers. This has deep consequences on the architecture. The unpredictable hierarchical memory is not likely to be very useful because of the need for predictable real-time processing for multimedia. I/O streaming between memory and the display is another important aspect for future computers. The new trends in computer architecture are due to the Internet, networking, and multimedia requirements involving extensive use of computer graphics, SIMD CPU extension with the use of narrow data (bytes), I/O streaming to shorten the path to display, real-time aspects and worst-case guaranteed performance to support QoS, support to fine-grain and coarse-grain parallelism for advanced multimedia algorithms, high code locality, very high network bandwidth, etc.

QUESTION 2: Processor-Memory Performance Gap

1. Since year 2000 the clock frequency of Intel IA32 processors is growing at a rate of approximately 1.54 per year. In 2005, the reference clock rate is 3 GHz. What is the expected clock frequency CF of IA32 processor in year 2010.
2. The access time of some DRAM memory is shrinking by a factor of 6% per year. It is estimated to be 27 ns in year 2005. What is the expected access time AT of the same DRAM in year 2010.
3. Denote by N(k) the ratio of the DRAM access time over the processor clock time, where k is the year. Evaluate N for k=2005 and k=2010 and comment on growth rate of N.

Solution:
1. The expected processor clock frequency in year 2010 is CF = 3 * (1.54)^5 = 25.986 GHz
2. The expected access time of DRAM in year 2010 is AT = 27 * (0.94)^5 = 19.82 ns
3. The expected value of N in year 2005 is N= AT / (1/CF) = AT * CF = 27 * 3 = 81. Therefore, in year 2010 we have N = 27 * (0.94)^5 * 3 * (1.54)^5 = 27 * 3* (0.94*1.54)^5 = 514.92. The gap between processor speed and DRAM access time is growing which is an indicator of the need of new techniques to improve performance of cache memory.

QUESTION 3: MIPS Assembly Language Programming

Consider the following fragment of C code:

```
for (i=0; i<=100; i=i+1) { V[i] = V[i] + W[i]; }
```

Assume that V and W are arrays of words and the base address of V is in $a0 and the base address of W is in $a1. Register $t0 is associated with variable i. Answer each of following instructions:
1. Write the code in MIPS.
2. How many instructions are executed during the running of this code?
3. How many memory data references will be made during execution?

```
            add    $s0, $s0, 1      ; Add 1 to N to exit when s0=0
Loop:       sub    $s0, $s0, 1      ; decrement N
            sub    $t0, $t0, 4      ; increment the index i by 4
            add    $t2, $t1, 1      ; evaluate pointer i for V[]
            add    $t4, $t3, 4      ; evaluate pointer i for W[]
            Lw     $t5, 0($t2)      ; load array element V[i]
            Lw     $t6, 0($t4)      ; load array element W[i]
            Add    $t5, $t5, $t6    ; compute V[i]= V[i]+ W[i]
            Sw     $t5, 0($t2)      ; store the value of V[i]+ W[i]
            bneq   $s0, $zero, loop ; Loop if N is not zero
```

The number of instructions are executed during the running of this code is 9x100+1=901
 The number of memory data references made during execution is 3*100=300

QUESTION 4: Internet search (No solution will be provided)

Search on the Internet for current technology on the following issues:
1. The RISC and CISC architectures, comparing them, and giving examples of processors from each class.
2. The most recent PC-based DRAM technology, and determine its most important functional features.
3. The most recent PC-based INTEL microprocessor, summarize its architecture, determine its most important functional features, and present the type of services that are targeted by its design.

For each of the above the student is expected to summarize his finding and attach a copy of the referenced papers.