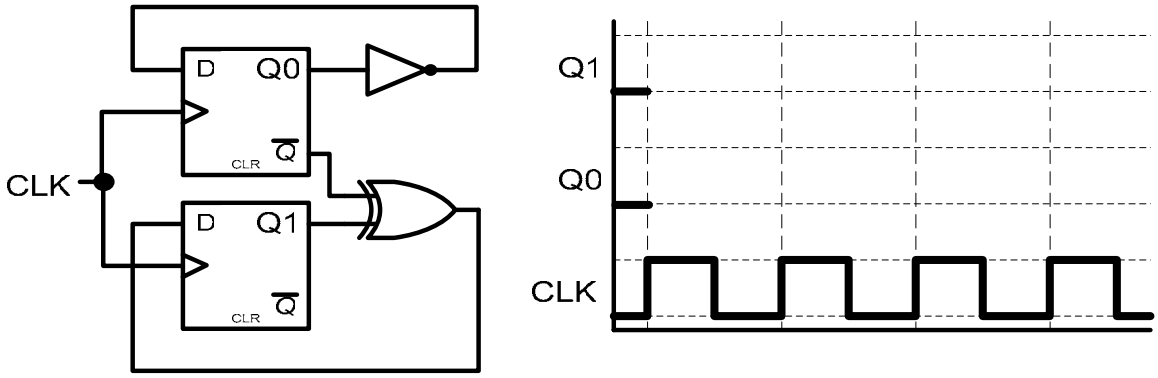
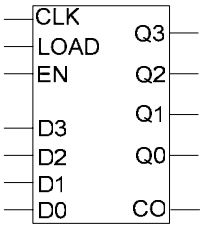
Synchronous Sequential Circuit Problems

Problem # 1: Two positive edge-triggered D flip-flops are connected as shown in the figure. Both flip-flops are initialized to 0 at the beginning. Fill in the timing diagram for the two outputs Q1 and Q0.



Problem # 2: Use as many as necessary of the following counter with minimal external gates to design a counter that counts from 0 to 20.



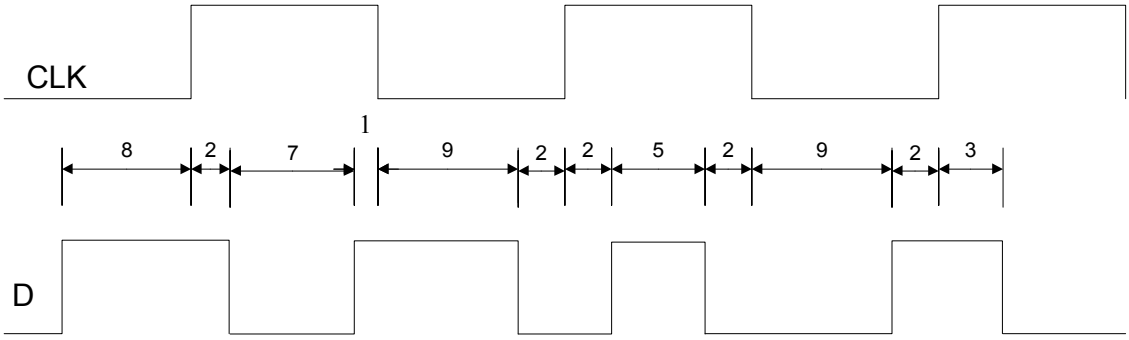
Synchronous Sequential Circuit Problems

Question 1

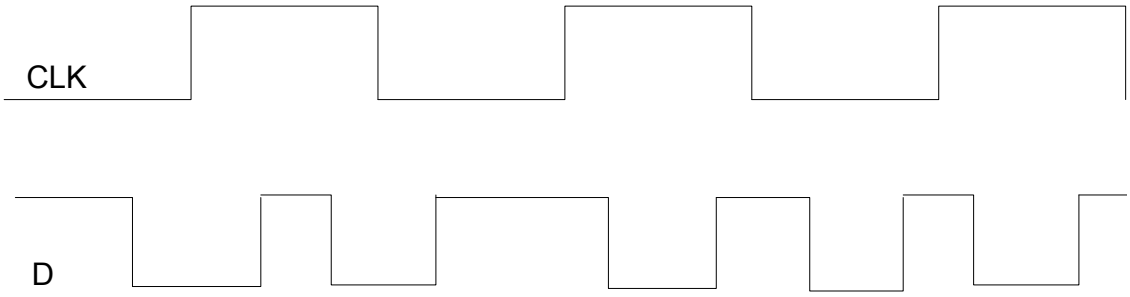
Draw the Mealy state diagram and state table for a serial even parity checker. The circuit receives a word of 4-bits serially on its single input X and produces the even parity bit after the fourth bit is received. The single output Z remains 0 except when the final (fourth) bit is received and the total number of 1's in the word is odd. The machine returns to the reset initial state after the 4th input bit. ~~Using the state assignment heuristics, indicate a possible good state assignment~~ (show all your work).

Question 2

A +ive edge triggered D-FF has a setup time of 2 ns and a hold time of 3 ns. If the waveforms shown below are applied to this FF, ***circle*** the timing violations and ***label*** them with the letters ***S*** or ***H*** depending on whether the violations are setup or hold time violations.



A level sensitive D-latch has a setup time of 3 ns and a hold time of 2 ns. If the waveforms shown below are applied to this FF, ***draw*** the output waveform (Q) and ***mark*** the timing constraints you would place on the D-input to satisfy the minimum setup & hold times. Assume that the initial FF-state is Q = 1.



Question 3

a) Write the excitation tables of the D and the JK Ffs
b) Design the synchronous sequential circuit whose state transition table is shown below. Use a D-FF to implement y0 and a JK-FF to implement y1.

PS y1 y0	**NS , out Y1 Y0 , Z**	
	x = 0	**x = 1**
0 0	0 1 , 0	0 1 , 0
0 1	1 1 , 0	0 0 , 1
1 1	0 1 , 0	1 0 , 0
1 0	1 1 , 0	0 1 , 1

Question 4

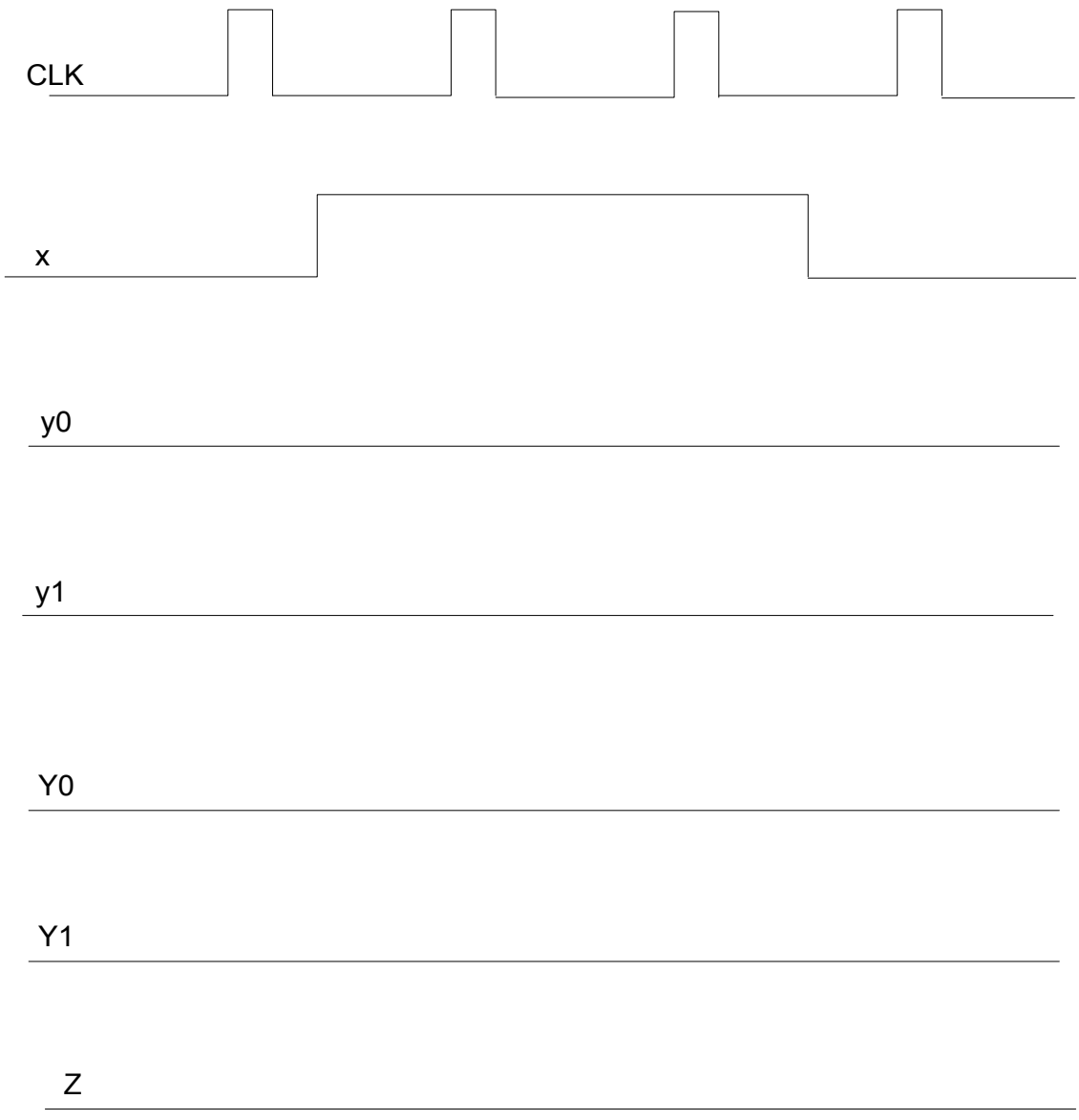
Draw the state diagram of the Moore machine which has 2 inputs (X1, X2) and one output Z. The output of the machine is determined by the following:

Z ***does not change*** its value if X1 X2 = 00
Z becomes **1** if X1 X2 = 01
Z becomes **0** if X1 X2 = 10
Z ***change its value*** if two consecutive 11 are received at the inputs X1X2
The reset input initializes the machine to a 0 output.

Question 5

The state transition table of state machine with a single input x and a single output Z is shown below. Draw the present state variables the next state variables, and the output Z for the shown input waveform x.

PS y1 y0	NS Y1, Y2 x=0	NS Y1, Y2 x=1	Output (Z)
0 0	0 0	0 1	0
0 1	1 0	1 1	1
1 1	0 1	1 1	0
1 0	0 1	1 1	1



Question 6

Draw the Mealy state diagram and state table for a serial even parity checker. The circuit receives a word of 4-bits serially on its single input X and produces the even parity bit after the fourth bit is received. The single output Z remains 0 except when the final (fourth) bit is received and the total number of 1's in the word is odd. The machine returns to the reset initial state after the 4th input bit. ~~Using the state assignment heuristics, indicate a possible good state assignment~~ (show all your work).

Question 7

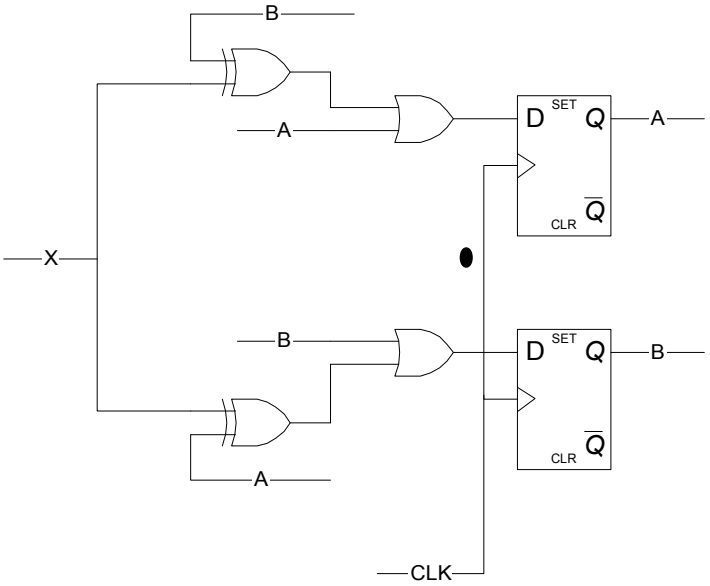
A synchronous sequential circuit has two inputs X_1X_2 representing a binary number, N. If the present value of N is greater than the previous value, then the two output bits Z_1Z_2 =10. If the present value of N is less than the previous value then the output Z_1Z_2 =01, otherwise Z_1Z_2 =00.

Derive the Mealy state diagram (*Hint*: The machine needs only five states).

Derive the Moore state diagram (*Hint*: The machine needs at least 11 states).

Question 8

Derive the state table and state diagram of the synchronous sequential circuit shown (X is an input to the circuit). Explain the circuit function.



Question 9

An up-down mod-4 binary counter has a single input x, such that the it counts up if x=0 and counts down if x=1:

Draw the Mealy state diagram of the circuit.

Draw the state Moore diagram of the circuit.

Implement both circuits using *negative-edge triggered* D-FFs.

For the shown input waveforms, draw the present state variables, the output variables and next state variables (D-inputs of the FFs) in both implementations (Mealy & Moore). Assume *zero propagation delay* and an initial count of 00

How the two sets of waveforms are different ? Explain.