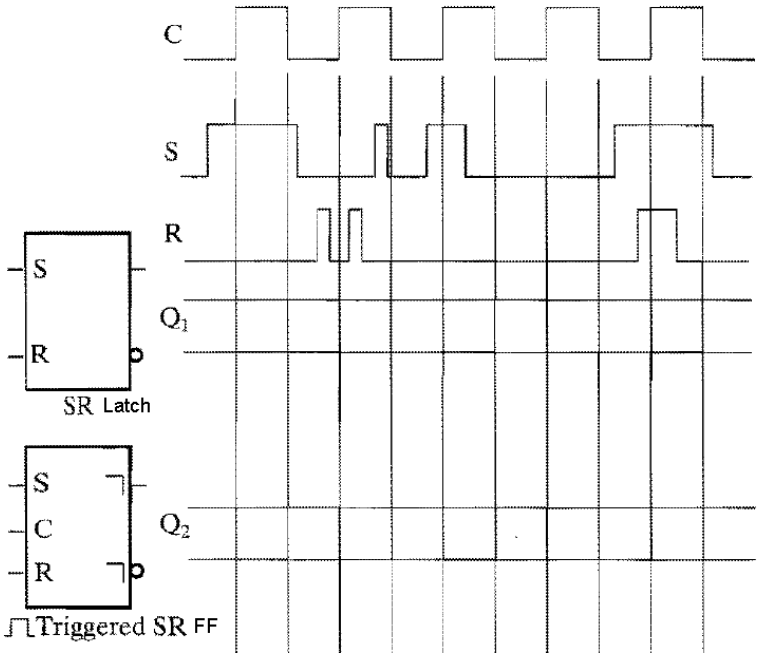
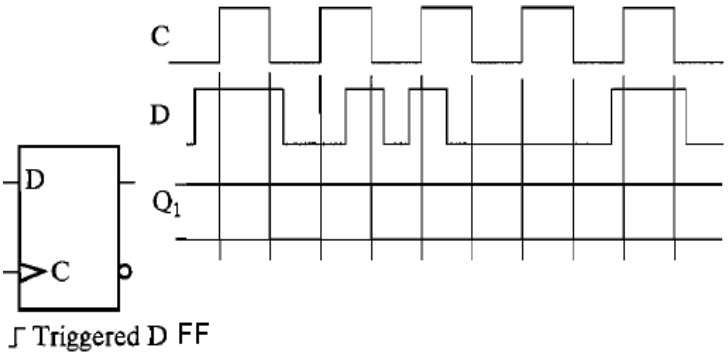
COE 202.03 (Term 101)
HW # 7: Tue 4 January 2011: Due at class time on Mon 10 Jan 2011
Note: All references to the textbook refer to Mano & Kime, 4th Ed., 2008

1. Carefully sketch the Q waveforms for each of the latches/flip flops below for the given input and clock signals.

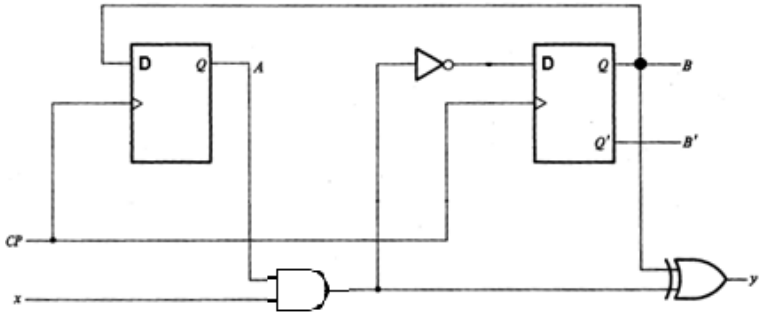


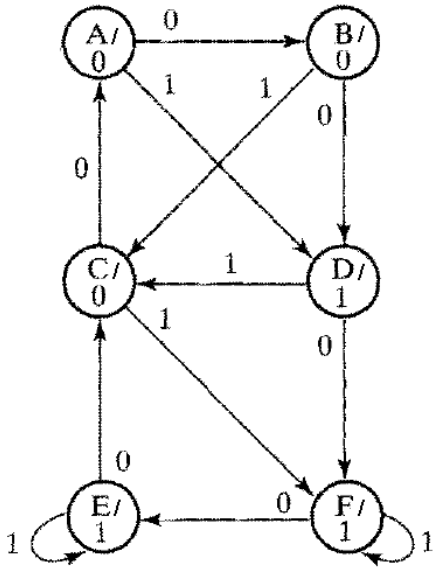

2. Solve Problem 5-6 on page 299 of the textbook. In part (b) provide both the 2-D and the 1-D state tables.

3. Analyze the sequential circuit in the figure opposite and determine its performance in the form of:

a. A one-dimensional state table.
b. A two-dimensional state table.
c. A state diagram




4. Refer to the state diagram opposite and answer the following questions:




a. Is the circuit Mealy or Moore type?
b. How many states, flip-flops, external inputs, and external outputs?
c. Using the symbolic states indicated, express the state diagram as:
- A 2-dimensional state table.
- A 1-dimensional state table.
e. Rewrite the 1-diemnsional state table after making state assignments that give states A to F the sequence of binary numbers starting at 0, i.e. A = 0, B = 1, C = 2, etc. respectively.
f. Design the circuit using D flip-flops that have direct S, R inputs. Use the 1-dimensional state table in (e) to optimize the flip flop inputs and the external output(s) using K-maps. Assume that unused states are don't care conditions. Give optimized SOP Boolean expressions. Make optimum utilization of the don't care conditions for the combinational logic outputs.
g. Give a complete logic diagram for the sequential machine. Include an external asynchronous INITIALIZE input that initializes the machine in state C.

5. We would like to design a sequential circuit that dynamically detects the occurrence of the sequence 10011 at its single external input. The output of the circuit will be normally 1, going to 0 only when the sequence is detected. For each of a Mealy and a Moore implementation of the circuit, give:

a. A state diagram, marking states symbolically as A, B, C, etc.
b. The number of states, state variables, flip flops.

6.
a. Give the binary state table for a 3-bit down (decrementing) counter starting from state 111 as the present state. The counter goes through the counting sequence 7, 6, 5, 4, 3, 2, 1, 0, 7, … etc. Assume state variables are ABC (where C is the LSB)
b. Use a K-map to obtain an optimized SOP logic expression for bit B of the counter.