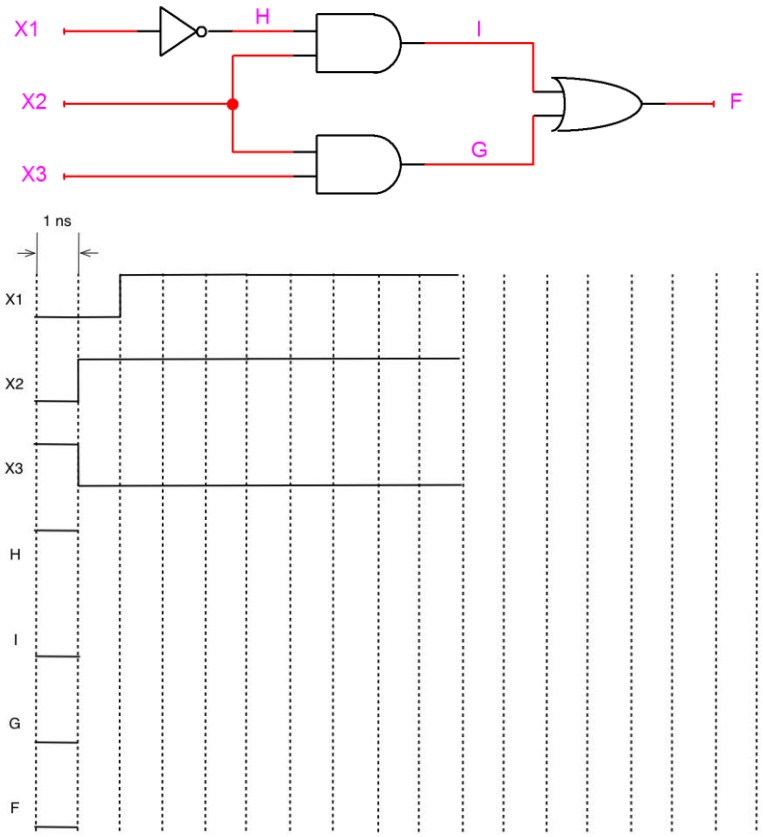
King Fahd University of Petroleum and Minerals
College of Computer Sciences and Engineering
Department of Computer Engineering

COE 202 – Digital Logic Design (T161)

Verilog Assignment # 01 (*due date & time: Tuesday 01/11/2016 during class period*)

Using a Verilog simulator, build the code for the following circuit and simulate it for the given timing diagram. Assume that the propagation delays through the NOT, AND, and OR gates are 1 ns, 2 ns, and 3 ns, respectively. You can verify your results by checking the solution for question 5 of major exam 1 of T131.
(link to solution: http://faculty.kfupm.edu.sa/coe/aimane/coe202/Maj1sol-202-T131.pdf)



Save your simulation code and an image of the timing diagram results as a Word document and name the file "*Verilog01_yourStudentID.doc*".

Deliverables:

1. Send a soft copy of your Word file to both myself (marwan@kfupm.edu.sa) and the grader (s201381710@kfupm.edu.sa) with the "subject" line being "*COE202-Verilog01-yourStudentID*".
2. Submit a printout (i.e., hard copy) of your Word file. Make sure that both the sets of inputs and the sets of outputs show up in the timing diagram results printout.

IMPORTANT: The simulation code and the timing diagram results developed and submitted should be the result of **your own individual genuine effort**. I follow a zero tolerance policy regarding plagiarism.