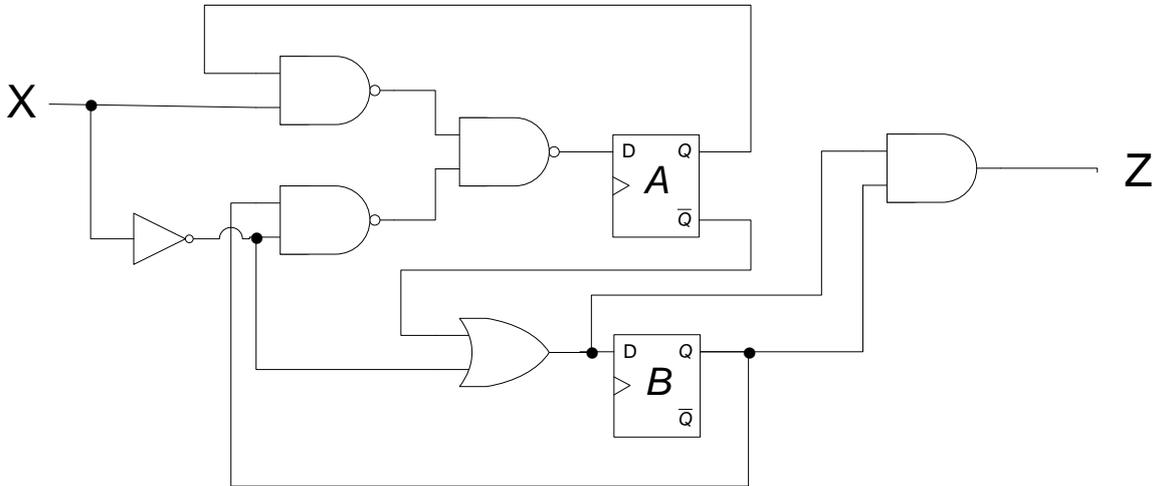


King Fahd University of Petroleum and Minerals
 College of Computer Sciences and Engineering
 Department of Computer Engineering
 COE 202 – Digital Logic Design (T131)

Homework # 05 (due date & time: Sunday 15/12/2013 during class period)

*** Show all your work. No credit will be given if work is not shown! ***

Problem # 1 (40 points): Drive the state diagram for the following circuit (show all the steps of your work):



Problem # 2 (40 points): Design a *Moore* sequential circuit that will be used in a vending machine that dispenses 20 SR account recharging cards for prepaid phones (e.g., SAWA, Mobily, Zain). The circuit can only accept 10 SR and 50 SR bills (i.e., cannot accept 1 SR, 5 SR, 20 SR, 100 SR, 200 SR, 500 SR bills), and can only accept one bill at a time (i.e., cannot accept 2 or more bills at the same time). The circuit should have 2 outputs. One output will be set to 1 when the circuit is ready to dispense the card (i.e., sufficient funds were deposited), while the other output will be set to 1 when the circuit needs to return the change, if any, to the customer. Use rising-edge triggered *D* flip-flop(s) and a non-inverted outputs decoder to design the circuit. **Show all steps of the design including state reductions, if any.**

Problem # 3 (20 points): In the circuit shown, the component at the top is a D-type flip flop and the component at the bottom is a clocked D-latch. Plot the waveforms at outputs Q1 and Q2 for the clock and external input waveforms indicated. Assume that both components were initially reset (i.e., Q1 = Q2 = 0).

