

King Fahd University of Petroleum and Minerals
College of Computer Sciences and Engineering
Department of Computer Engineering

COE 202 – Digital Logic Design (T131)

CAD Assignment # 01 (due date & time: Tuesday 19/11/2013 during class period)

Using the “LogicWorks” tool, build the circuit of Problem # 3 of Homework # 03 with only **NOR** gates. Label all inputs and outputs. Verify that your circuit is functioning properly by applying all input combinations.

Save your circuit and name the file “CAD01_yourStudentID.cct”.

Deliverables:

1. Send a **soft copy** of your circuit file to both myself (marwan@kfupm.edu.sa) and the grader (g200376970@kfupm.edu.sa) with the “subject” line being “COE202-CAD01-yourStudentID”.
2. Submit a **printout of the circuit window**. Make sure that the entire circuit appears in the printout.
3. Submit a **printout of the timing window** after applying all input combinations. Make sure to zoom-in as far as you can inside the timing window before printing. Also, make sure that both the sets of inputs and the sets of outputs show up in the printout.