King Fahd University of Petroleum and Minerals
College of Computer Sciences and Engineering
Department of Computer Engineering

COE 202 – Digital Logic Design (T112)

Homework # 03 (*due date & time: Wednesday 14/03/2012 during class period*)

***** Show all your work. No credit will be given if work is not shown! *****

Problem 1 (30 points): Consider the Boolean function F(A, B, C, D)=Σ m(0, 1, 2, 5, 6, 7, 8, 9, 10, 12, 13). Find the following:

1. Identify all the *prime implicants* and the *essential prime implicants* of F.
2. Simplify the Boolean function **F** into a minimal sum-of-products expression.
3. Simplify the Boolean function **F** into a minimal product-of-sums expression.

Problem 2 (30 points): Consider the Boolean function **F**(A, B, C, D)=Σ m(0, 2, 5, 8, 10), together with the don't care conditions **d**(A, B, C, D)=Σ m(1, 4, 7, 9, 11, 12, 14, 15). Find the following:

1. Simplify the Boolean function **F** together with the don't care conditions **d,** into minimal sum-of-products expression.
2. Starting with the sum-of-products expression, implement the function using only **NAND** gates and **Inverters**.
3. Starting with the sum-of-products expression, implement the function using only **NOR** gates and **Inverters**.

Problem 3 (40 points): Design a 3-bit decrementer using **only NAND gates**. The circuit takes a 3-bit unsigned number $\mathbf{I=I_2I_1I_0}$ as input and generates a 3-bit output number $\mathbf{Z = Z_2Z_1Z_0}$ and a **Valid** output **V.** Whenever **I > 0** the output **Z = I-1** and **V=1**. If **I=0**, the output is invalid which is indicated by an output **V=0.** Derive the simplified Boolean expressions of all outputs, and show the logic diagram implementation of the **all NAND gates** circuit.