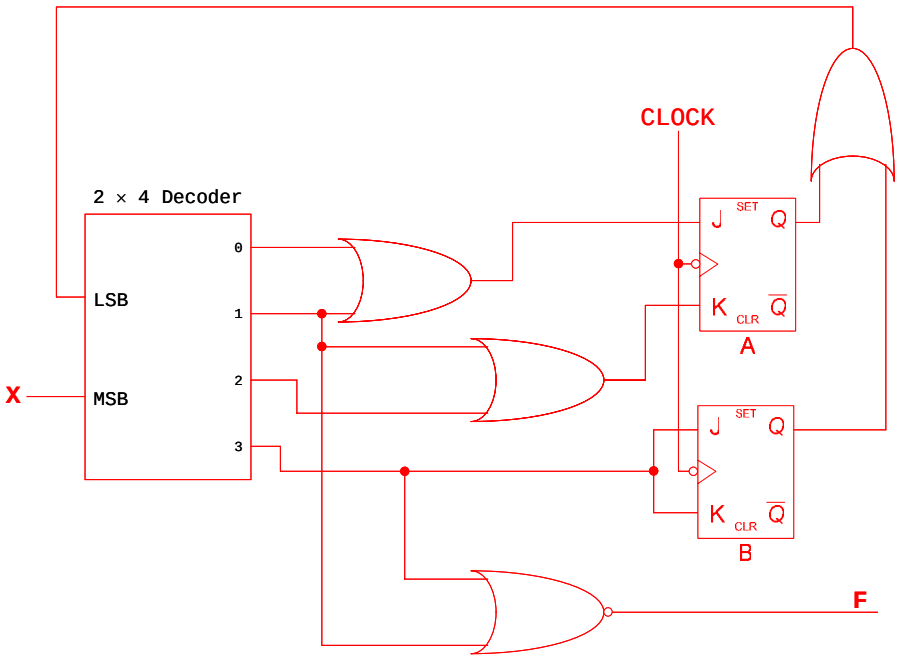
King Fahd University of Petroleum and Minerals
College of Computer Sciences and Engineering
Department of Computer Engineering

COE 202 – Fundamentals of Computer Engineering (T081)

Homework # 05 (*due date & time: Saturday 17/01/2009 during class period*)

***** Show all your work. No credit will be given if work is not shown! *****

Problem # 1 (50 points): Drive the state diagram for the following circuit (show all the steps of your work):



Problem # 2 (50 points): Design a *Mealy* sequential circuit that receives data serially on input *X* and produces an output *Y*. The output *Y* is equal to 1 when **all** of the following three conditions are satisfied:

1. The input sequence "10" is detected at least once.
2. At least one "1" is received since the sequence "10" was detected.
3. The total number of "1"s received so far is *odd*.

Use rising-edge triggered *JK* flip-flop(s) and a non-inverted decoder to design the circuit. **Show all steps of the design including state minimization**. The following are sample traces to help you in the design of the state diagram as well as verifying your final design:

1. Trace 1:
   X = 00**10**1**1**110011…
   Y = 000001011101…

2. Trace 2:
   X = 001**10**00**1**1110011…
   Y = 000000010100010…