King Fahd University of Petroleum and Minerals
College of Computer Sciences and Engineering
Department of Computer Engineering

COE 202 Digital Logic Design (3-0-3)

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Term: 112 (2nd term 2011–2012)
Day & Time: SMW 08:00 AM – 08:50 AM
Location: 24-156
Textbook: *Logic and Computer Design Fundamentals*, Morris Mano and Charles Kime, Fourth Edition, Prentice Hall International, 2008.
Office Hours: SMW 11:00 AM – 11:50 AM (or by appointment)
Web Site: http://faculty.kfupm.edu.sa/COE/marwan

Tentative Grading Policy:

- Homeworks **10%** (Each homework may carry a different weight)
- CAD Assignments **5%** (Each CAD assignment may carry a different weight)
- Quizzes **10%** (Each quiz may carry a different weight)
- Major Exam I **20%** (Thursday March 1, 2012, 1:00 PM)
- Major Exam II **25%** (Thursday April 12, 2012, 1:00 PM)
- Final Exam **30%** (Monday May 28, 2012, 7:00 PM)

Course Learning Outcomes

1. Ability to use math and Boolean algebra in performing computations in various number systems and simplification of Boolean algebraic expressions.
2. Ability to design efficient combinational and sequential logic circuit implementations from functional description of digital systems.
3. Ability to use CAD tools to simulate and verify logic circuits.

IMPORTANT NOTES:

- All KFUPM regulations and standards will be enforced. Attendance will be checked each class. The KFUPM rule pertaining to a DN grade will be strictly enforced (i.e. > **9 absences** will result in a DN grade). *Check your university e-mail regularly for warnings regarding your absences.*
- If you are late to the class for more than 5 minutes (i.e. arrive after 08:05 AM), you will **NOT be allowed to enter** the classroom and you will be considered absent for that class.
- Only university approved/certified excuses will be accepted, and should be presented **no later than 1 week** after absence.
- Use of cell phones and PDAs during class period and during exams is absolutely **prohibited**.
- Homeworks are to be submitted **in class** on the due date during the class period. Late homeworks will **NOT be accepted**.
- You have 48 hours to object to the grade of a homework, a quiz, or a major exam from the end of the class time in which the graded papers have been distributed back. If for some reason you cannot contact me within this period, send me an email requesting an appointment. The email should be sent within the 48-hour time period.
- **NO make up exams**. ALL homeworks and quizzes will be counted towards your grade.
- Final exam is **comprehensive & common**.

Tentative schedule:

Week	Topics
1	• Introduction: Information processing, and representation, Digital vs Analog quantities, Number systems: Binary system • Weighted Number Systems: Decimal, Binary, Octal and Hexadecimal • Arithmetic in Binary and Hex (addition, subtraction, multiplication) • Number base conversion (Dec to Bin, Oct, and Hex, General)
2	• BCD Codes: Excess-3 & other BCD codes, Parity Bits. • Binary logic and gates, Truth tables, Boolean Algebra, Basic identities. Principle of duality. • DeMorgan's Theorem. • Manipulation of Boolean expressions. • Gate Implementation of Boolean expressions
3	• Canonical and Standard forms, Minterms, Maxterms, Sum of products & Products of Sums. • 2-Level gate implementation (SOP, POS). • From Truth tables to Boolean Expressions. • Physical properties of gates: fan-in, fan-out, propagation delay. Timing diagrams. Tri-state drivers.
4-5	• K-Map method of simplification: 2, 3 and 4-variable maps. Implicants, Prime Implicants, Essential Prime Implicants. • POS simplification. • Don't care conditions and simplification. • Universal gates (NAND, NOR) • Implementation using NAND and NOR gates: 2-level & Multilevel implementation. • Exclusive-OR (XOR) and Equivalence (XNOR) gates, Odd and Even Functions, Parity generation and checking.
6-7	• Combinational Circuit Design Procedure & Examples. • Code Converter. • BCD to 7-Segment Display Conversion. • Half and Full Adders. • Ripple Carry Adder (RCA) design and Delay analysis of RCA • Signed Numbers: sign-magnitude, 1`s complement, and 2`s complement. • Signed Binary Arithmetic. (Addition and Subtraction). • Binary Adder-Subtractor. • Carry Look-ahead adder. • Delay analysis
8-9	• Decoders 2x4, 3x8, 4x16. Designing large decoders from smaller decoders. Function implementation using decoders. • Encoders: Priority Encoders. • Multiplexers: 2x1, 4x1. Constructing large MUXs from smaller ones. • Function implementation using multiplexers. • Magnitude Comparator • MSI Design Examples
10	• Sequential Circuits: Latches, Clocked latches: SR, D, T and JK. Race problem in clocked JK-Latch. • Flip-Flops: Master-Slave, D-FF. • Using D-FF to build other flip-flops.
11	• Asynchronous/Direct Clear and Set Inputs. Setup, Hold, FF propagation delay. • Sequential Circuit Design. Design procedure, State diagrams and state tables. • Analysis of Sequential Circuits. State table, State diagram.
12	• Mealy vs. Moore machine • Design Examples and Calculation of maximum clock frequency
13	• Registers, Registers with parallel load. • Synchronous Binary Counters: Up-Down Counters • Counters with Parallel load, enable, synchronous clear and asynchronous clear. • Use of available counters to build counters of different count. • Design with unused States • Shift Registers. Bi-directional shift register.
14	• Memory devices: RAMs & ROMs • Combinational Circuit Implementation with ROMs • Sequential Circuit Implementation using ROMs • Programmable Logic Devices: PLAs, PALs, FPGA'a
15	• ***Review***