King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)
Term 101 (Fall 2010)
Major Exam 2
Sunday, December 26th, 2010

Time: 120 minutes

Name:_____ ID:_____ Section: _____

Notes:

- Do not open the exam book until instructed
- Calculators are not allowed (basic, advanced, cell phones, etc.)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

Question	Maximum Points	Your Points
1	10	
2	10	
3	20	
4	15	
5	15	
6	20	
Total	90	

Question 1. **(10 points)**

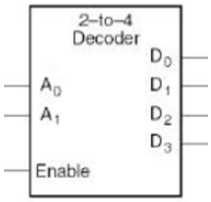
Fill in the Spaces: (Show all work done to reach your answer)

a. For a 4-input function, F (A, B, C, D), which of the following expressions represents the prime implicant having the largest area on the function's K-map?:

(i) AB+C+CD
(ii) $ABC\overline{D}$
(iii) $\overline{A}C$

b. The symbol  is an equivalent representation of the _____ gate.

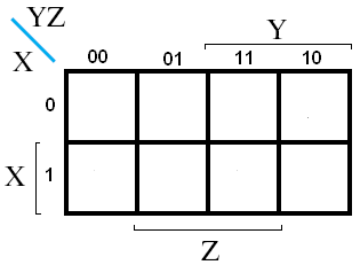
c. Given five 2-to-4 decoders with Enable (similar to the one shown opposite), the largest decoder we can build without any additional components is a _____-to-_____ decoder.



d. For XYZ = 100, the function $F(X, Y, Z) = X \oplus Y \oplus Z$ is _____(0/1). This function can be used to generate and detect _____ even/odd parity in digital communications.

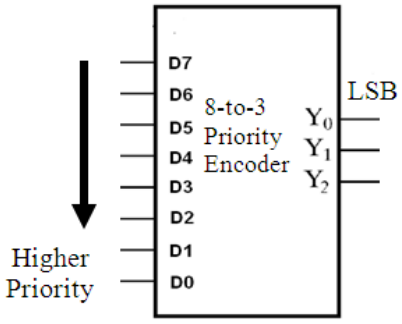
e. Represent the function F(X,Y,Z) given below on the opposite K-map:

$$F(X,Y,Z) = (\overline{X} + Z).(X + Y + \overline{Z}).(X + \overline{Y} + Z)$$



f. In the priority encoder shown opposite, the output $Y_2Y_1Y_0$ = 101. Circle any statements that can correctly describe the status at inputs D0-D7, with all other inputs being in a don't care condition:

i. D3 = 1 and D5 = 1
ii. D6 = 1 and D5 = 1
iii. D1 = 1 and D2 = 1
iv. D0 = 1 and D2 = 1



Question 2. **(10 Points)**

We would like to design a combinational circuit that takes as input a 3-bit unsigned binary number **X** and produces two binary numbers **Y** and **Z** as outputs which together represent the result of dividing the input number **X** by 3, where **Y** is the quotient and **Z** is the remainder.

a. List in the first 3 columns in the table below all possible values for **X** and the corresponding values for **Y** and **Z** (all in decimal).

b. The minimum number of bits needed to represent the output number **Y** is _____(how many) bits and the minimum number of bits needed to represent the output number **Z** is _____(how many) bits.

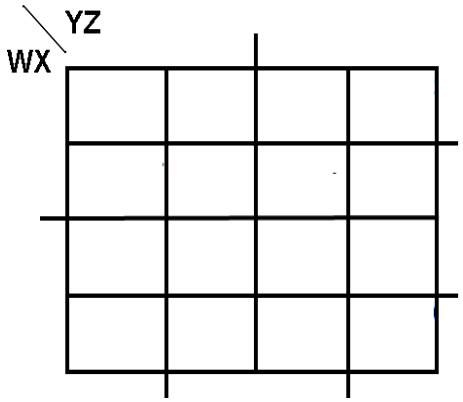
c. In the next two columns of the table below, provide the binary truth table for the circuit, showing the bits of the inputs and outputs, with the MSB on the left in each case. Represent the outputs with the minimum number of bits obtained in (b) above. Show **Y** and **Z** bits appended together with **Y** at the left. Express the bit combination **Y:Z** in hex in the last column.

Input **X** (Decimal)	Output **Y** (Decimal)	Output **Z** (Decimal)	Input **X** (Binary)	Output **Y:Z** (Binary)	Output **Y:Z** (Hex)

Question 3. **(20 Points)**

Consider the function $F(W,X,Y,Z) = \overline{W}\,Y\,Z + \overline{W}\,\overline{Z} + W\,Y\,Z$

a. Represent the function on the K-map opposite, showing both the 1s and 0s of the function.



b. Express $F(W,X,Y,Z) = \Sigma m($_____$)$

c. Express $F(W,X,Y,Z) = \Pi M($_____$)$

d. Use the K-map to minimize the expression above for F to 4 literals

e. Draw the logic diagram for a 2-level implementation of $F(W,X,Y,Z) = \overline{W}\,Y\,Z + \overline{W}\,\overline{Z} + W\,Y\,Z$ using only NAND gates. Assume that both the true and complemented forms of each variable are readily available.

Question 4. **(15 Points)**

Given the following K-map for a function *F*:

AB \ CD	00	01	11	10
00				
01	1	1		
11	1		1	1
10		1	1	1

(a) List all Essential Prime Implicants

(b) Provide a minimized **SOP** expression of *F*

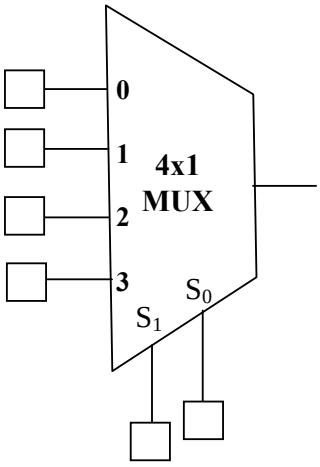
(c) Provide a minimized **POS** expression of *F*

Question 5. Given the function **(15 Points)**

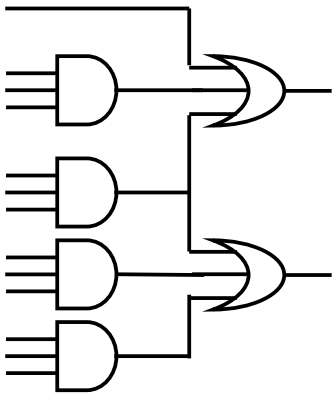
F (A,B,C) = Π M (0,1,3,4,6,7)

a. Implement F using two 2-to-4 decoders (each has an enable En input), an inverter and a NOR.

b. Implement F using the 4-to-1 MUX shown below. Show how you obtained your solution.



c. Convert the following logic circuit to NAND-only:



Question 6. **(20 Points)**

Use any number of the following MSI components: **inverters, decoders, encoders, multiplexers, adders, and/or magnitude comparators**, to design a circuit that takes two 4-bit binary numbers $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$ and a 2-bit user selection input $S = S_1S_0$. The circuit should produce a 5-bit output $O = O_4O_3O_2O_1O_0$ according to the following table:

S_1S_0	O is equal to
00	Max(A, B)
01	Min(A, B)
10	$2 \times A$
11	$A - B$

Note that you must clearly label the MSI part used together with all inputs and outputs.