

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING
COMPUTER ENGINEERING DEPARTMENT
COE 200 Fundamentals of Computer Engineering
Syllabus Term 032

Catalog Description

Introduction to Computer Engineering. Digital Circuits. Boolean algebra and switching theory. Manipulation and minimization of Boolean functions. Combinational circuits analysis and design, multiplexers, decoders and adders. Sequential circuit analysis and design, basic flip-flops, clocking and edge-triggering, registers, counters, timing sequences, state assignment and reduction techniques. Register transfer level operations. (*Prerequisite: PHYS 102*)

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Text Book: Mano and Kime, *Logic and Computer Design Fundamentals*, Second Edition, Prentice Hall International, 2000.

Grading Policy: Laboratory=20%, Attendance, Class work & Quizzes=15%, Exam I=20%, Exam II=20%, Final=25%

Week	Course Topics	Ref
Number System and Codes		
1	Introduction. Information Processing, and representation. Digital vs Analog	1.1
	Number Systems. Binary, octal and hexadecimal numbers	1.2, 1.3
2	Number base conversion (Dec to Bin, Oct, and Hex, General), Conv (Bin, OCT, Hex), Binary & other System Arith.	1.3
	Signed Binary Number representation, Signed Mag, R's & (R-1)'s Complement	1.3
3	Signed Binary Addition and Subtraction. R's & (R-1)'s Complement Signed Binary Addition and Subtraction. R's & (R-1)'s Complement, Codes. BCD, Excess-3, Parity Bits, ASCII & Uni-Codes	1.4, 1.5
Binary Logic & Gates		
4	Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra. Boolean functions, Algebraic manipulation, Complement of a function. Canonical and Standard forms, Minterms and Maxterms, Sum of products and Products of Sums.	2.1, 2.2, 2.3
5	<i>Map method of simplification:</i> Two-, Three-, Four-variable K-Map, and Five -variable K-Map	2.4
6	<i>Map manipulation:</i> Essential prime implicants, Nonessential prime implicants, Simplification procedure.	2.5
	Don't care conditions and Simplification Universal gates; <i>NAND and NOR gates:</i> 2-level implementation.	2.5, 2.6
7	<i>Multilevel NAND Circuits.</i>	2.6
	Exclusive-OR (XOR) and Equivalence (XNOR) gates, Parity generation and checking.	2.7
Combinational Logic		
	Combinational Logic, Design procedure. BCD-to-Excess 3 code Conversion.	3.4
8	BCD-to- 7 Seg. Display. Half and Full Adders.	3.4, 3.8
	Design using MSI parts. Decoders, Decoder Expansion. Combinational Circuit implementation using decoders.	3.5
	Encoders & Priority Encoders <i>Magnitude Comparator.</i>	3.6
9	Multiplexers. Function Implementation using multiplexers, Demultiplexers	3.7
	<i>Binary Adders: 4-Bit Ripple Carry Adder, Carry Look-Ahead Adder, Binary Adder-Subtractor.</i>	3.8, 3.10
	BCD Adder, Binary Multiplier.	3.11, 3.12
Sequential Circuits		
10	<i>Sequential Circuits:</i> Latches, SR and D-latch, Clocked latch.	4.1, 4.2
	<i>Flip-Flops:</i> Master-Slave, Edge-Triggered. <i>Timing Diagrams</i>	4.3
11	<i>Flip-Flops Characteristic & Excitation Tables:</i> D-FF, SR-FF, JK-FF, T-FF.. <i>Asynchronous/Direct Clear and Set Inputs</i>	4.3
	Setup, Hold, Enable times. Timing control and Clocks. Path delay constraints. <i>Sequential Circuit Design:</i> Design procedure, Construction of state diagrams and state tables.	4.5
12	Designing with D-FFs & JK-FFs. Designing with unused states. Sequential Circuit Design Examples.	4.6, 4.7
13	<i>Sequential Circuit Analysis:</i> Input equations, State table.	4.4
Registers & Counters		
	Registers, Registers with parallel load, Shift Registers.	5.2, 5.3
	Shift register with parallel load, Bi-directional shift register.	5.3
14	<i>Ripple Counters:</i> Up-Down Counters. Synchronous Binary Counters: <i>Counters with JK-FF, and D-FF.</i>	5.4
	<i>Serial and Parallel Counter, Up-Down Binary Counter, Binary Counter with Parallel Load.</i>	5.5
	Other Counters: BCD Counter, Arbitrary Count Sequence.	5.5
Memory & PLDs		
15	<i>Memory and Programmable Logic Devices:</i> Read-Only Memory. Combinational Circuit with ROM.	6.1, 6.6
	Programmable logic Array, Programmable Array logic. Programmable Logic Devices and FPGAs	6.7, 6.8, 6.9