A Portable High-Frequency Digitally Controlled Oscillator (DCO)

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ABSTRACT
A novel digitally-controlled oscillator (DCO) is reported. Utilizing a new capacitive load, the new DCO is capable of producing much higher output frequencies than existing DCOs. All other components are fully digital and modular, allowing portability to any CMOS process and customization for different applications. At the heart of the DCO is a digital ring oscillator (DRO) that utilizes the new shunt-capacitive loads. Unprecedented higher frequencies are obtained through a novel idea of electrically removing the effect of un-enabled loads. Simple design conditions for achieving proper operation of the DRO are provided. Spice simulations verified the correct and superior operation of the DCO even with device mismatch. A custom layout of the DRO was generated using LFoundry's 150 nm technology. The total DRO area was found to be 418 μm^2.

Categories and Subject Descriptors
B.7.0 [**Integrated Circuits**]: General

General Terms
Performance, Design.

Keywords
Digitally-Controlled Oscillator (DCO), Systems-on-Chip (SoCs), Digital Circuits.

1. INTRODUCTION
Many applications implemented as systems-on-chip require the generation of high speed on-chip clocks with minimal area and power consumption. Analog Phase-locked loops (PLLs) can provide precise frequencies but contains analog circuits and filters that take up large chip area and can't be ported from one fabrication process to another. All-digital PLLs (ADPLLs) are more portable and have smaller area. They, however, require digital DCOs with monotonic behavior, fine frequency resolution and good period linearity.

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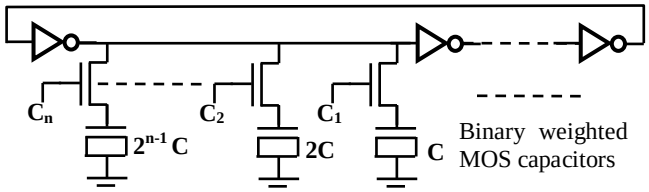
Over the years, many DCOs have been proposed. Almost all of the reported DCOs use two stages for frequency tuning; a coarse tuning stage and a fine tuning stage. This allows the DCO to have a large frequency range with fine resolution while using a minimal number of control bits. This however, may also limit the maximum output frequency of the DCO. Most of these DCOs employ one or more of the techniques illustrated in Figure 1 to change the delay. These techniques are; current-starved inverters as delay stages [1-3,9,12], inverters with switched shunt MOS capacitors [4-5, 12-13], and multiplexors to select the number of delay stages (path selection) [1,6-11]. The current starvation and path selection methods are seldom used on their own and are usually combined with other techniques (e.g. [1,9]). This is because current starvation has very limited range and path selection has very limited resolution. This means the former would require large number of delay elements (resistors) and the latter would require a large number of delay stages (inverters). For DCO's with shunt capacitors delay elements, some researchers use MOS varactors with differential drive due to their excellent linearity [12-14]. This, however, also requires a large number of delay stages due to the small capacitance of varactors.

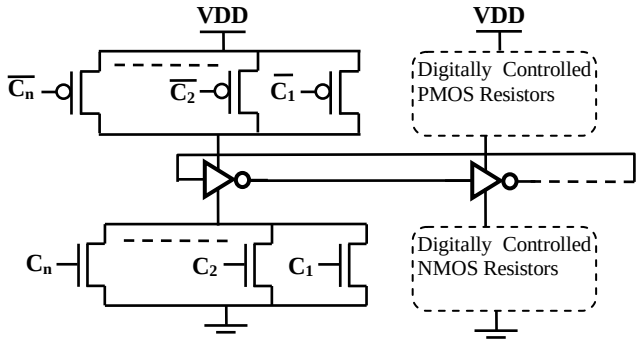
Although all the above mentioned techniques were effectively used to produce fine resolution and large frequency range with adequate linearity, they all suffer from a basic shortcoming; limited achievable maximum frequency. This is due to the fact that whatever technique is used to control the DCO's period, the elements that are used to control the delay (series resistances, shunt capacitors, or selection multiplexors) always exist in the circuit and can't be physically eliminated at the highest DCO frequency. Also, switches (NMOS, PMOS or transmission gates) controlling these elements introduce significant parasitic capacitances reducing the DCO's maximum attainable frequency further. These two issues lead to a basic trade off in all existing DCOs; in order to increase the resolution and/or frequency range, more delay elements have to be added which reduces the DCO's intrinsic (maximum) frequency. Also, in order to increase the range, the range of values of the binary-weighted resistors or capacitors (used as delay control elements in the DCO) must be increased. This causes matching problems and can lead to non-monotonic DCO frequency characteristics at some control code words. This also forces designers to use the highly non-linear MOS capacitors to be able to get large capacitance values in reasonable silicon area.

The developed DCO circuit attempts to solve these problems by electrically removing delay elements (shunt capacitors) that are not

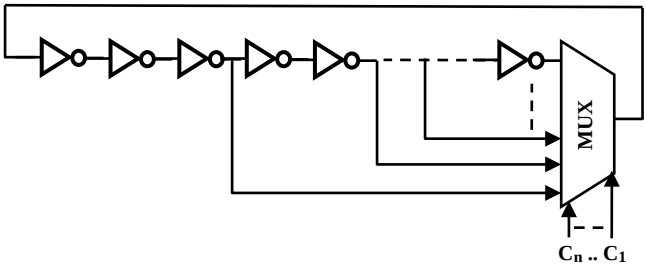
enabled by the digital control word. This allows obtaining a maximum intrinsic frequency (when the control word is all 0s) close to that of an unloaded oscillator. It also allows obtaining the desired frequency range with much smaller values of shunt capacitors. In section 2 the general architecture of the proposed DCO is introduced followed by a detailed description of the digital ring oscillator (DRO) which is the core of the DCO in section 3. Simulation results showing the superior operation of the operation of the DRO are shown in section 4. Finally, a custom layout of the new DRO is shown in section 5 to illustrate the small area of the new DRO.



(a) A Digital Oscillator based on shunt MOS capacitors.



(b) A Digital Oscillator based on current starving.



(c) A Digital Oscillator based on path selection.

Figure 1. Conventional methods for implementing DCOs.

2. DCO ARCHITECTURE

Figure 2 below shows the general architecture of the proposed DCO. It is made of a new digitally-controlled digital ring oscillator (DRO), a frequency divider (counter) and a range selection MUX. The DRO generates the basic high frequency range, the counter generates lower frequency ranges (through division by powers of 2), and the MUX provide range selection. Hence, for proper operation, the DRO frequency range must be: $f_{max} - 0.5f_{max}$, where f_{max} is the maximum frequency. This ensures continuous frequency range with the successive division by 2. As such, the required range of the DRO is relatively small, allowing for finer resolution with few bits of control word. It also means that the maximum shunt capacitance is significantly reduced, preserving DRO's signal slopes and improving linearity. The reduced range of capacitance values also makes it easier to ensure monotonicity of the oscillator with process variations.

3. THE DRO

3.1 DRO Circuitry

The DRO is made of two digital oscillators with identical inverters and a merging NAND (MNAND) gate, Figure 3. The two oscillators oscillate at the same frequency and phase. The merging NAND gate, Figure 3(b), resets the oscillators to start at the same exact moment and 'merges' the two oscillators' last-stage signals ensuring phase and frequency synchronization between the two oscillators under process variations. Newly developed, binary weighted, digitally controlled, capacitive loads are connected between each delay stage in one oscillator and the corresponding stage in the other oscillator, Fig. 3(c). As this Figure shows, a capacitive load cell is made of two identical capacitors connected in series and an NMOS switch that conditionally connects the node in between them to ground. These switches are controlled by the DCO's fine frequency control word.

3.2 Concept of Operation

Figure 4 illustrates the basic concept of the new capacitive load. When the NMOS switch is off, only its small (relative to C) drain junction capacitance (Cj) is connected between the common node and ground. Since the capacitor combination is driven from both ends with identical phase, the two inverters in the two oscillators see very small capacitances (< 0.5 Cj). When the switch is on the common node is connected to ground and each inverter sees a load of C which increases its delay while identical phase is still maintained. Hence, unlike conventional shunt capacitance schemes, this new scheme results in a large capacitance difference between the two states since there are no parasitic capacitance at the inverters' outputs. This means that the required frequency range and resolution could be obtained with small values of C and few load cells. It should be noted here that the shunt capacitances must be implemented with metal layers not MOS capacitors to avoid excessive parasitic capacitances. This however is not a problem since the required values are very small. For example, for a 3-stage DRO implemented in a 0.13 µm technology with 4-bit/stage control, the required value of C is 0.5 fF. This yields an astonishing DRO frequency range of 2.5 – 5 GHZ. The on-chip area of such a capacitor would be in the order of few square micrometers.

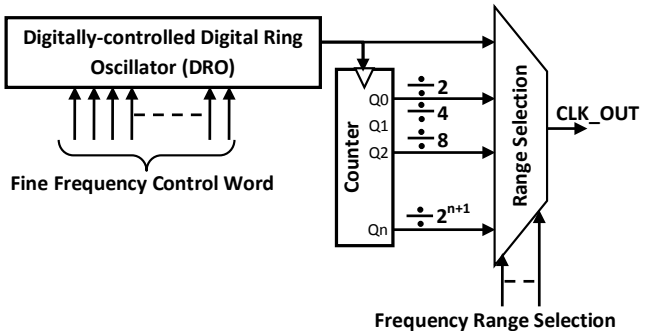


Figure 2. The general architecture of the new DCO.

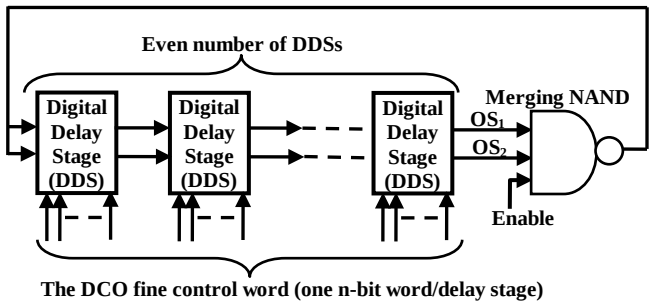
3.3 Design Constraints

For proper portability of the DRO to any fabrication process, it has to be ensured that $\mathbf{f_{max}} \geq 2\mathbf{f_{min}}$ (i.e. the frequency range is one octave). That means the maximum delay through a DRO stage must be at least twice its minimum delay, i.e. $\mathbf{TD_{max}} \geq 2\mathbf{TD_{min}}$. Also, to improve linearity of the DRO, the sizes of the NMOS switches in the capacitance cells have to be increased at the same ratio of the capacitance (i.e. binary-weighted fashion).

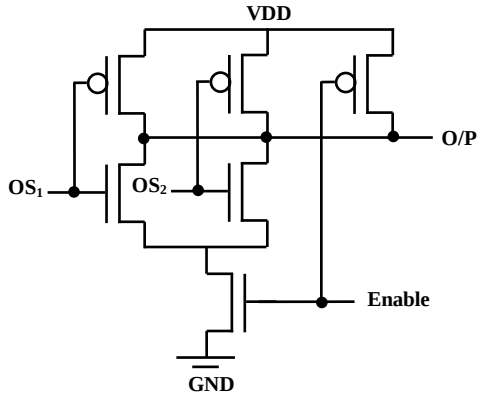
Now the minimum value of $\boldsymbol{C}$ (the unit load capacitance, Fig. 2(c)) that is needed for proper DRO operation can be estimated as follows; first, the following two equations give approximate values of $\mathbf{TD_{max}}$ and $2\mathbf{TD_{min}}$ for a 3-stage DRO based on simple RC delay model:

$$\mathbf{TD_{min}} = \mathbf{R_{eq}} * [2\mathbf{C_{in}} + 0.5*(2^{n} - 1)\,\mathbf{C_j}] \quad (1)$$

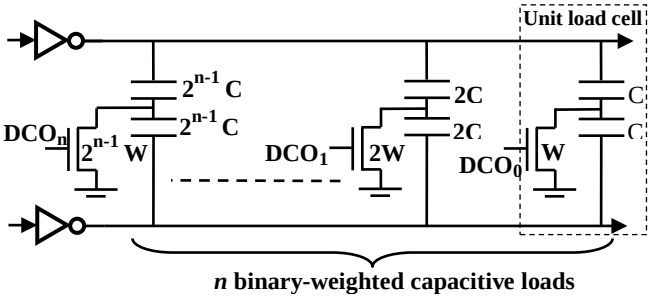
$$\mathbf{TD_{max}} = \mathbf{R_{eq}} * [2\mathbf{C_{in}} + (2^{n} - 1)\,\mathbf{C}] \quad (2)$$



(a) Basic structure of the DRO



(b) The Merging NAND gate.



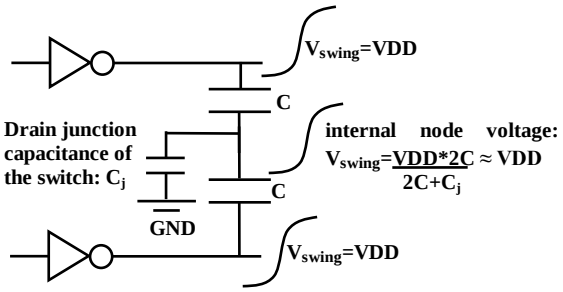
(c) A Digital Delay Stage (DDS)

Figure 3. The DRO's circuitry.

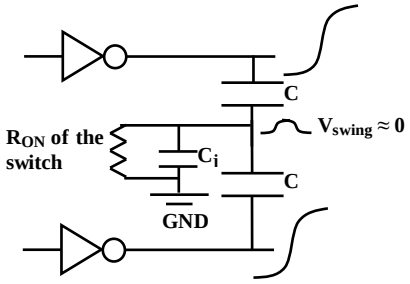
Where $\boldsymbol{R_{eq}}$ is the equivalent resistance of the CMOS inverter in the DDS, $\boldsymbol{C_{in}}$ is its input capacitance, $\boldsymbol{C_j}$ is the unit drain junction capacitance of the NMOS switch in the capacitance cell (its value is split between the two inverters), and $\boldsymbol{n}$ is the number of control bits/DDS. In (1) and (2) above, the delay of the MNAND gate (which is relatively constant) is divided among the two DDSs, hence the factor of 2 in front of $\boldsymbol{C_{in}}$. The intrinsic delay of the MNAND is approximately twice that of the inverters in the DDSs since it has twice the FanOut. So from the above equations, the condition for proper operation of the DRO is:

$$\mathbf{C} \geq \frac{2\mathbf{C_{in}} + \left(2^{n} - 1\right)\mathbf{C_j}}{\left(2^{n} - 1\right)} \quad = \quad \frac{2\mathbf{C_{in}}}{2^{n} - 1} + \mathbf{C_j}$$

For the 0.13µm, 1.2V technology used in this work, the values of $\boldsymbol{C_{in}}$ and $\boldsymbol{C_j}$ were 1.6 fF and 0.27 fF, respectively. According the condition obtained above and for 4-bit control/DDS, the value of $\boldsymbol{C}$ should be 0.48fF. The actual value found from simulations was actually 0.5fF, an excellent agreement with the predicted value.



(a) When the switch is off, each inverter sees a load capacitance ≈ $0.5(C\,C_J)/(C+C_J) < 0.5\,C_J$



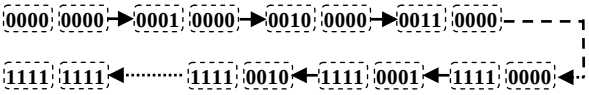
(b) When the switch is ON, each inverter sees a load ≈ C

Figure 4. Concept of operation of the new capacitive load cell.

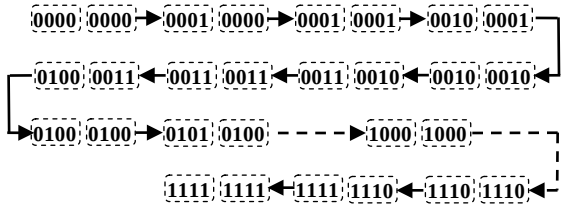
3.4 DRO Control Schemes

Since each DDS has its own control word, there are many ways to control the DRO. All DDSs' words can't be treated as one big word because that will result in many redundant codes (producing equal frequencies) which in turn will cause non-monotonic RDO characteristics. As such, there are two main ways to properly control the DRO to ensure non-redundant codes; one way is to control the DDSs in a binary round-robin fashion (one DDs at a time) and the other is to control all the DDSs' loads together in a thermometer coding fashion. In the first method, starting with the

first DDS, its control word is incremented till it reaches its maximum value, then the control word for the 2nd DDS is incremented till it reaches its maximum value, then the control word for the 3rd DDS is incremented and so on as illustrated in Figure 5(a). This is equivalent to dividing the frequency range into a number of sub-ranges equal to the number of DDSs. In the second DRO control method, Figure 5(b), the load capacitances are enabled in a thermometer coding fashion; 1st ***C*** (the smallest capacitance) of the 1st DDS is enabled, then that of the 2nd DDS, then that of the 3rd DDS till the last DDS's ***C*** is enabled. Next the ***2C*** of the 1st DDS is enabled and its ***C*** is disabled, then the ***2C*** of the 2nd DDS is enabled and its ***C*** is disabled, and so on till all the ***2C***s are enabled. Then another round of enabling the ***C***s, followed by a round of enabling the ***4C***s and disabling the ***C*** and ***2C*** of each DDS. This will be followed by another round of enabling the ***C***s, and then the ***2C***s, followed by a round of enabling the ***8C***s and disabling the ***C***, ***2C*** and ***4C*** of each DDS and so on till all loads in all DDSs are enabled (minimum frequency). This type of control achieves better linearity but is more complex to implement. Both methods yield the same number of total distinct codes; for *m* DDS stages and *n*-bits/stage control word, the total number of distinct codes is $\boldsymbol{m*(2^n - 1) + 1}$.



(a) Controlling the DDSs in a binary round-robin fashion.



(b) Controlling the DDSs in a thermometer coding fashion.

Figure 5. The two main methods for controlling the DRO (illustrated for 2 DDSs with 4-bit/stage control words).

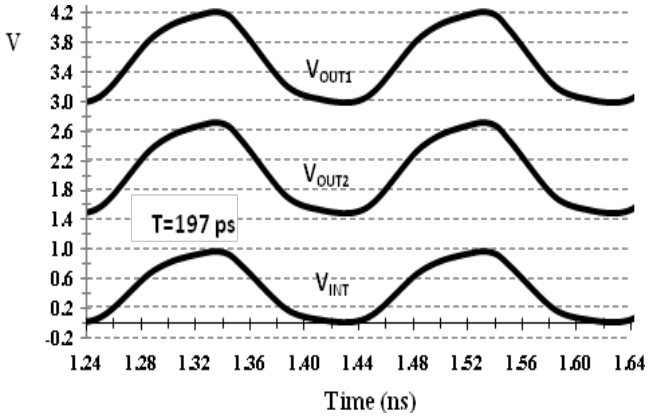
4. SIMULATION RESULTS

4.1 Validation of the Basic Operation

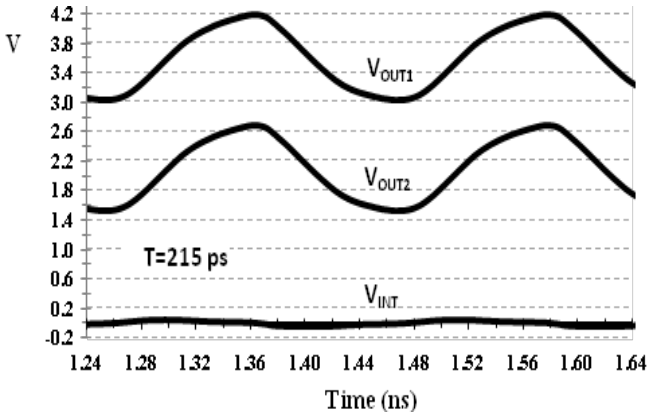
To verify the validity of the new DCO design a 3-stage DRO (two DDSs) and a 3-bit counter were simulated with Spice using a 0.13 m, 1.2V CMOS technology. All NMOS transistor widths were set to a minimum of 1.5*L (L is the minimum channel length) and that of the PMOS transistors to twice that (i.e. 3*L). C was selected to achieve the required frequency criteria as explained in 3.3 ($\mathbf{f_{max} \geq 2f_{min}}$). Fig. 6 shows the voltage waveforms at the outputs of the first stage of both oscillators of the DRO (VOUT1 & VOUT2), and the internal node of the unit capacitance load cell (the smallest capacitance) for two conditions; (a) when all control words are 0s (maximum frequency), and (b) when the 1st control word is 0011 (three steps above minimum period). This figure illustrates how the concept of the new capacitive load cell works. When the switch is OFF, the internal node follows the inverters' outputs very closely, resulting in very small 'effective' capacitive loads for these inverters, thus the attained extremely high frequency. The figure also shows how the two oscillators remain in-phase all the time (with or without the capacitive cells enabled).

4.2 Resolution and Linearity

Figure 7 shows the period and frequency of the DRO's output with the two types of control methods. As this figure shows, the thermometer coding method produces a very linear response. It also shows that with only 4-bits of control word/stage the period step is ~ 6ps, a remarkable performance. Lower frequency ranges, obtained through frequency division, will have larger period steps. Also, when using the binary round-robin control, the period step slightly increases as we move from the 1st DDS to the second DDS due to the effects of increased signal slopes. Hence there will be a set of sub-ranges within the DRO's intrinsic range equal to the number of DDSs within the DRO when using this type of control. The DRO's response is still very acceptable.



(a) Voltage waveforms with the NMOS switch in the capacitance cell off; the internal voltage tracks the inverters' output hence the inverters practically see no capacitance. Waveforms (V_{out1} & V_{out2}) have been shifted up for clarity.



(b) The waveforms with the NMOS Switch ON; the internal voltage is held close to 0 V (i.e. the inverters in the DRO see the full load capacitance.

Figure 6. The voltage waveforms of the 1st stage of the DRO and internal node of the unit capacitance load cell.

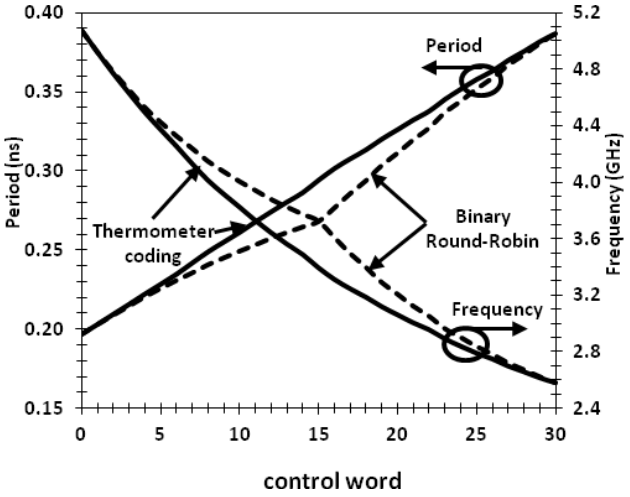


Figure 7. The DRO's Characteristics (period/frequency versus control word) using the two control methods.

It should be noted that, when lower frequency ranges are obtained through successive divisions by 2, non-montonic transitions at the borders between adjacent ranges can occur due to $\mathbf{f}_{max}$ being > $2\mathbf{f}_{min}$. This, however, won't cause any problems since the transition from one range to another is accomplished using the selection MUX while the DRO has the same frequency (i.e. the DCO would go from a frequency **f** to 0.5**f**, 2**f**, 0.25**f**, or 4**f** ...etc.). So any search algorithm used in a feedback loop (such as in a digital PLL) won't be stuck in a non-monotonic region.

4.3 Comparison with Conventional DCO

A 3-stage, 4-control bits/stage conventional DCO based on shunt MOS capacitive loads (such as in Figure 1 (a)) was designed and simulated. Figure 8 shows the period and frequency of this DCO versus the control word. Also reproduced on the same Figure are the results for the proposed DCO. Both DCO's had the same inverters' sizes but the loads were adjusted such that the ratio between $\mathbf{f}_{max}/\mathbf{f}_{min}$ ~ 2. As this figure shows, the new DCO can achieve double the maximum frequency of the conventional DCO due to the new capacitive cell. It also has a much better linearity than the conventional DCO.

4.4 Effects of Devices Mismatch

Since the new DCO is utilizing two oscillators that are suppose to oscillate in perfect synch for the new load cell to operate properly, one concern might arise; what would be the effect of devices mismatch between the two oscillators? The concern here is that the device mismatch would cause phase mismatch between the two oscillators. With such phase mismatch, capacitances in cells that are off which are suppose to 'appear' as open circuited would have an actual value that depends on the mismatch. To check this concern the DRO was simulated with the channel lengths of all MOS transistors in one of oscillator being 10% larger than the minimum. This goes beyond any reasonable process mismatch. Figure 9 shows the output of the DRO at maximum frequency (the most sensitive point to phase mismatch) without the mismatch (Vout1) and with the mismatch (Vout2). As this figure clearly shows, the capacitive cell (and the DRO) still operate exactly as they should. The MNAND gate actually 'mixes' the two oscillators frequency and the resulting frequency is an interpolation between the two. The 10% increase in the channel length of one of the oscillators increased its period by ~7%. The net result, as shown in Figure 9, is that the DRO's period actually increased by ~3.5%.

5. DRO AREA

A custom layout of the DRO was generated using LFoundry's 150 nm technology and is shown in Figure 10 below. M1-M2 capacitances were used for the load cells (at the top part of the layout). The total DRO's area came out to be 44 µm X 9.5 µm (i.e. 418 μm^2), a remarkably small area even at this technology node.

6. CONCLUSIONS

A new fully-digital DCO has been developed. It utilizes a new type of shunt capacitive load for delay control. The new load significantly reduces the effects of parasitic capacitance resulting in a large increase of the maximum achievable frequency. Two methods for controlling the DCO have been devised. Also a simple yet very accurate equation was obtained for selecting the value of the unit capacitance load to ensure proper operation of the DCO. Spice simulations were carried out to verify the operation of the new DCO and evaluate its performance using a 0.13 µm, 1.2V technology. The DCO achieved a maximum frequency of 5.08 GHz at this technology node, an un-precedent performance. With only 4-bit control word/stage, the DCO's resolution at the maximum frequency was 6ps/step. Comparison results show the superior performance of the new DCO compared to conventional shunt capacitive load based DCOs. Also, the custom layout of the DRO shows its remarkable small area.

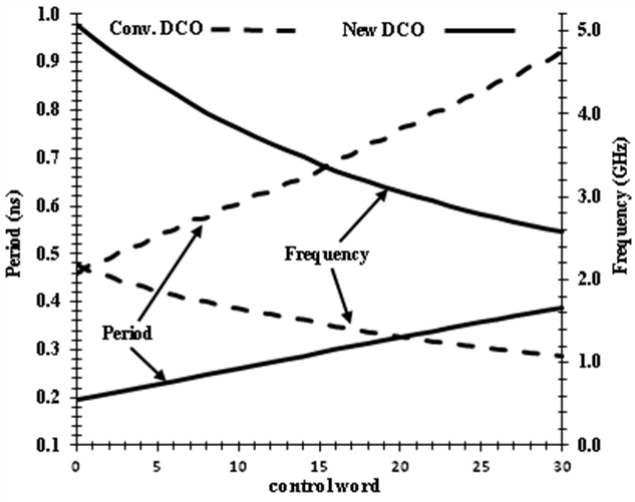


Figure 8. Comparison results for the new DCO and a conventional DCO based on MOS shunt capacitive loads.

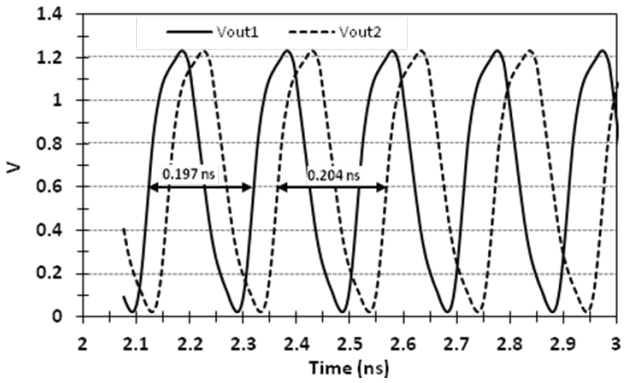


Figure 9. Simulation results of the DRO's output with and without device mismatch.

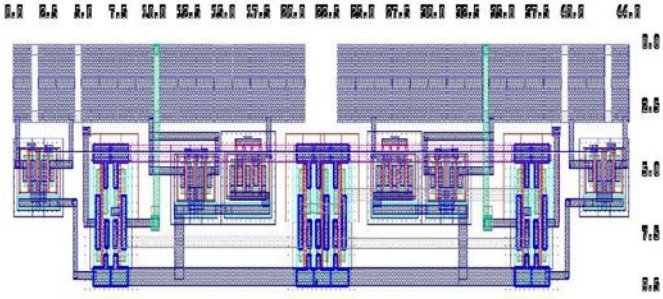


Figure 10. Custom layout of the DRO using LFoundry's 150 nm technology.

7. ACKNOWLEDGMENTS

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