

# A low-cost Method for Test and Speed Characterization of Digital Integrated Circuit Prototypes

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## ABSTRACT

A novel method for the high-speed test and characterization of digital integrated circuit (IC) prototypes has been developed. It utilizes a specially developed, off-chip, test and characterization processor (TACP) in addition to supporting circuitry that is to be included on the prototype IC to facilitate the test and characterization process. The TACP administers the user-defined test, receives and stores the test results. The test procedure and data is downloaded to the TACP memory through a standard interface. The supporting circuitry receives the test data serially from the TACP, apply it to the selected circuit within the IC, collect and reformat the test results and send it to the TACP. It also includes a high-frequency configurable clock generator to be used for performance characterization of the prototyped circuits. This allows the interface between the TACP and the prototype IC to be fixed with any circuits being prototyped and tested. This unique hybrid solution, enables testing an IC at full speed with minimal cost compared to the current method of using high-speed test equipments. To show the validity of the proposed method, a complete prototype has been realized using FPGAs. A complete layout of the on-chip support circuitry using Lfoundry's 150 nm technology shows that the total area required to test 4 circuit prototypes is  $\sim 0.01 \text{ mm}^2$ .

**Keywords:** Circuit Intellectual Property, Integrated Circuits, Characterization and Testing.

## 1. INTRODUCTION

Many university researchers and chip designers in small companies are faced with a difficult problem when it comes to developing new circuit intellectual products (IPs); the cost of prototyping. In order to verify their IP(s) they need to fabricate a prototype, test it and characterize its performance. With the current speeds of up to few Giga Hertz, these circuits would require very expensive testers and scopes. The high cost of such testing equipments is prohibitive for most universities. At the same time, trends in electronic design have converged to what is known as an IP-Based design. This is a design methodology based on re-using existing circuit blocks, namely the IP blocks. These blocks are designed and verified (through prototyping and testing) by IP vendors and are then used and re-used by ASIC (application-specific integrated circuits) and SoC (system on chip) designers. Hence, developing a cost-effective method for testing and characterizing prototypes of circuit IPs is highly desirable.

Some on-chip characterization techniques have been proposed before [1-4] but they are either for specific class of circuits (e.g. memories) or can't perform high speed characterization. They also represent specific custom solutions and do not have the flexibility of the standalone testers.

Some low-cost testing platforms were recently proposed [4-7]. The platforms reported in [4, 5] either can't operate at high speed or requires very elaborate and unreliable solutions based on discrete components [4]. Also, some of these techniques are designed to assist automatic test equipments [6, 7], making them a high cost solution. In [8], a method for characterizing integrated circuits is devised. Voltage and clock controllers are integrated on the device-under-test (DUT) chip to characterize speed versus voltage. Test vectors could come from outside or from an on-chip BIST (Built-In-Self-Test) circuit. For high speed characterization, the test controller would be added on-chip in addition to the BIST circuit resulting in huge area overhead. Also, no general way for applying stimuli and capturing results is provided, requiring custom BIST circuit for each prototype.

As the above discussion shows, there is a need for a low-cost method for testing and characterizing digital integrated circuits containing prototypes of (possibly several) independent circuit IPs. In this work, a novel low-cost test and characterization method has been developed. It allows functional testing and speed characterization of any number of IPs on the same chip. The user can specify his/her functional test procedure and data, capture the results, and specify the clock frequency. It can support any number of input/output ports per IP under test (IUT) with arbitrary port widths (number of bits).

In section 2 an overview of the proposed method is presented followed by a detailed description of the support circuitry in section 3. Section 4 provides a description of the stand-alone test processor. The complete prototype of the proposed method that has been designed and implemented on FPGAs is presented in section 6.

## 2. OVERVIEW OF THE NEW METHOD

Figure 1 below shows the general architecture for a test and characterization platform employing the new method. The TACP is used to apply the user-specified test procedure and data, receives the results and communicate with the user's PC. On-Chip test support circuitry (TSC) facilitates IUT selection, formatting of input and output test data, and configuring the high-frequency clock generator. This new hybrid approach is

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unlike previous techniques which either uses a test circuit that is entirely on the device under test's (DUT) chip or entirely off the DUT's chip. It also differs from the approach in [8] in that it provides a general way for applying stimuli and capturing results with fixed interfaces. Hence the same test and characterization platform can be used to test and characterize any circuit. The TACP can be implemented on an ASIC or a Field-Programmable Gate Array (FPGA) and is interfaced to a PC for receiving test instructions and data and sending the test results.

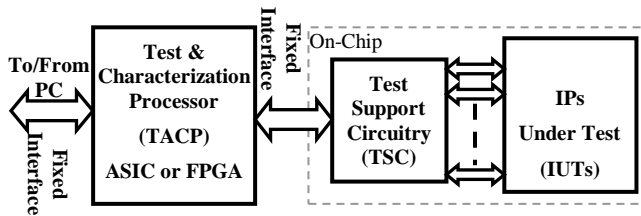


Figure 1. Overview of the proposed Test & Characterization Method.

### 3. The Test Support Circuitry (TSC)

The proposed platform supports testing and characterization of unlimited number of IPs on the prototype chip. Each IP could also have several input/output ports for different purposes (functional I/Os and scan I/Os). To facilitate the testing and characterization of any number of IPs, all signals to/from the TSC from/to the TACP are serialized. Figure 2 shows a block diagram of the TSC. Specific test input/output ports are selected through a selection mask. Test data, strobe signals and test clock are then applied/read to/from these ports. The different blocks in the TSC are described in details below. With the exception of the clock generator, all blocks are parameterized modules that can be synthesized with any user-defined parameters.

#### 3.1 Port Selection Block

The Port selection block, Figure3, is responsible for selecting a specific test application/test result port (TAP/TRP) to deliver the stobes, test clock and input test data to or receive test results from. To make this block general (i.e. parameterized) yet with a fixed interface to the TACP, it is made up by cascading a basic cell as shown in Figure 3. The selection mask is a bit stream with 1s in the positions corresponding to the ports to be selected and 0s otherwise. It is loaded serially using the *Strobe\_in\_PMask* strobe signal and the TACP clock (TCLK\_in). The TACP instructions support variable length selection mask. The selection mask can also be read out for testing.

#### 3.2 Test Application/Results Ports

TAPs/TRPs, Figure4, are used for applying and capturing primary inputs/outputs of an IUT. They are similar to boundary scan ports and are made of shift registers for scanning in/out the test data/results and parallel-load registers for applying/capturing the test data/results. Each TAP (or TRP) is made of a cascaded number of identical cells equal to the port's data width. The shift registers use the TCLK\_in and the application/capture registers use the selected *apply and capture* clock *CLK\_Out*. *CLK\_Out* is produced by a special circuit in the configurable clock generator (CCG). The user can select between the TACP clock (TCLK\_in) or the high frequency clock produced by the on-chip clock

generator (HFCLK). Then, in response to an *apply and capture* strobe from the TACP, the CCG would generate two pulses of the selected clock on the *CLK\_Out*. *CLK\_Out* is also used for the IUT's internal registers. Special TAP/TRP scan ports were also developed for scan chain inputs/outputs of IUTs (used in pairs). These require the internal Flip Flops of the IUT to be scanable. The *TCLK\_in*, *Scan\_En* and *CLK\_Out* signals are made available for the internal scan FFs of the IUT. The TACP instructions support shifting test data in and test results out separately or simultaneously.

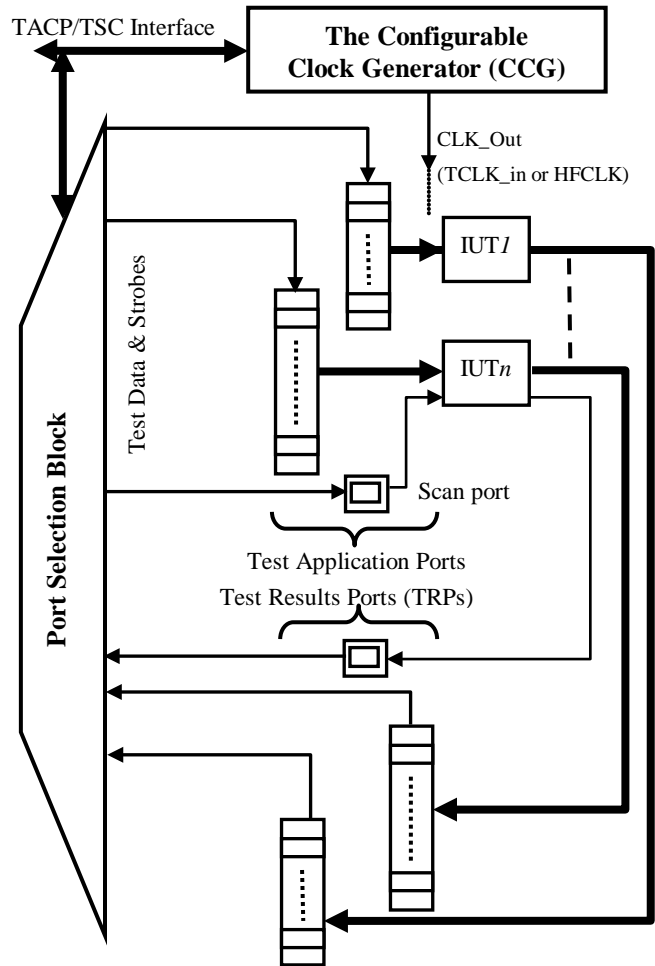


Figure 2. A block diagram of the test support circuitry (TSC) on the prototyping chip.

#### 3.3 The Configurable Clock Generator

The regular test clock *TCLK\_in* coming from the TACP is kept at a moderate frequency (50~100 MHz) to avoid the need for special high-frequency transceivers or signal traces thus keeping the interface design simple and inexpensive. These frequencies are adequate for scanning in/out the test data/results and performing functional characterization of the IUTs. However, for speed characterization, an on-chip programmable high frequency clock source is required. The CCG, Fig.5, provides such a clock. It contains a frequency measuring circuit (FMC), a digitally-controlled oscillator (DCO), a clock frequency control register, and a clock selection and application circuit. The DCO generate

the high frequency clock (*HFCLK*). The frequency of this clock is controlled by the control register. The TACP has instructions to measure the frequency of *HFCLK* and to load control words into the frequency control register, allowing the user to read and control the on-chip high-speed clock through software.

The FMC is shown in Fig.6. The TACP initiates a frequency measurement by asserting the request *HFCLK\_Meas\_R*. The FSM clears the high-frequency counter and enable counting till the TACP de-asserts *HFCLK\_Meas\_R*. The period between the assertion and de-assertion of *HFCLK\_Meas\_R* is the measurement period. The count value is then loaded into the frequency register and *HFCLK\_Meas\_A* (acknowledgement) is asserted so the TACP can readout the value using the strobe. The En (enable) signal is synchronized as it crosses from the *TCLK\_in* to the *HFCLK* clock domain. The *HFCLK* frequency is calculated (in the user interface software) as:

$$F_{HFCLK} = \text{Frequency Register Value} / \text{Measurement Period}$$

The clock selection and application circuit, Figure 7(a), is used by the TACP to select the desired test clock and apply exactly two pulses of that clock to the selected TAP/TRP ports in response to a two-cycle strobe on the *AaC* (Apply and Capture) input. It is made of multiplexor, a series of synchronizers and two FFs to synchronize the *AaC* signal and produce a two clock-pulses wide signal. This signal is then used by a special clock gating circuit to produce *exactly* two pulses of the selected clock as shown in the gate-level simulation results in Figure 7(b).

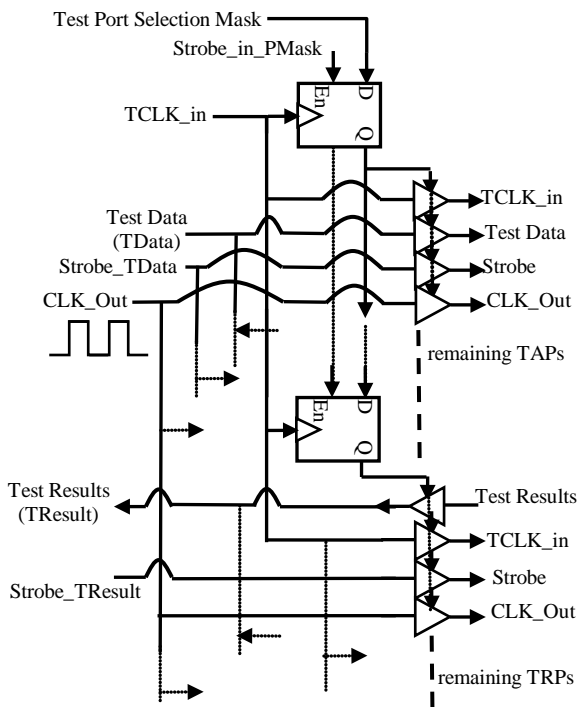
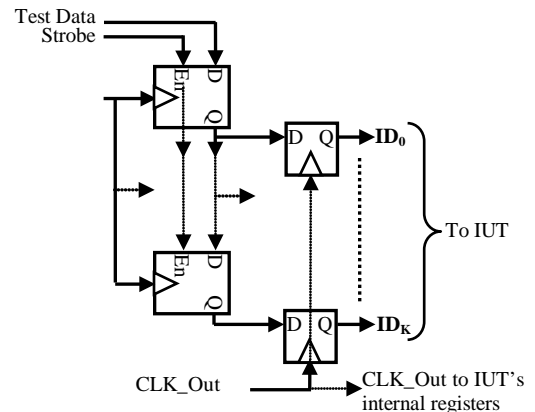


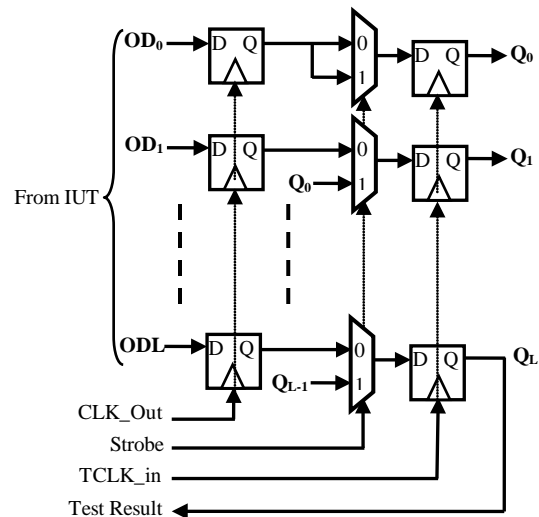
Figure 3. The Port Selection Circuitry.

A simple DCO circuit, Fig. 8, was used for generating the basic high frequency range of *HFCLK*. It is based on switched-capacitance shunt loads. Low frequency ranges were obtained by dividing by powers of 2 with a binary counter (not shown in the

figure). To get continuous DCO's frequency range with the division by powers of 2, the basic oscillator had to be designed such that it has a 2x frequency range (i.e.  $f_{max} \geq 2f_{min}$ ). Using a 0.13 $\mu$ m technology, with only 2 delay stages (plus the NAND) and 4-bit of control per delay stage, a frequency range of 1.08 – 2.19 GHz with an average resolution of ~8 ps and excellent linearity was obtained as shown in Fig. 9. It should be noted that with 4-bits per stage we only get 31 different frequencies after eliminating redundant codes (that yield the same frequency).



(a) A *K*-bits wide Test Application Port (TAP)



(b) An *L*-bits wide Test Results Port (TRP)

Figure 4. Test Application/Result Ports.

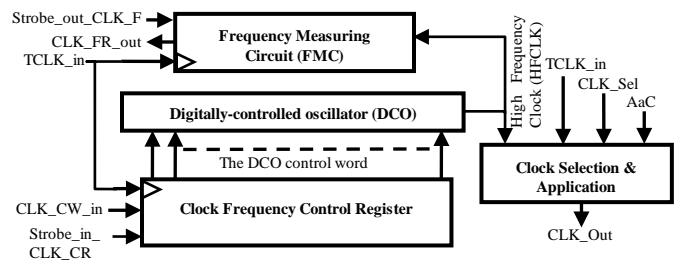


Figure 5. The Configurable Clock Generator (CCG).

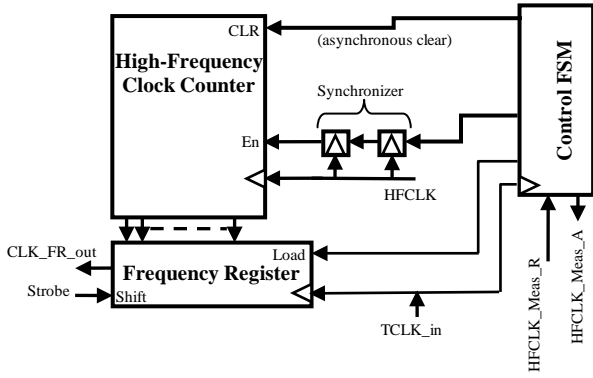
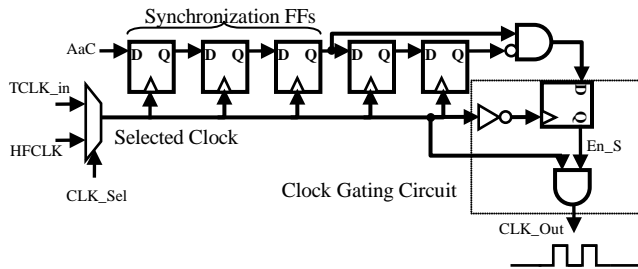
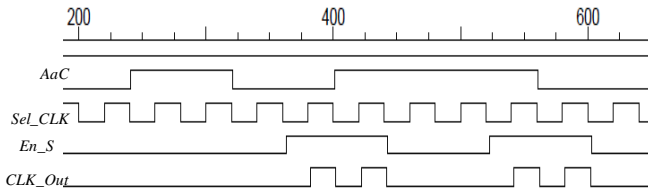


Figure 6. The Frequency Measurement Circuit (FMC).



(a) The Clock selection and Application circuit.



(b) Gate-Level simulations of the above circuit.

Figure 7. The Clock Selection and Application Circuit.

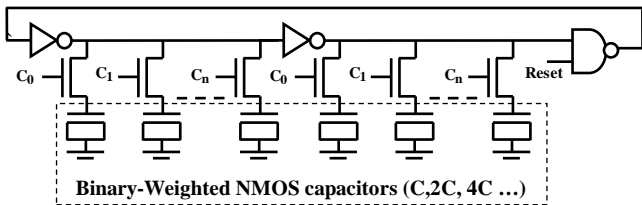


Figure 8. The DCO Circuit.

#### 4. THE TACP

Due to the fact that most of the required test and characterization instructions are multi-cycle instructions with a variable data-dependent number of cycles the TACP was implemented using micro-coding. The data path is made of shift registers for shifting in/out test data and counters to count the number of shifts. The control unit decodes the test instructions, loads the counters with the length of bit streams and controls the shift registers. Table 1 lists some of the key TACP's instructions and their description. Additional instructions include setting up counters, jump, conditional jump, subroutine call and return.

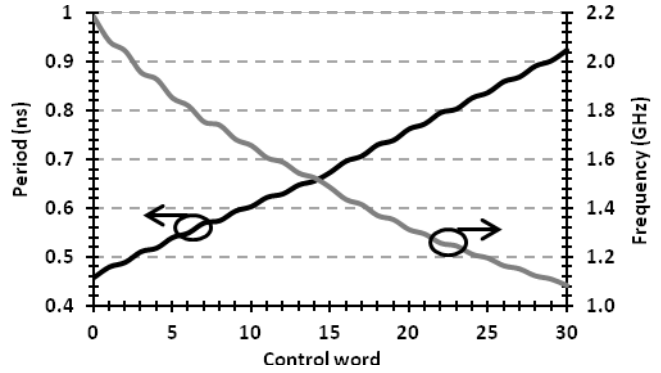


Figure 9. Spice simulation results showing the frequency and period of the DCO's output as a function of the control word.

To simplify memory management, the TACP's memory is partitioned into three partitions that are under the direct control of the host computer; one for instructions, another for test data and another for test results. Also, a simple protocol and the circuit that implement it were developed for host-TACP communications. Special interactive configuration commands allow the host to read the on-chip HFCLK frequency, increase it or decrease it. Other commands also allow the host to set the TACP frequency (TCLK) and read out its internal registers for debugging purposes. The simple TACP architecture allows the addition of more instructions if needed in future revisions.

#### 5. EXPERIMENTAL RESULTS

A complete prototype of the proposed test and characterization method was implemented using FPGAs as illustrated in Figures 10 and 11. The TACP, running at 50 MHz, was implemented on an FPGA and successfully used to test several IPs on another FPGA board. The DCO in the configurable clock generator was replaced by a group of DCMs (digital clock managers) and clock multiplexors to produce the high speed test clock to the IUTs. The communication unit is made of two parts; a communication media unit (a phy+MAC) and a protocol execution unit. This two-layered design allows media-independent communication under different media types (i.e. serial, USB or Ethernet).

A user-interface software for downloading test programs and data to the TACP and uploading test results and register contents was also developed. It also allows single-step execution and debugging of the TACP. Figure 12 shows the user-interface tool with an example test program that apply a set of test vector to one of the IUTs in a loop, compare the results with the expected value and if they match increments the testing clock frequency till the test fails. As the figure shows, for the selected IUT, the maximum frequency reached was 129.98 MHz as measured by the frequency measuring circuit (FMC) on the IUT's FPGA. The actual frequency generated by the DCM was 130 MHz. Hence the accuracy of the FMC is 99.985%.

A complete test support circuit that allows the testing of 4 IUTs (two 8-bit adders and two sequential circuits with 5-FF each) was synthesized from Verilog description to GDSII layout as shown in Figure 13. With a total of two 16-bit input ports (TAPs), two input/output scan ports and two 17-bit output ports (TRPs) the area is  $\sim 10,000 \mu\text{m}^2$  ( $\sim 0.01\text{mm}^2$ ). The size of the

complete circuit with the 4 IUTs was  $\sim 75,000 \mu\text{m}^2$  i.e. the TSC took less than 15% of the total area.

## 6. CONCLUSIONS

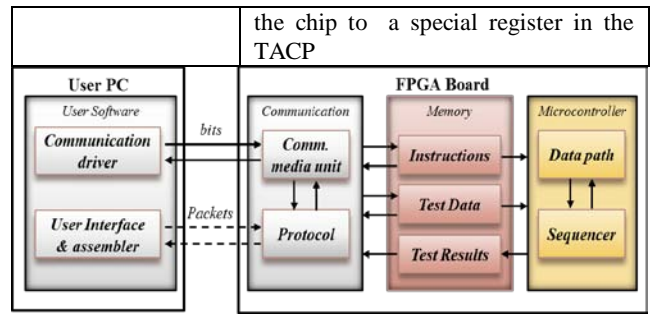
A new low-cost platform for the test and characterization of circuit IP prototypes has been developed. The new platform would allow IP developers to test the functionality and speed of their IP prototypes. It supports unlimited number of IPs per IC and unlimited number of ports/port widths per IP with constant interfaces. Hence the platform itself does not need any configuration or design change to test any circuit. The new concept has been successfully verified using a complete FPGA prototype and a specially-developed user-interface software. Also a complete layout of the support circuitry that is included on the chip with the IUTs was generated using a150 nm technology. It shows that the area overhead of this circuitry is insignificant.

## ACKNOWLEDGMENT

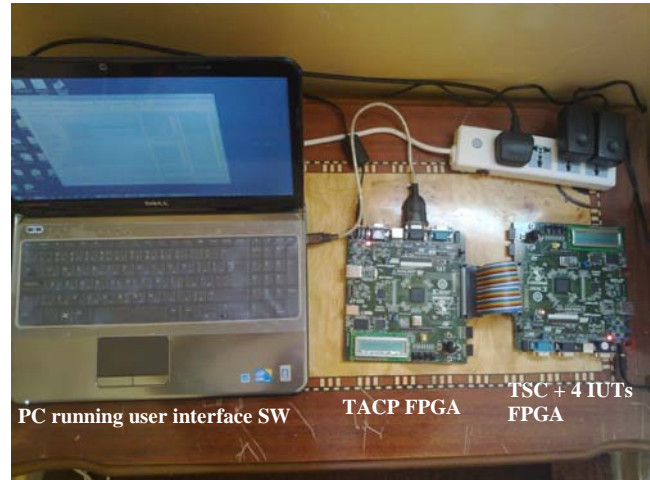
This work has been supported by King Abdel-Aziz City for Science and Technology through development grant 4-14/2010. KFUPM's facilities support is highly appreciated by the authors.

**Table 1. Key instructions of the TACP and their description.**

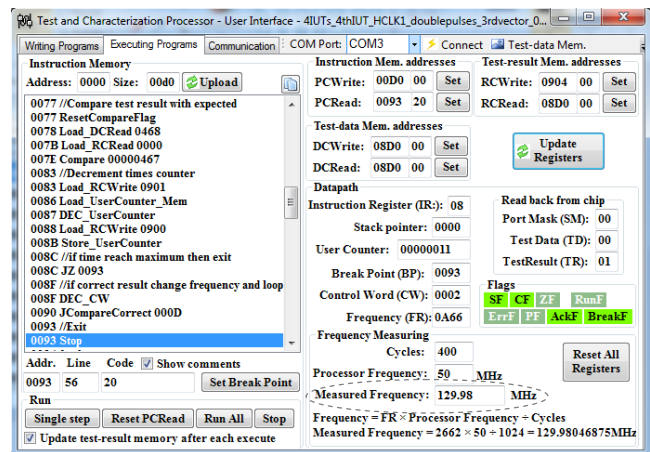
Instruction	Brief Description
<i>SendSelMask</i>	Sends a bit stream to the port selection mask register on the chip (along with the required strobe) to enable the selected IUT port(s).
SendTestData	Sends test data from the TACP test data memory (from the address specified by the DCRead register) to the chip with the required strobe.
Load_DCRead	Sets a value to the test data address register DCRead
ReadResult	Reads results back from the chip and stores them in the TACP's test result memory in the address specified by RCWrite register.
Load_RCWrite	Sets a value to the test result writing address register
Load_RCRead	Sets a value to the test result reading address register RCWrite
ApplyAndCapture	Sends an <i>apply and capture</i> (AaC) signal to the chip causing the CCG to produce two pulses of the selected clock which are applied to the selected IUT.
Compare	Compares (XOR) between two memory locations and store the comparison result in another location
SetFreqContWord	Sets a value in the frequency control word register in the TACP
SendFreqCoWord	Shifts out the frequency control word to the chip's frequency control register
MeasureFrequency	Starts the frequency measuring algorithm in the chip
ReadFreqReg	Shifts out the frequency register from



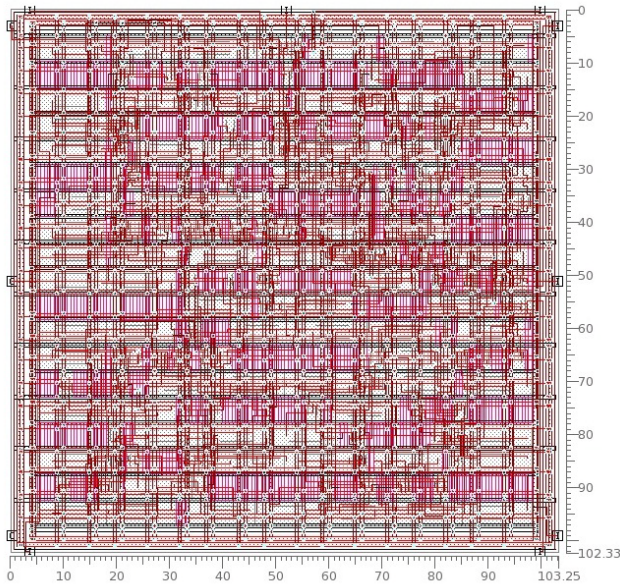
**Figure 10. Block diagram of the prototype platform.**



**Figure 11. The prototype platform implemented with two FPGA boards.**



**Figure 12. The user interface software showing a test program that finds the maximum frequency of operation of an IUT.**



**Figure 13. The layout of test support circuitry that test 4 IUTs using LFoundry's 150 nm technology.**

## REFERENCES

- [1] Galke, C., Pflanz, M. and Vierhaus, H. "A Test Processor Concept for Systems-on-a-Chip", Proceedings of the 2002 IEEE International Conference on Computer Design: VLSI in Computers and Processors (ICCD'02), pp. 210-212.
- [2] Bahl, S. and Singh, B., "On-Chip and At-Speed Tester for Testing and Characterization of Different Types of Memories," US Patent # 7,353,442 B2, April 1st, 2008.
- [3] Franco, P., Farwell, Stokes, R. and McCluskey, E. "An Experimental Chip to Evaluate Test Techniques: Chip and Experiment Design", Proceedings of the IEEE International Test Conference on Driving Down the Cost of Test, pp. 653 – 662, 1995.
- [4] Maggioni, S., Veggetti, A., Bogliolo, A. and Croce, L. "Random Sampling for On-Chip Characterization of Standard-Cell Propagation Delay", Proc. of the 4th International Symposium on Quality Electronic Design, pp. 41-45, 2003.
- [5] L. Mosterdini, et al, "FPGA-based low-cost automatic test equipment for digital integrated circuits", Proc. IEEE workshop IDAACS, 2009, pp. 32-37.
- [6] L. Ciganda, et al, "FPGA-based Low-cost Automatic Test Equipment for Digital Integrated Circuits", Proc. 12th IEEE Symp. DDECS, 2009, pp. 258-263.
- [7] Justin S. Davis, "AN FPGA-BASED DIGITAL LOGIC CORE FOR ATE SUPPORT AND EMBEDDED TEST APPLICATIONS," PhD. Dissertation, Georgia Institute of Technology, 2003.
- [8] K. M. Van Kaam, "Integrated Circuit (IC) With On-Board Characterization Unit", US Patent 7,475,312 B2, Jan. 6, 2009.