A Universal 3.3V 1 GHz BiCMOS Transceiver (Driver/Receiver)

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ABSTRACT: A universal BiCMOS low-voltage-swing transceiver (driver/receiver) with low on-chip power consumption is reported. Operating at 3.3V, it can drive/receive low-voltage-swing signals with termination voltages ranging from 5V down to 2V without using any external reference voltages.

I. Introduction

Existing low-voltage-swing transceiver circuits are incompatible with each other due to their different termination/reference voltage requirements. Hence, they require special interface parts between them and several voltage references, thus increasing the overall system cost. Also, low on-chip power is a major concern for such transceivers because of the increase in the required number of I/O's in Telecommunication IC's.

BiCMOS technology has proven to be an excellent workhorse for telecommunication applications [1]. We have fabricated and tested a novel low-voltage-swing transceiver (Receiver/Driver) with low on-chip power, using a 0.8 μm BiCMOS technology. Using a supply voltage of 3.3V, the new transceiver can drive/receive low-voltage-swing signals with termination voltages ranging from 5V down to 2V without using any external reference. The on-chip power consumption is much lower than that of CML/ECL transceivers with comparable speeds. The circuit description and performance of the receiver and driver are described in this paper.

II. The Universal Receiver

The novel receiver circuit consists of three sub-circuits; the universal input buffer (UIB) of Fig. 1, the Vref generator (Fig. 2(a)), and the load control circuits (Fig. 2(b)). The UIB consists of an emitter-coupled BJT pair followed by a source follower stage. The four PMOS devices M1-4 serve as loads for the emitter-coupled BJT's. The Vref generator keeps the value of the reference voltage Vref at about 0.45V below the termination voltage VT (assuming a signal voltage swing of 0.8 to 1.0 V). The PMOS load devices are controlled by the two biasing voltages V1 and V2 which are generated by the load control circuit. The load control circuit biases the PMOS load devices such that the input BJT pair never saturates. M5 and M6 ensure that the N-wells of all the PMOS devices M1-6 are connected to the higher voltage between VT and VDD. A source-follower stage was used instead of an emitter-follower to avoid saturation problems when VT is larger than VDD.

The Vref generator produces a stable reference voltage, Vref, over a wide range of temperature and for VT's ranging from 1.5V to 5V. Mn1 in Fig. 2(a) is only on for VT's less than 2.5V while Mp1 and the diode are used for temperature compensation. Mp1 is biased in such a way that its drain current will increase linearly with VT. This behavior will keep the current through Q1 constant and hence Vref will always remain constant with respect to VT (i.e. Vref = VT - 0.45 V). Figure 3 shows the stability of the measured output of the Vref generator over a wide range of temperatures for several termination voltages. The maximum change in Vref over the whole temperature range for all values of termination voltages was 51 mV, 5% of the voltage swing.

The load control circuit is a simple source-coupled NMOS pair with cross-coupled PMOS loads. When VT is less than VDD, V1 will be "High" and close to VDD (*VDD - V1* would be less than the PMOS threshold voltage V_{tp}), and V2 will be "Low". When VT is greater than VDD, V2 will be "High" and close to VT ($VT - V2 < V_{tp}$), and V1 will be "Low". So for VT < VDD, M1 and M4 in the UIB are off and M2 and M3 are on. Also M5 will be on and the N-wells will be connected to VDD. If VT exceeds VDD, M1 and M4 will be turned on, M1 and M4 will be turned off, and the N-wells will be connected to VT. As VT increases further, V2 keeps increasing such that M2, M3, and M5 remain off. No current will flow between VT and VDD under any circumstances. The load control circuit was found to be very stable over the temperature range. The maximum change in V1 and V2 over the whole temperature range for any value of VT was found to be less than 10 mV.

The outputs of the UIB are shown in Fig. 4 for two values of VT (2V and 5V), an input frequency of 1 GHz, and an ECL gate as a fan out. The value of the tail current of the UIB used was 1 mA, and the total power of the receiver for a 3.3V termination voltage (including that of the biasing circuits) at 1 GHz was 17 mW. An ECL receiver consumes more than 30 mW at the same frequency. Experimental results showed that the new receiver successfully read signals with termination voltages ranging from 1.5V to 5V and frequencies exceeding 1.5 GHz.

III. The Universal Output Driver

Two versions of the universal output driver (UOD) were developed (Fig. 5). The Cx's capacitors (Fig. 5) are used to enhance the speed, and for the design of both drivers double termination (25 Ω load to VT) was assumed. The output current "high" value of both drivers is determined by Vc and Rs. Vc equals the difference between Va and Vb. When I/P is high:

$$Vc = z \cdot V_{BE}$$

Where z is the multiplication factor of the V_{BE} multiplier (Q1 and the two resistors connected to it) in Fig. 5. For the first version of the UOD (UOD1) the following condition is further imposed in the design:

$$1 < z \leq 1 + \frac{V_s}{V_{BE}}$$

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Where V_s is the voltage swing of the input signal. This requirement will set the output current "Low" value to zero (Vc would be V_{BE} when I/P is low). So for this driver to be designed properly, a rough value of V_s should be known in advance. The "High" value of the output current and consequently, the output swing, is independent of the exact value of V_s.

The UOD1 has two shortcomings: 1) The large Q3 is turned on/off solely through the base, hence the base resistance R_B makes the turn on/off slower than the combined base/emitter turn on/off (as in CML/ECL circuits); and 2) The "Low" value of the output current might not be exactly zero as intended in the design (it may reach a few hundreds of μA's) because of resistor tolerance, thus slightly reduce the noise margins by reducing the value of V_{OH}.

To overcome these shortcomings, Q4 was added to the UOD1 to produce the second version of the universal output driver (UOD2), as shown in fig. 5. Q4 (which is much smaller than Q3) has its base connected to a reference voltage Vr. For this version the restriction on the high limit of z is relaxed since the "Low" value of Vc (Vc_{Low}) does not have to be less than V_{BE}. When the input I/P goes low, the tail current is steered away from Q3 to Q4. The "Low" value of the tail current, however, is much smaller than the "High" value because: 1) Vr is set to a value less than the "High" value of Vc, and 2) V_{BE} of Q4 is larger than that of Q3. Hence, the voltage across Rs will be much smaller when I/P is low. When I/P becomes high, the "Low" tail current is steered away from Q4 to Q3 and helps turn it on. The disadvantages of the UOD2 as compared to the UOD1 are the slight increases in power and area.

Figure 6 shows the measured outputs of both drivers at 0.5 GHz and a termination voltage of 5V. The on-chip power requirements at that frequency were 75 mW and 80 mW for the UOD1 and the UOD2, respectively. The power of a CML driver at the same termination voltage is about 125 mW. An ECL or pseudo ECL driver would dissipate an even greater power under the same conditions. For a 2V termination the UOD1 and the UOD2 powers are 25 mW and 29 mW, respectively. Simulations showed the superior speed performance of UOD2 over the VT range. They also showed that for both drivers the maximum frequency of operation decreased as VT decreased due to the increase of the collector capacitance and the saturation effects of Q3. Finally, fig. 7 shows the measured output of the UOD1 at 1 GHz and 5V termination. The swing is still 0.8V (the same as the low-frequency swing) at this high frequency.

IV. Conclusion

A novel BiCMOS transceiver has been developed. Operating with a 3.3V supply, it can receive signals with termination voltages from 1.5V to 5V at frequencies exceeding 1.5 GHz. The driver can operate at frequencies above 1 GHz with termination voltages ranging from 2V to 5V. The on-chip power of both receiver and driver are well below that of CML/ECL transceivers with comparable speeds.support.

References

[1] R. Hadaway, *et al.*,"BiCMOS Technology for Telecommunications," *IEEE BCTM Proc.*, 1993, pp. 159-166.

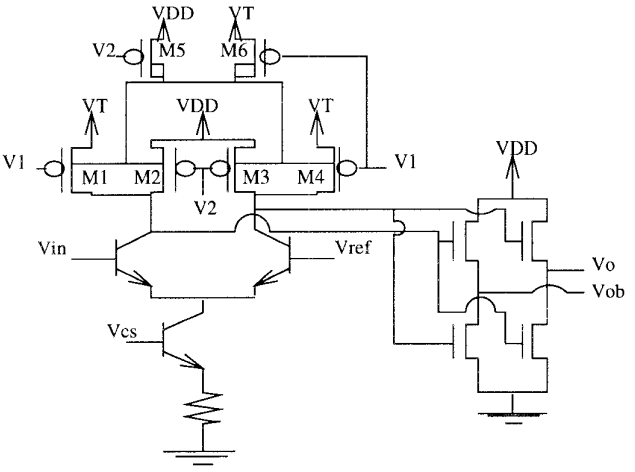
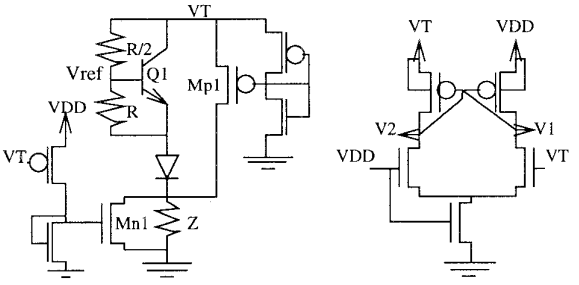


Fig.1. The universal input buffer (UIB).



(a) The Vref generator (b) The load control circuit.

Fig.2. The receiver reference circuits.

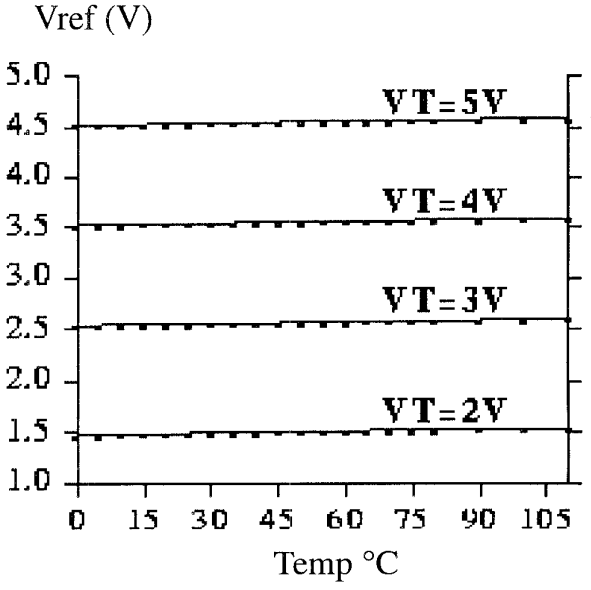


Fig.3. The measured output of the Vref generator vs temperature for several termination voltages.

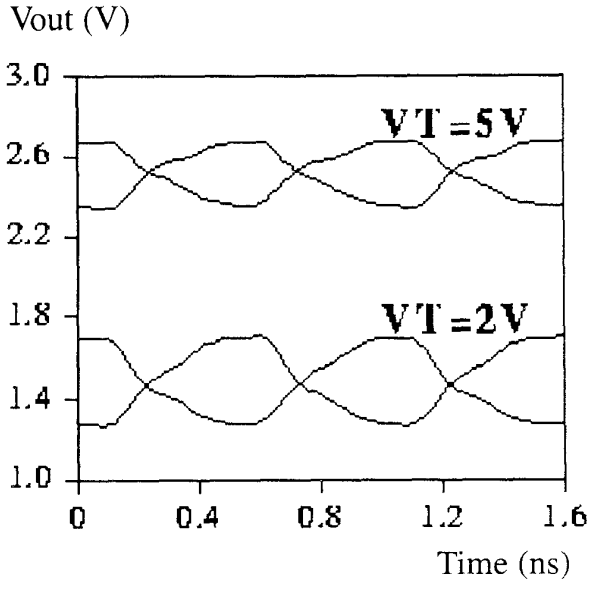


Fig.4. The simulated UIB outputs for two termination voltages at 1 GHz and a fanout of one (ECL gate at the output).

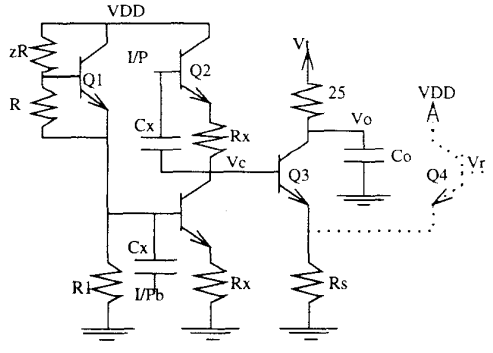


Fig.5. The two UOD versions; The first one is without Q4, and the second one includes Q4 (dashed line).

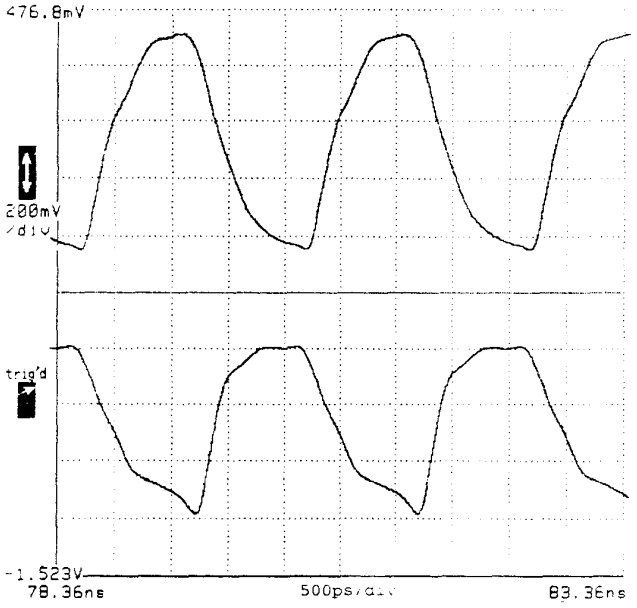


Fig.6. The measured output waveforms of the two novel drivers at 500 MHz and 5V termination. UOD1 output is the lower trace.

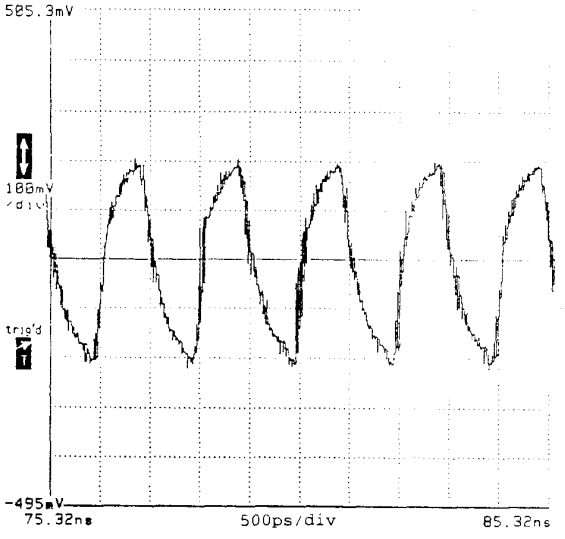


Fig.7. The measured output waveform of the UOD1 at 1 GHz and 5V termination (6db attenuation at the input of the sampling scope).