Principles of VLSI Design COE 360 (3-0-3)
Course Outline

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Office hours shall be announced in the class and posted on the door			

Course Description

MOS Transistor operation and limitations, MOS digital logic circuits (NMOS & CMOS), static & dynamic logic, combinational and sequential circuits, propagation delay, transistor sizing, MOS IC fabrication, layout and design rules, stick diagrams, IC Design and Verification Tools, subsystem design and case studies, and practical considerations.

Prerequisite: EE 203.

Text Book: S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 2nd ed., 1999. Also some handouts on basic semiconductor concepts will be used insha'Alla.

References:
1) N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design*, Addison Wesley, 1993.
2) Ken Martin, *Digital Integrated Circuit Design*, Oxford Press, 2000.
3) Jan Rabaey, *Digital Integrated Circuits; A design Perspective*, Prentice Hall, 1996.

Course Rationale

This course teaches the fundamental issues involved in the design, simulation, verification and manufacturing of digital integrated circuits (ICs).

Course Objectives

Insha'Allah by the end of this course students are expected to be able to:

- Describe the operation of MOS transistors using adequate models while realizing the limitations of these models
- Analyze and evaluate the performance of different digital circuits
- Describe the basic CMOS manufacturing process
- Synthesize an efficient mask design (layout, or blue print) of a CMOS IC starting from a functional description. This would involves such skills as design segmentation, logic design, circuit design, simulation and post layout evaluation
- Work better within a group

Learning Methodology

The course objective shall be met insha'Allah though lectures, hands-on in-class exercises, assignments and the use of software for simulations and design of MOS chips.

Course Topics:

1. ***Review Material:*** **(2 weeks)**
   - Types of solids (in terms of conductivity)
   - Review of basic semiconductor concepts (types, doping, Electrons and holes, calculating n and p, Mobility, conductivity, current transport)
   - PN junction (structure, built-in potential, I-V characteristics, and capacitance).
2. ***The MOS Transistor:*** **(3 weeks)**
   - Structure (NMOS, PMOS, Enhancement vs. depletion)
   - Operation (regions and basic equations)

- Limitations and scaling effects (Body effect, Latchup, Velocity saturation, Drain-Induced Barrier lowering (DIBL), Hot Electrons injection, and leakage)
- SPICE models and capacitances

3. ***Digital MOS Circuits:*** **(5 weeks)**
   - Review of basic Specifications of Digital Integrated Circuits (Noise Margins, Fanin, Fanout and Power dissipation).
   - Static MOS inverters (NMOS and CMOS inverters, delay models, transistor sizing, and power dissipation)
   - Static NMOS & CMOS logic, pass-transistor logic (PTL), transmission gates, differential Cascode Static Logic (DCSL), Latches and registers
   - Dynamic MOS Logic (Domino Logic, Dynamic DCL, Charge Sharing and True Single-Phase Clock (TSPC)

4. ***CMOS Processing Technology:*** **(3 weeks)**
   - Photolithography and masking
   - CMOS fabrication process (epitaxy, oxidation, diffusion, implantation, metalization and passivation)
   - CMOS design rules and layout (transistors, interconnects, Sheet resistance, integrated resistors and capacitors, and Distributed RC Effect)

5. ***CMOS IC Design & Case Studies***: **(2 weeks)**
   - Subsystem Design (Floor planning, Adders, shifters, ALUs, decoders, counters, Memories, I/Os and case studies)
   - ***VLSI Design Styles*** (Custom vs. Semicustom techniques, Standard Cells, Gate Arrays, FPGAs and testing)

Course Project: The course project is a very important tool to develop and apply different concepts learned in the course. It should also enhance the student's presentation skills and ability to work within a group. Groups of 1 to 3 students shall be formed and each will be assigned a different project. Each group shall divide the work among them and present their progress throughout the project phases.

Grading Policy

Grading is meant only as a way of assessing the student's achievements in the course. Students should not feel too much pressured by this process. The adopted grading policy allows and indeed rewards improvements. A student failing to achieve a good grade in the first exam should not feel that he has no chance. The whole purpose of the adopted grading policy is to give the student a second and even a third chance if he needs it to achieve the best result he wants.

Assignments & Quizzes	10 points	
Project	20 points	
Progress exam I	5 points	(tentative date 8/10/2006)
Midterm Exam	20 points	(tentative date 26/11/2006)
Progress exam II	5 points	(tentative date 24/12/2006)
Final Exam	40 points	
Total	100 points	

Attendance Policy

- Attendance will be taken regularly. Students who are more than 10 minutes late are considered absent,
- There will be a 0.5% grade deduction for every unexcused absence,
- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.