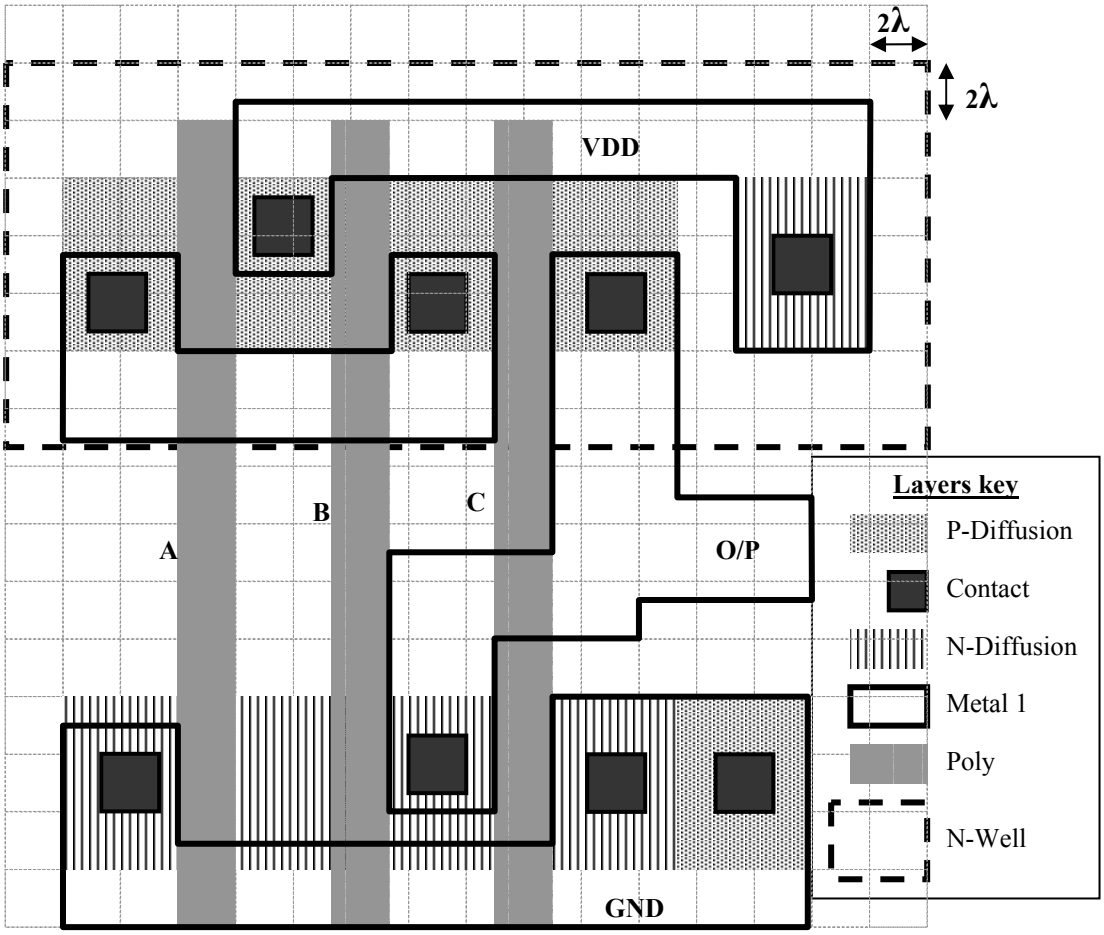
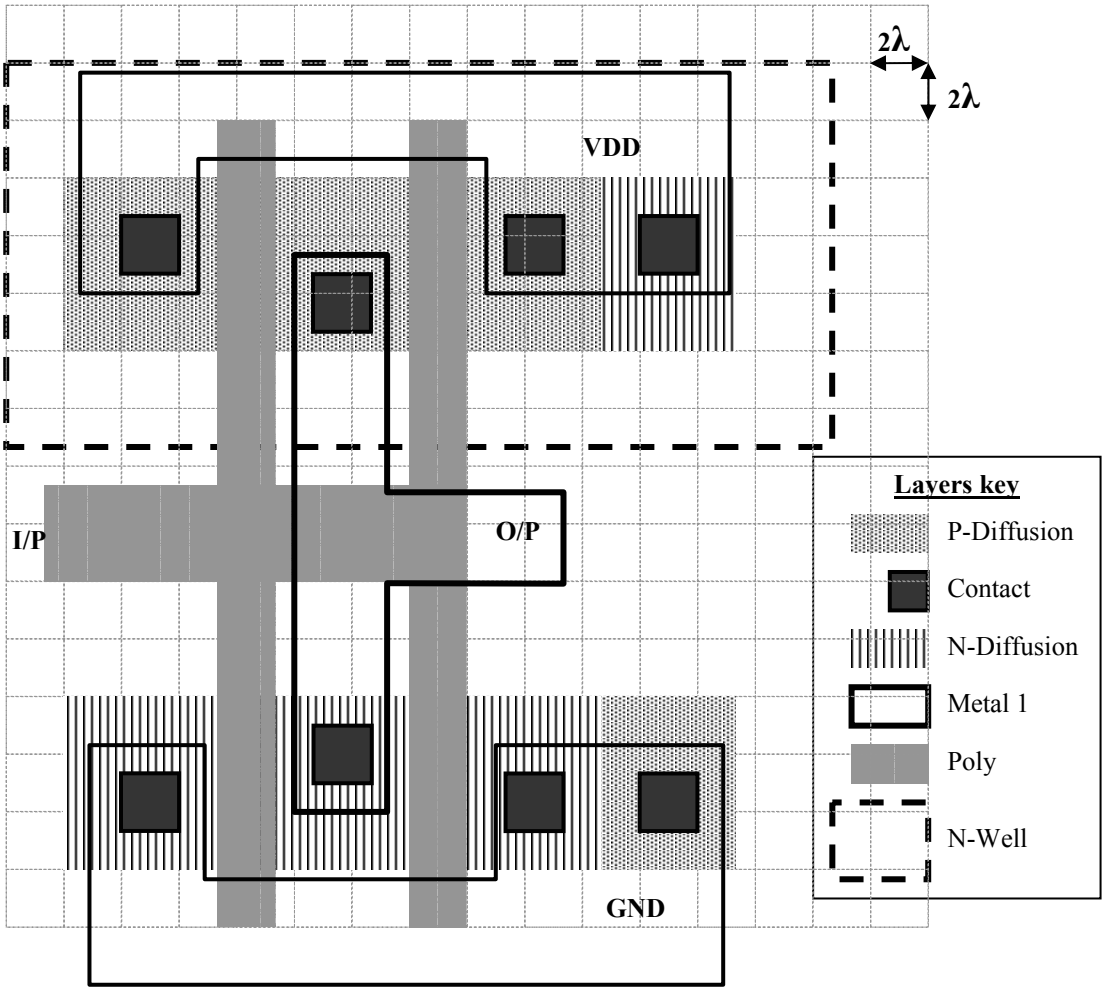
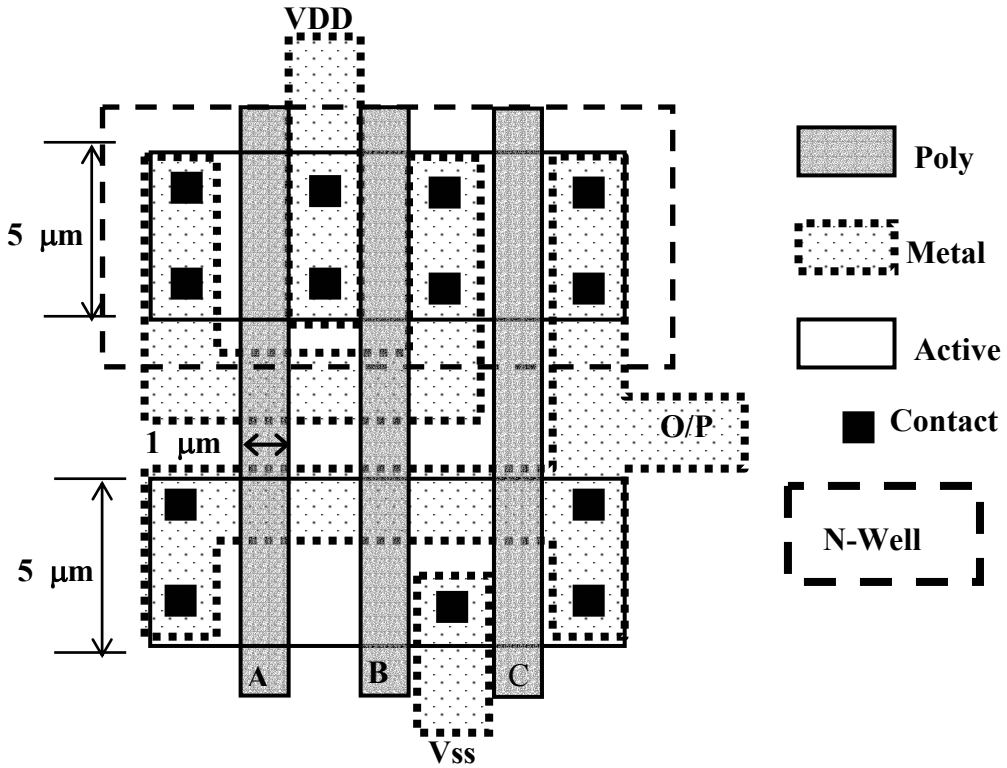
The following layouts of CMOS circuits:

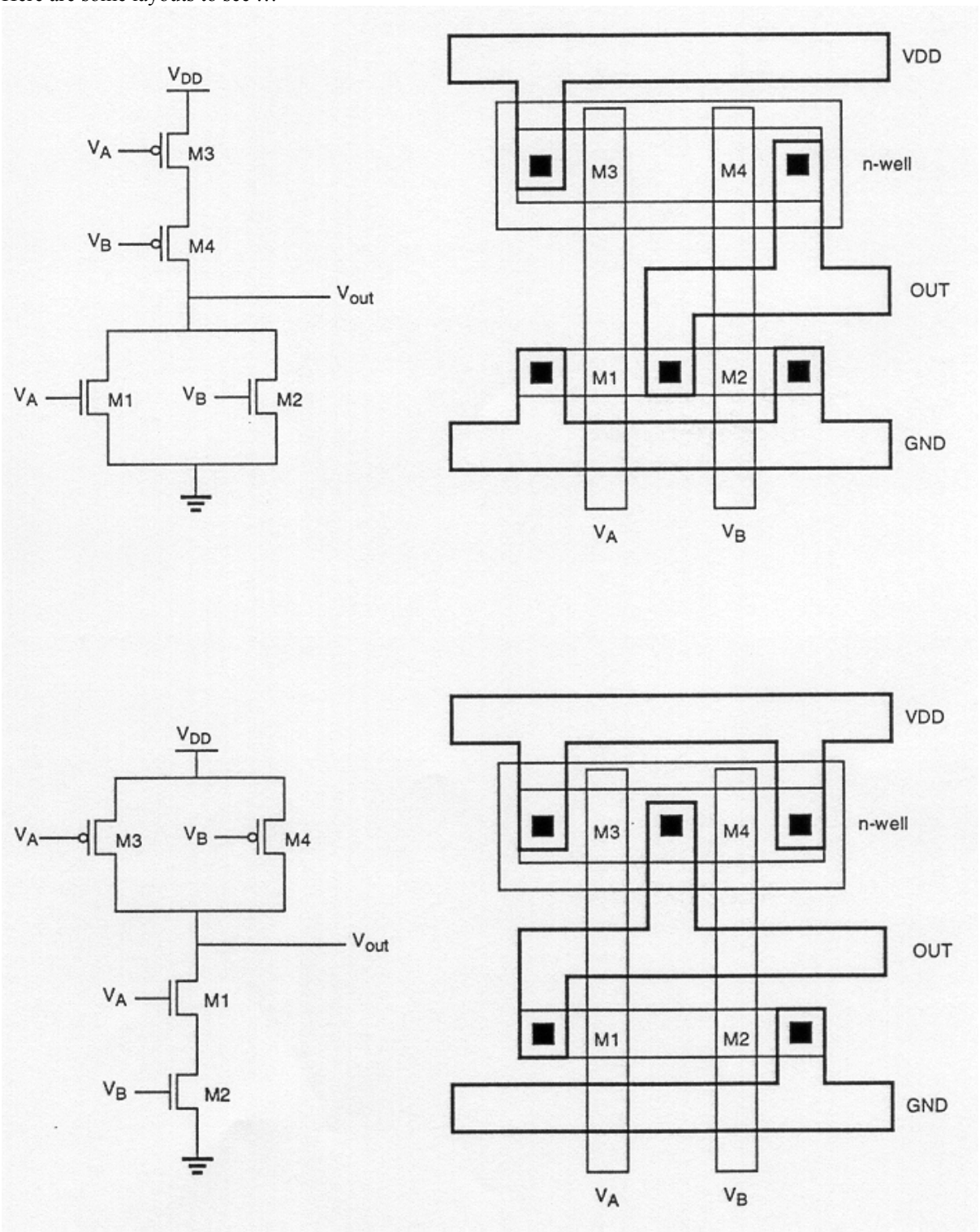
1. **Obtain the circuit schematic with transistors sizes (W/L) <u>in microns</u> (assume a 1µ m technology)**
2. **What is the function of this circuit?**

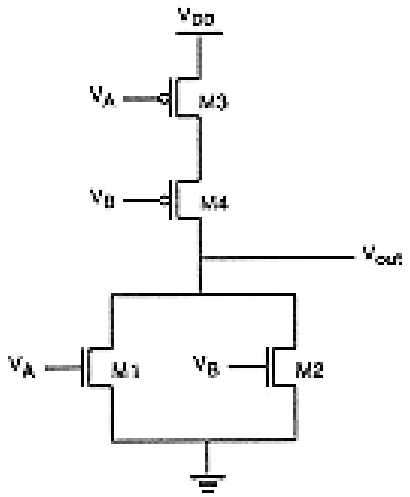


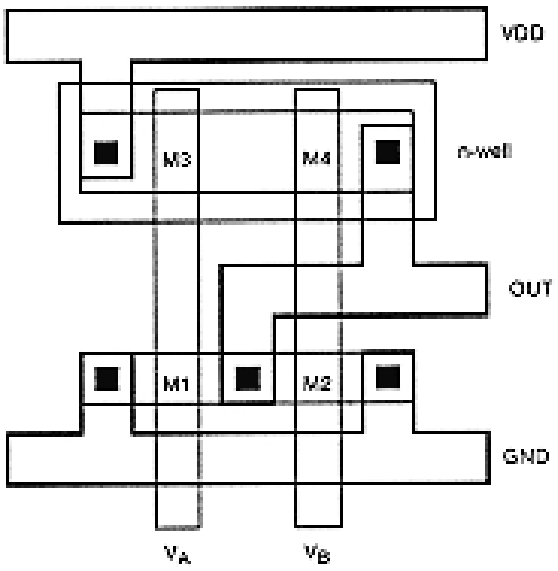

2λ
2λ
VDD
I/P
O/P
GND
Layers key
P-Diffusion
Contact
N-Diffusion
Metal 1
Poly
N-Well

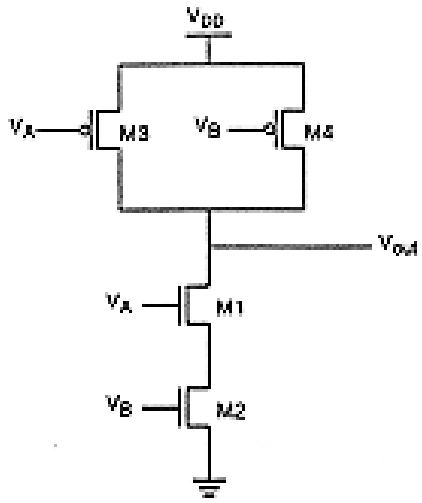

VDD
5 μm
1 μm
5 μm
O/P
A
B
C
Vss
Poly
Metal
Active
Contact
N-Well

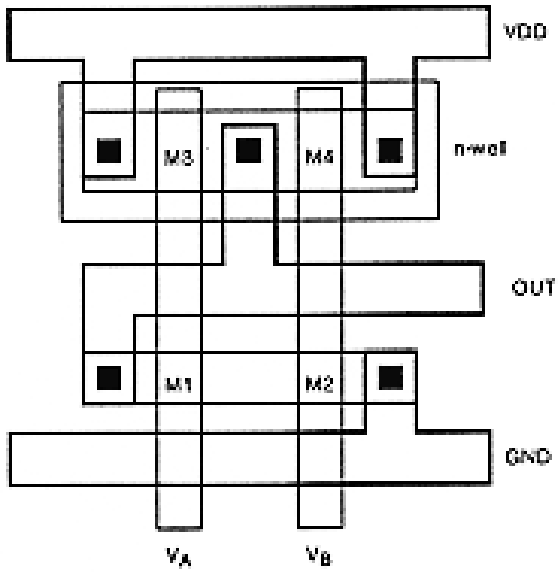
Here are some layouts to see …

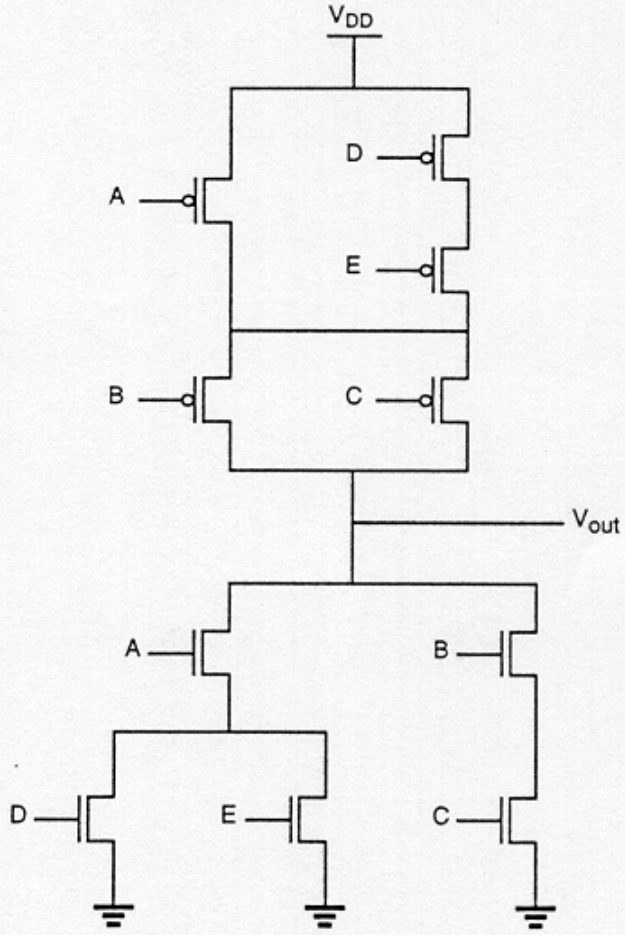


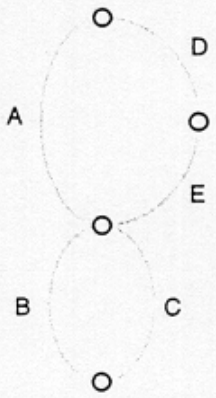

VDD
VA
M3
VB
M4
Vout
VA
M1
VB
M2


VDD
M3
M4
n-well
OUT
M1
M2
GND
VA
VB

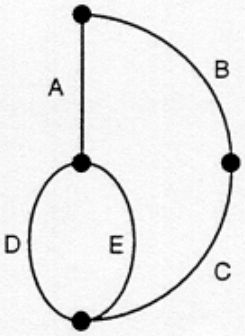

VDD
VA
M3
VB
M4
Vout
VA
M1
VB
M2


VDD
M3
M4
n-well
OUT
M1
M2
GND
VA
VB

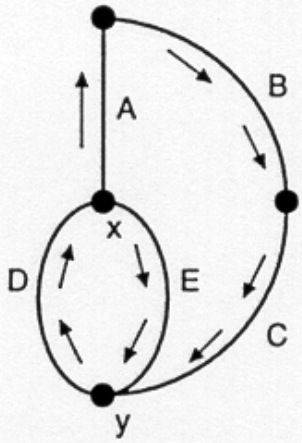




pMOS network graph



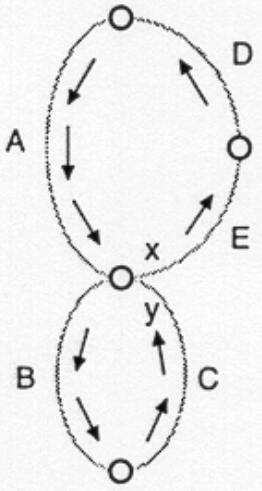
nMOS network graph



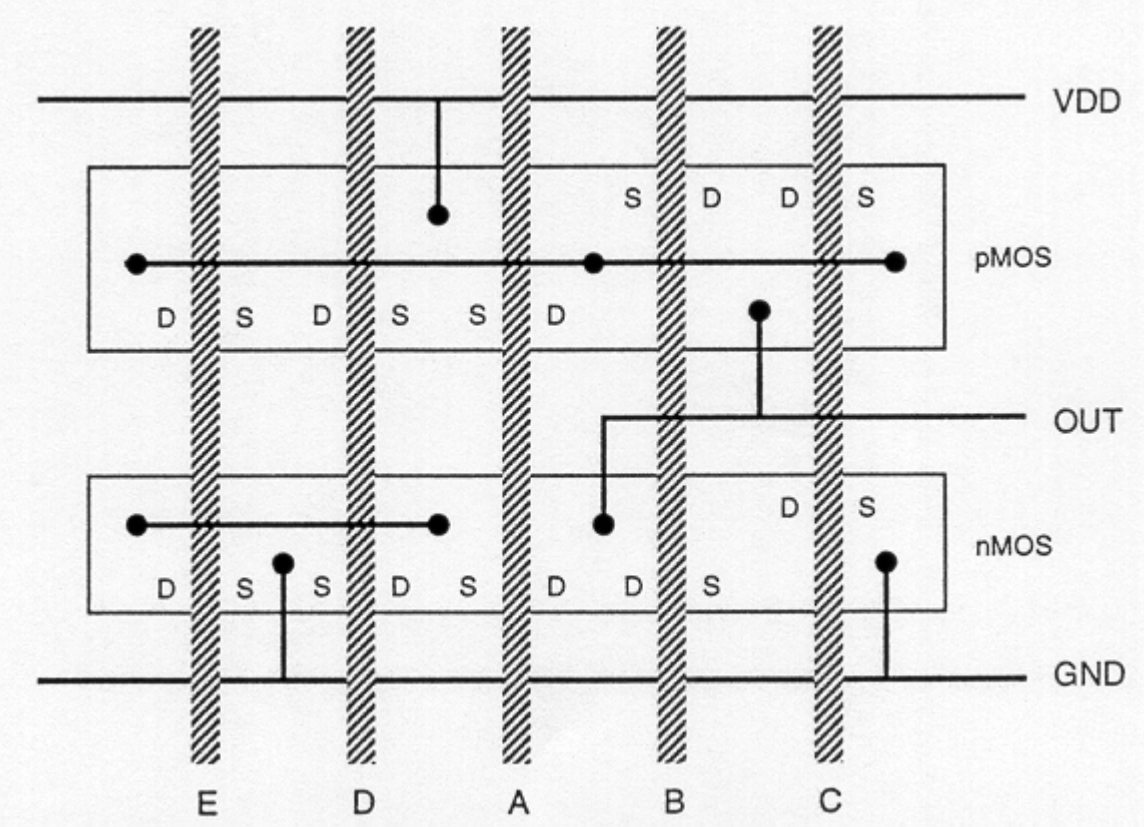
nMOS network graph

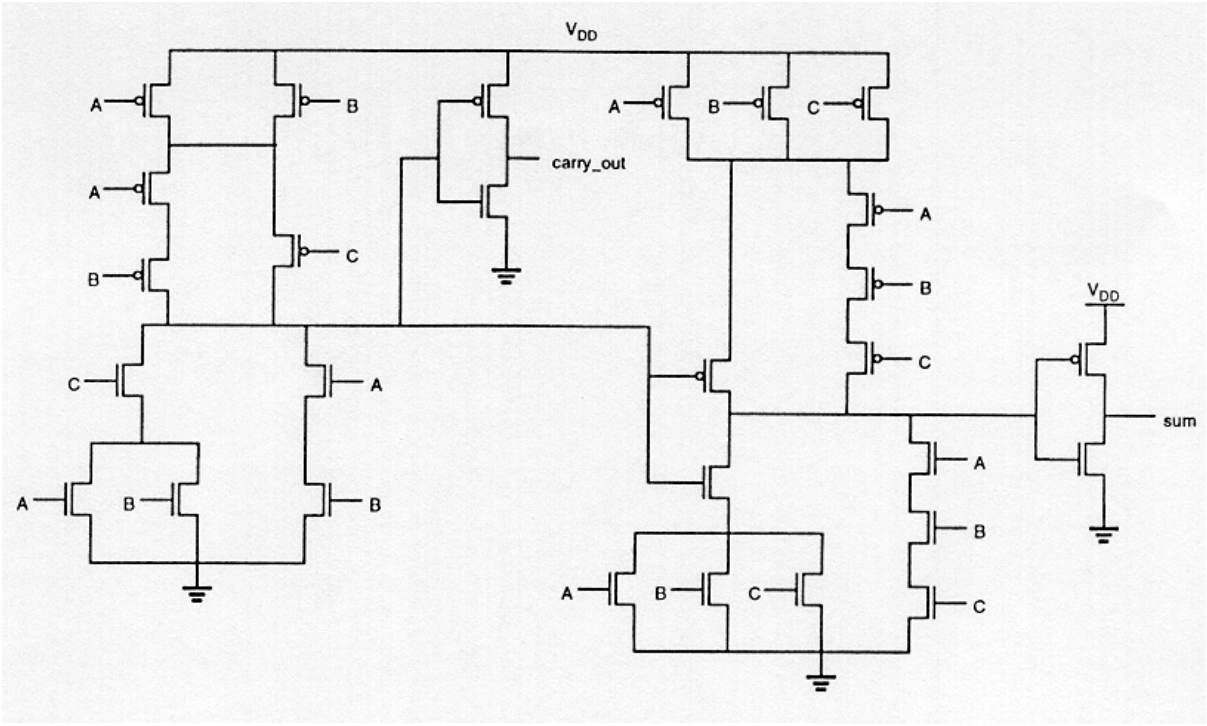
Common Euler path :

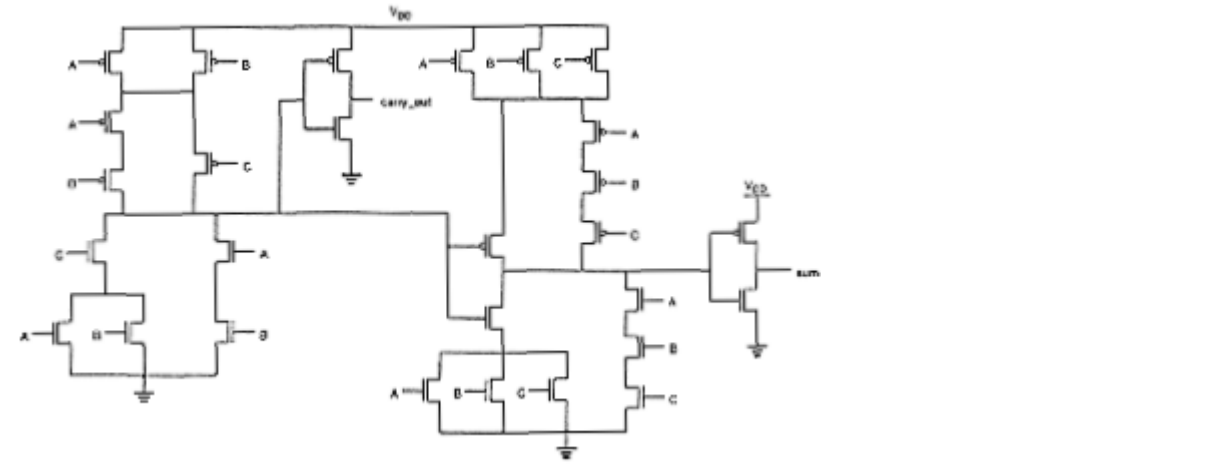
E - D - A - B - C

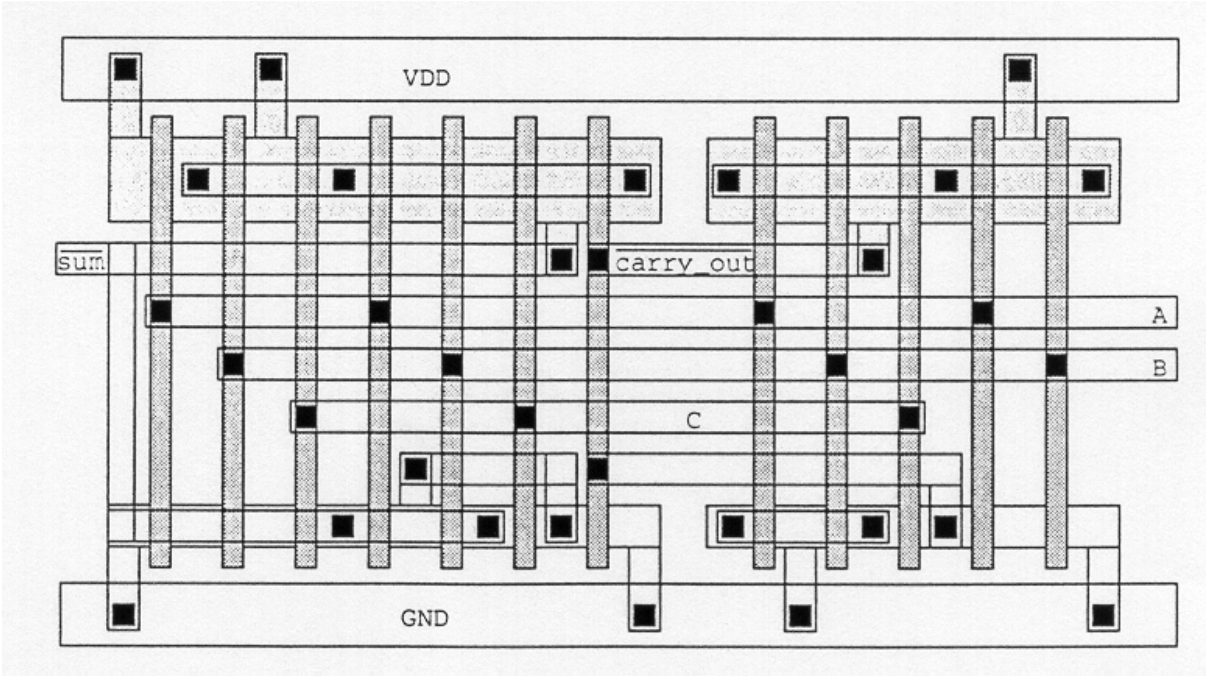


pMOS network graph


VDD
S
D
D
S
pMOS
D
S
D
S
S
D
OUT
D
S
nMOS
D
S
S
D
S
D
D
S
GND
E
D
A
B
C


V_{DD}
A
B
C
carry_out
sum




VDD
sum
carry_out
A
B
C
GND