Q1) Implement the following Function in CMOS using minimum number of transistors:
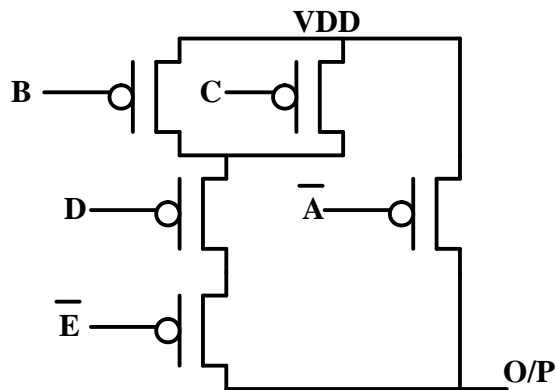
$$F = \overline{A (B + C (D + E (G + H)))}$$

Q2) Implement the following Function in CMOS using minimum number of transistors:

$$F = A (B + \overline{C \cdot D} + E \cdot G)$$

Q3) Re-do Q2 above assuming that inputs are available in true and complement form.

Q4) The following schematic shows the PMOS (PU) block of a CMOS gate. <u>Complete the schematic</u> of the gate (i.e. the NMOS PD block) and **specify the function** implemented by this gate.

Q5) Implement the following logic block in CMOS gates:
   1) Using <u>minimum number of logic levels</u>
   2) Using <u>minimum number of transistors</u>