COE360 – Assignment # 6 (Out of 20)
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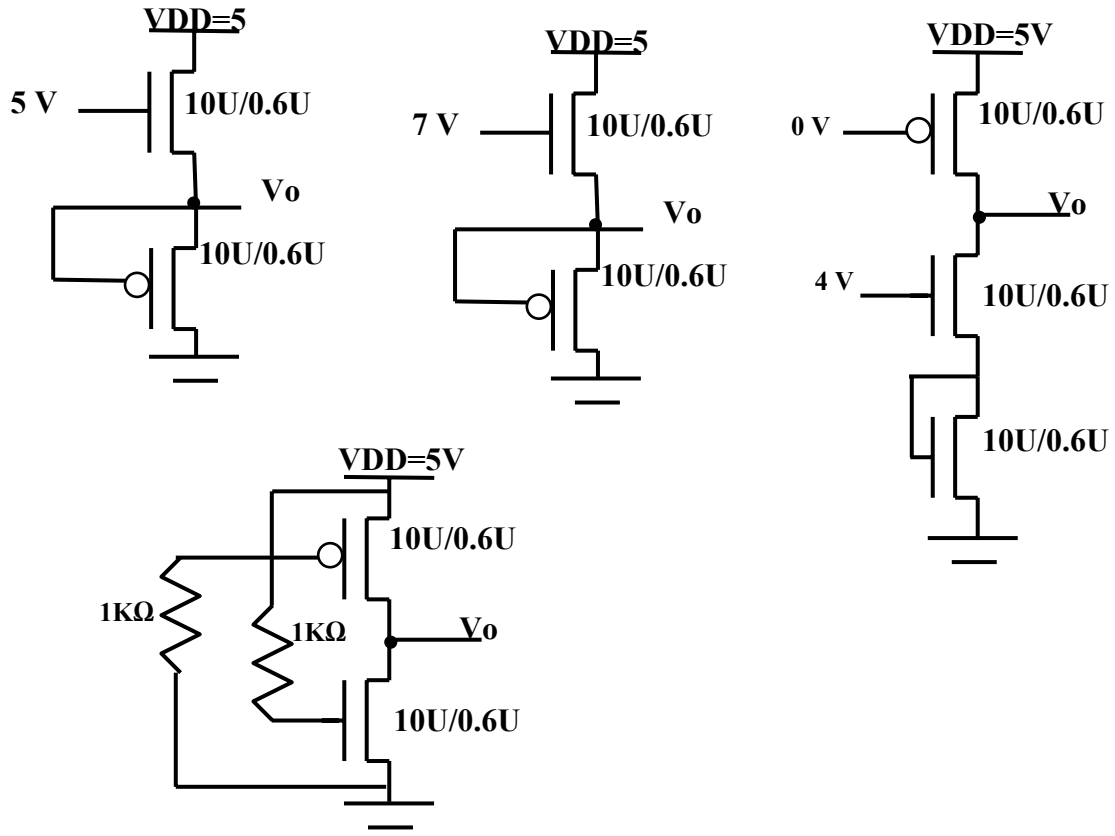
For the problems below submit both the Spice code and the simulation results as hardcopy. Use the AMI0.5U technology with WinSpice.

For all NMOS transistors connect the bulck (i.e. substrate) node to ground

For all PMOS transistors connect the bulck (i.e. substrate) node to VDD

Q1) For the circuits shown below, use WinSpice and the AMI0.5U technology to find Vo.

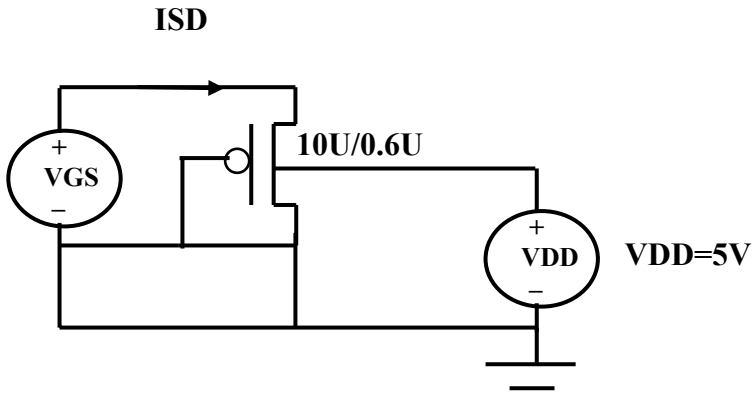
Hint: Use the operating point analysis (op) and print the voltage at Vo.



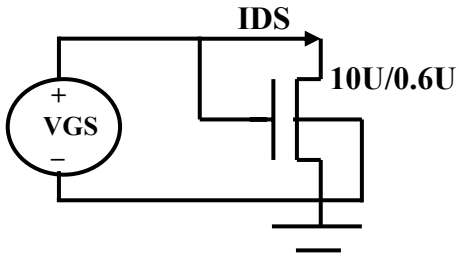
Q2) Use the DC sweep simulation command in Spice to find the saturation currents per micron width ($I_{DSat/\mu m}$) and threshold voltages of NMOS and PMOS devices in the AMI0.5U technology.

Hint: Use the circuits below to obtain I_{DS} versus V_{GS} (in saturation) then from the plot of I_{DS} find V_{th} (when the current starts increasing) and I_{DSat} when $V_{DS} = V_{GS} = 5V$. Divide this value of I_{DSat} by 10 and you'll get $I_{DSat/\mu m}$

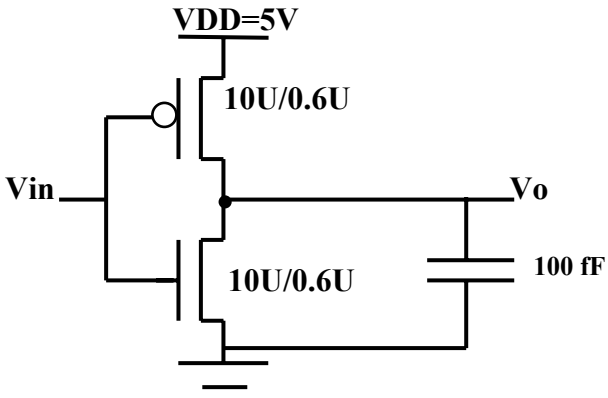
Circuit to measure Vth and ISD of the PMOS transistor



Circuit to measure Vth and ISD of the NMOS transistor



Q3) Find the logical threshold (using DC sweep of Vin) and the average propagation delay (using a pulsed source at Vin and tran analysis) of the CMOS inverter below:



To measure the current in any branch insert a 0v source as shown and print or plot the current through it (i.e. print I(Vt) or plot I(Vt))