KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE-202 – Fundamentals of Computer Engineering
January 13th, 2009 – Major Exam #2

Student Name:
Student Number:
Exam Time: 90 mins

- Do not open the exam book until instructed
- The use of programmable calculators and cell phone calculators is not allowed – only basic calculators are permitted
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

Question No.	Max Points	
1	50	
2	40	
3	50	
4	30	

Total: 170

Q.1) (50 points) Mark the following statements with either TRUE (T) or FALSE (F)

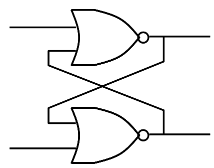
1	The XOR gate is a universal gate since it can implement all basic (AND, OR, NOT) operations.	F
2	A priority encoder has a valid line which indicates whether the output is valid or not.	T
3	Two 2-to-4 line decoders with enable signals can be connected to form a 4-to-16 line decoder.	F
4	A quadruple 4-to-1 line multiplexer has four select lines (S3, S2, S1, S0) select lines and one output line.	F
5	The partial adder circuit is a circuit that adds two bits and generate the sum and carry.	F
6	The decoder circuit has *n* inputs and 2^n outputs.	T
7	The ripple carry adder is built using n parallel half adders with all input bits applied simultaneously to produce the sum.	F
8	The logic diagram of the demultiplexer is identical to that of the decoder with the enable signal.	T
9	An 8-to-1 multiplexer can be used to implement any function of 4 variables with no added logic gates except perhaps for inverters.	T
10	An 2-to-1 multiplexer can be used to implement any function of 3 variables with no added logic gates except perhaps for inverters.	F
11	The 2^n-to-1 multiplexer can be used to implement *n* logic functions with the use of n external OR gates	F
12	The adder logic circuit can be also used to perform 2's complement subtraction	T
13	The carry lookahead adder does not suffer from extended delay to generate the required carry signals unlike the ripple carry adder	T
14	The clocked SR latch is an edge sensitive device.	F
15	The JK flip flop is a memory element that can store two bits.	F
16	For a NOR SR latch, the input 00 and the SR lines lead to an undefined state.	F
17	The master-slave flip-flop consists of two latches connected in series and an inverter.	T

18	A 4-to-16 decoder can be connected to a 16-to-4 encoder to perform BCD to excess-three code conversion without the need for external logic gates.	T
19	A clocked SR latch can not go into the undefined state.	F
20	A positive edge triggered flip-flop means the flip-flop changes state while the clock signal is positive.	F
21	Flip-flops often provide means to set or reset the flip-flop asynchronously regardless of its inputs.	T
22	The average propagation delay for a device is the average of Tsetup and Thold.	F
23	The setup time for a flip-flop is the minimum time required for the input to maintain its level (0 or 1) after the application of the clock transition of the pulse.	F
24	A 3-to-8 line decoder can be used to implement all possible functions of 1, 2, or 3 variables.	T
25	The characteristic equation for a D flip-flop is given by $Q(t+1) = D$.	T

Q.2) (40 points) Choose the most appropriate answer for the following questions:

1. The logic circuit shown represents most closely the architecture of a

   a. <u>Simple Latch</u>
   b. SR Latch with Enable
   c. D Latch with Enable
   d. D Flip-Flop
   e. JK Flip-Flop



2. Which of the following will correctly complete the JK flip-flop truth table shown below?

```
                                                    J K Qn  | Qn+1
                                                    -------|-----
a. 0    b. 0    c. 0    d. 0    e. 1                0 0 0   |  ?
   1       1       0       0       1                0 1 1   |  ?
   1       0       1       1       0                1 0 1   |  ?
   0       0       1       0       1                1 1 1   |  ?
```

(Answer: **d.**)

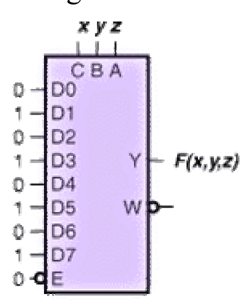
3. Which of the following will correctly complete the D flip-flop truth table shown below?

```
                                                    D Qn  | Qn+1
                                                   ------|-----
a. 1    b. 1    c. 0    d. 0    e. 0                0 0   |  ?
   1       1       0       0       1                0 1   |  ?
   1       0       0       1       1                1 0   |  ?
   1       1       1       1       0                1 1   |  ?
```

(Answer: **d.**)

4. An 8-line to 1-line multiplexer is connected as shown, where output Y = F(x,y,z) and z is the least significant input. Which of the following functions does Y generate?

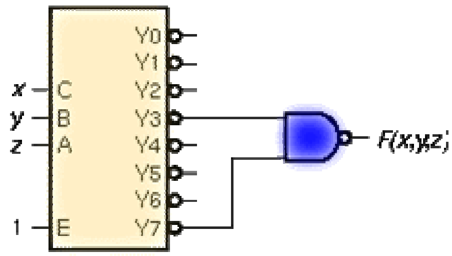
   a) <u>F(x,y,z) = z</u>
   b) F(x,y,z) = y
   c) F(x,y,z) = z'
   d) F(x,y,z) = x
   e) F(x,y,z) = x + y'



5. Which of the following is the correct output expression for an eight to one MUX? (Di is the ith input to the mux while mi is the ith minterm for the selection variables)

   a) Y = D(m0 + m1 + m2 +...+ m7)
   b) <u>Y = D0*m0 + D1*m1 + D2*m2 +...+ D7*m7</u>
   c) Y = m0' + m1' + m2' +...+ m7'
   d) Y = D0*m0' + D1*m1' + D2*m2' +...+ D7*m7'
   e) Y = D*m0 + D*m1 + D*m2 +...+ D*m7

6. A 3-to-8-line decoder is connected as shown. Where x, y and z are inputs (z is the least significant input digit) and F is an output. Which of the following expressions correctly describes F?

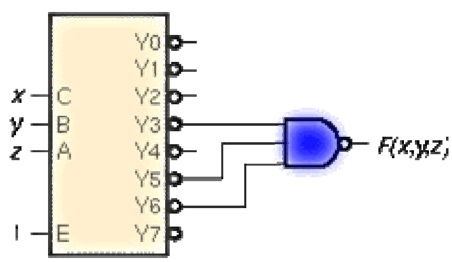


a) F(x,y,z) = z
b) F(x,y,z) = x
c) F(x,y,z) = z'
d) <u>F(x,y,z) = yz</u>
e) F(x,y,z) = x'

7. A circuit which gates one input of data line to one of 2^n output lines is defined as a

a) MUX
b) <u>DeMUX</u>
c) Encoder
d) Decoder
e) ROM

8. A 3-to-8-line decoder is connected as shown, where x, y, and z are inputs (z is the least significant input digit) and F is an output. F = 1 when



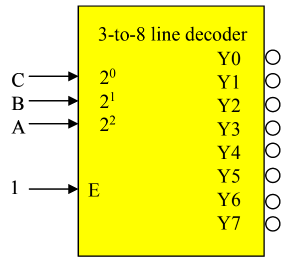
a) All 3 inputs are logical 0
b) 2 out of 3 inputs are logical 0
c) <u>1 out of 3 inputs are logical 0</u>
d) No input is logical 0
e) None of the above

9. A circuit which translates n input lines into an m-bit code word, where n <= 2^m is defined as a

a) MUX
b) DeMUX
c) <u>Encoder</u>
d) Decoder
e) ROM

10. Which of the following correctly describes output Yi (0 to 7) of the 3-to-8-line decoder, where mi is the i^{th} minterm of the three variables applied to the input lines 2^0, 2^1, 2^2, and E is the enable input?

a) Yi = mi*E
b) <u>Yi = (mi*E)'</u>
c) Yi = (mi*E')'
d) Yi = (mi'*E)'
e) Yi = (mi'*E')'



Q.3) (50 points) We would like to design a circuit that adds three bits X, Y and Cin and produces the sum bit S and the carry out bit Cout.

1) (10 points) Write the true table for the functions S and Cout. In your truth table X should be the MSB, and Cin should be the LSB.

2) (10 points) Implement the functions S and Cout using a 3-to-8 decoder.

3) (10 points) Implement the function S using a 2^2-to-1 MUX.

4) (20 points) Implement the function Cout using a 2^1-to-1 MUX.

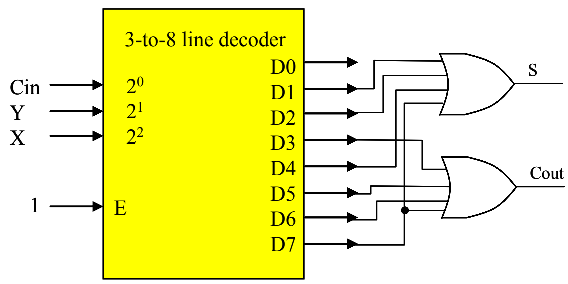
For parts (2), (3), and (4) **<u>DO NOT FORGET TO LABEL</u>** the decoder/MUX pins correctly to correspond to the variables in the truth table.

Solution

(1) The truth table for functions S and Cout is as follows:

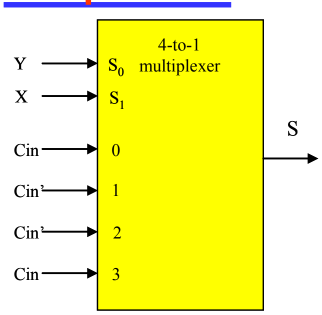
X	Y	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(2) The implementation of functions S and Cout using a 3-to-8 line decoder is as follows:



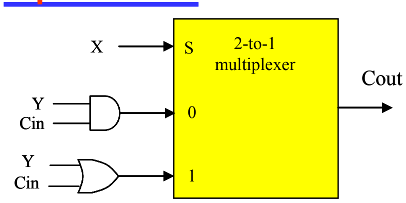
(3) The implementation of the function S using a 4-to-1 MUX is as follows:

X	Y	Cin	S	
0	0	0	0	→ S = Cin
0	0	1	1	
0	1	0	1	→ S = Cin'
0	1	1	0	
1	0	0	1	→ S = Cin'
1	0	1	0	
1	1	0	0	→ S = Cin
1	1	1	1	



(4) The implementation of the function Cout using a 2-to-1 MUX is as follows:

X	Y	Cin	Cout	
0	0	0	0	→ Cout = YCin
0	0	1	0	
0	1	0	0	
0	1	1	1	
1	0	0	0	→ Cout = Y+Cin
1	0	1	1	
1	1	0	1	
1	1	1	1	



Q.4) (30 points) Design a combinational circuit that takes a BCD digit as input represented by the four bits A3A2A1A0 and produces an output F. F should be 1 if the BCD digit is valid (i.e. between 0 and 9, inclusive) and should be zero otherwise. Implement the circuit as a sum of products.

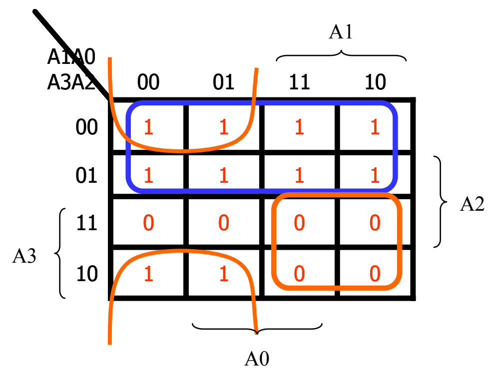
Solution:

The truth table for the required is as shown. Note the function F(A3, A2, A1, A0) is equal to 1 for binary codes 0000, 0001, …,and 1001. The function F(A3, A2, A1, A0) is equal to 0 otherwise.

The corresponding K-map is as shown. Therefore, F(A3, A2, A1, A0) = A3' + A2'A1'.

The circuit implementation is as shown also in figure below.

Digit	A3	A2	A1	A0	F
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	0



F = A3' +A2'A1'