

HW# 4 Solution

Q.1. Consider a technology library containing the following cells:

Cell	Area Cost
$INV(x1) = x1'$	1
$NAND2(x1, x2) = (x1 x2)'$	2
$NAND3(x1, x2, x3) = (x1 x2 x3)'$	3
$NOR2(x1, x2) = (x1 + x2)'$	2
$AOI21(x1, x2, x3) = ((x1 x2) + x3)'$	3
$OAI21(x1, x2, x3) = ((x1+x2) x3)'$	3

(i) Show the **pattern trees** of the library cells using **NAND2** and **INV** as base functions. Assume that symmetric representations do not need to be stored.

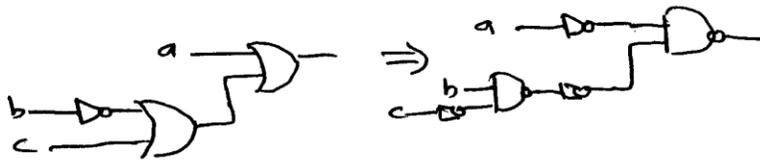
	Cell	gate	pattern tree	cost
t1	INV			1
t2	NAND2			2
t3	NAND3			3
t4	NOR2			2
t5	AOI21			3
t6	OAI21			3

- (ii) Decompose the function $f = a + b' + c$ using NAND2 and INV as base functions into all possible **non-symmetric decompositions**. Then, **map** the decomposed circuits using the given library and determine the decomposition that leads to a **lower area cost**.

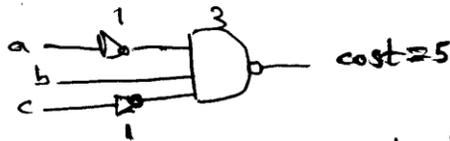
The function $f = a + b' + c$ can be decomposed into 2-input OR gates by one of the following decompositions:



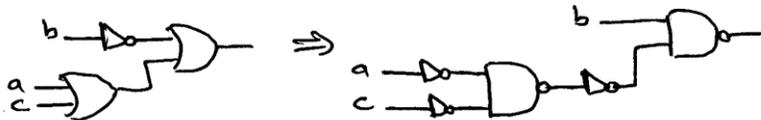
The first and second decompositions have the same structure and will lead to a solution of the same cost. So, we will consider mapping the first and third decompositions.



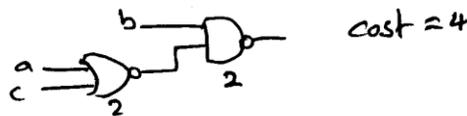
The minimum solution for mapping this decomposition has a cost of 5 as shown below:



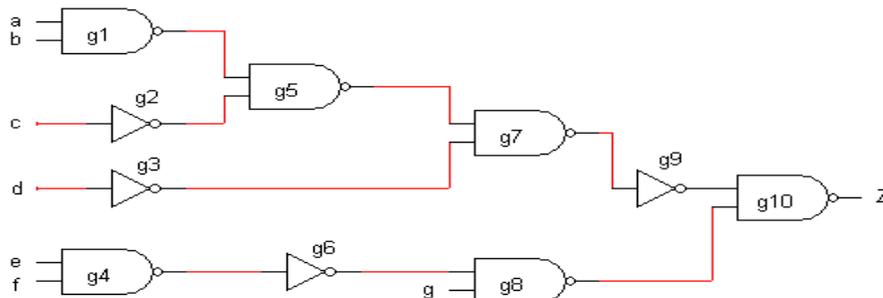
Next, we consider the third decomposition.



The minimum solution for mapping this decomposition has a cost of 4 as shown below:

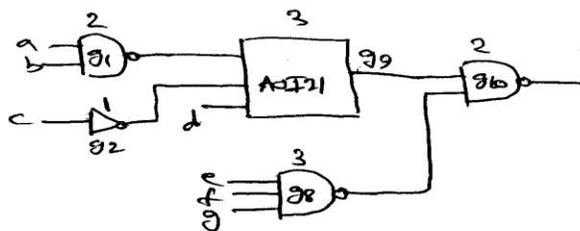


(iii) Using the dynamic programming approach, **map** the circuit given below using the given library into the **minimum area** cost solution. Inputs are $\{a, b, c, d, e, f, g\}$ and output is $\{Z\}$.



vertex	Match	gate	cost
θ_1	t_2	Nand ₂ (a,b)	2
θ_2	t_1	INV(c)	1
θ_3	t_1	INV(d)	1
θ_4	t_2	Nand ₂ (e,f)	2
θ_5	t_2	Nand ₂ (θ_1, θ_2)	$2+2+1=5$
θ_6	t_1	INV(θ_4)	$1+2=3$
θ_7	t_2	Nand ₂ (θ_5, θ_3)	$2+5+1=8$
θ_8	t_2	Nand ₂ (θ_6, θ_7)	$2+3=5$
	t_3	Nand ₃ (e,f,g)	<u>3</u>
θ_9	t_1	INV(θ_7)	$1+8=9$
	t_5	AOI21(θ_1, θ_2, d)	$3+2+1=\underline{6}$
θ_{10}	t_2	Nand ₂ (θ_9, θ_8)	$2+6+3=\underline{\underline{11}}$
	t_3	Nand ₃ ($\theta_5, \theta_3, \theta_8$)	$3+5+1+3=12$

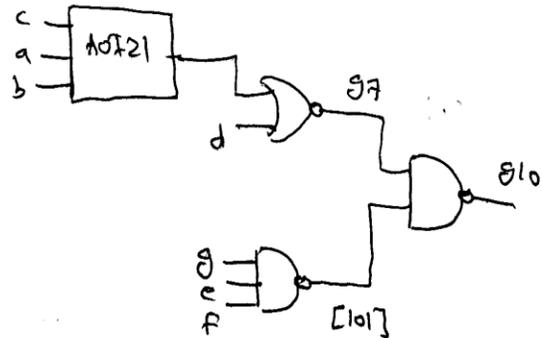
Thus, the minimum cost is 11 and the mapped solution is shown below:



- (iv) Using the given library, use the SIS command *read_libray q1.lib* to read the library. Then, map the circuit to the library using the sis command *map -s -m 0*. Compare your solution to the solution obtained in (iii). You can save the mapped circuit using the sis command *write_blif -n*. Why do you think the solution obtained by SIS is better than your solution?

The solution achieved by SIS is given below with a total area of 10.

```
.model hw4q1_081.blif
.inputs a b c d e f g
.outputs g10
.default_input_arrival 0.00 0.00
.default_output_required 0.00 0.00
.default_input_drive 0.20 0.20
.default_output_load 1.00
.default_max_input_load 999.00
.gate NAND3 a=g b=e c=f O=[101]
.gate AOI21 a=c b=a c=b O=g5
.gate NOR2 a=d b=g5 O=g7
.gate NAND2 a=[101] b=g7 O=g10
.end
```



The obtained solution is better than the solution we obtained because SIS uses an additional optimization technique by inserting pairs of inverters at each line in the subject graph and then finding an optimal mapping of the subject graph. Any mapped pair of inverters can then be eliminated. Using this technique it is possible to obtain a better mapping of the given network.

- (v) Assuming **Boolean matching**, determine the number of ROBDD's that need to be stored in the cell library for each of the following cells. Justify your answer.

a. $f = a b + a c + b c$

Since $a, b,$ and c are all symmetric
 $C_3 = \{ (a,b,c) \} \Rightarrow \# \text{ ROBDD's } = 1$

b. $f = a b c + a' b' d$

we have 2 binate variables $\{a, b\}$
 and 2 unate variables $\{c, d\}$
 variables a and b are symmetric.
 $\Rightarrow \# \text{ ROBDD's } = 2$

Q.2. Consider the incompletely-specified FSM that has 6 states, two inputs and one output, represented by the following state table:

Present State	Next State, Output			
	00	01	11	10
S1	S2, 0	-, -	S5, 1	-, -
S2	S1, 0	S3, -	-, -	-, -
S3	S3, -	S1, 1	S5, -	S4, 1
S4	-, -	S2, -	S1, -	-, -
S5	S3, -	S2, 1	-, 0	S6, -
S6	S6, 1	S1, -	S2, -	S5, -

(i) Determine the incompatible and the compatible states along with their implied pairs.

Compatibility Table

S2	✓				
S3	(S2, S3)	(S1, S3)			
S4	(S1, S5) X	(S2, S3)	(S1, S2) (S1, S5) X		
S5	X	(S1, S3) (S2, S3)	(S1, S2) (S4, S6)	✓	
S6	X	X	(S2, S5) (S4, S5)	(S1, S2)	(S1, S2) (S3, S6)
	S1	S2	S3	S4	S5

The incompatible states are:
 $(S1, S4)$, $(S1, S5)$, $(S1, S6)$, $(S2, S6)$, $(S3, S4)$

The compatible states with their implied pairs:

- $(S1, S2)$
- $(S1, S3) \Leftarrow (S2, S3)$
- $(S2, S3) \Leftarrow (S1, S3)$
- $(S2, S4) \Leftarrow (S2, S3)$
- $(S2, S5) \Leftarrow (S1, S3), (S2, S3)$
- $(S3, S5) \Leftarrow (S1, S2), (S4, S6)$
- $(S3, S6) \Leftarrow (S2, S5), (S4, S5)$
- $(S4, S5)$
- $(S4, S6) \Leftarrow (S1, S2)$
- $(S5, S6) \Leftarrow (S1, S2), (S3, S6)$

(ii) Compute the maximal compatible classes along with their implied state pairs.

Maximal compatible classes:

we assign for every state s_i variable x_i .
From the incompatible state pairs we have

$$\begin{aligned} & (\bar{x}_1 + \bar{x}_4)(\bar{x}_1 + \bar{x}_5)(\bar{x}_1 + \bar{x}_6)(\bar{x}_2 + \bar{x}_6)(\bar{x}_3 + \bar{x}_4) \\ &= (\bar{x}_1 + \bar{x}_4\bar{x}_5)(\bar{x}_1 + \bar{x}_6)(\bar{x}_2 + \bar{x}_6)(\bar{x}_3 + \bar{x}_4) \\ &= (\bar{x}_1 + \bar{x}_4\bar{x}_5\bar{x}_6)(\bar{x}_2 + \bar{x}_6)(\bar{x}_3 + \bar{x}_4) \\ &= (\bar{x}_1\bar{x}_2 + \bar{x}_1\bar{x}_6 + \bar{x}_2\bar{x}_4\bar{x}_5\bar{x}_6 + \bar{x}_4\bar{x}_5\bar{x}_6)(\bar{x}_3 + \bar{x}_4) \\ &= \bar{x}_1\bar{x}_2\bar{x}_3 + \bar{x}_1\bar{x}_2\bar{x}_4 + \bar{x}_1\bar{x}_3\bar{x}_6 + \bar{x}_1\bar{x}_4\bar{x}_6 \\ & \quad + \bar{x}_2\bar{x}_4\bar{x}_5\bar{x}_6 + \bar{x}_4\bar{x}_5\bar{x}_6 \end{aligned}$$

Thus, we have 5 maximal compatible classes as follows:

$$\begin{aligned} \bar{x}_1\bar{x}_2\bar{x}_3 & : c_1 : (s_4, s_5, s_6) \Leftarrow (s_1, s_2), (s_3, s_6) \\ \bar{x}_1\bar{x}_2\bar{x}_4 & : c_2 : (s_3, s_5, s_6) \Leftarrow (s_1, s_2), (s_4, s_6), (s_2, s_5), (s_4, s_5) \\ \bar{x}_1\bar{x}_3\bar{x}_6 & : c_3 : (s_2, s_4, s_5) \Leftarrow (s_2, s_3), (s_1, s_3) \\ \bar{x}_1\bar{x}_4\bar{x}_6 & : c_4 : (s_2, s_3, s_5) \Leftarrow (s_1, s_3), (s_1, s_2), (s_4, s_6) \\ \bar{x}_4\bar{x}_5\bar{x}_6 & : c_5 : (s_1, s_2, s_3) \end{aligned}$$

(iii) Reduce the state table into the minimum number of states and show the reduced state table.

If we consider the maximal compatible classes to find a minimum cover, we will get either $c_1 c_2 c_3 c_5$ or $c_1 c_2 c_4 c_5$ i.e. a minimum of four reduced states.

However, the state table can be reduced into 3 states by using the following

cover: $(s_1, s_2, s_3), (s_4, s_5), (s_6)$

The reduced state table is:

Present state	Next state, output			
	00	01	11	10
s_{123}	$s_{123}, 0$	$s_{123}, 1$	$s_{45}, 1$	$s_{45}, 1$
s_{45}	$s_{123}, -$	$s_{123}, 1$	$s_{123}, 0$	$s_6, -$
s_6	$s_6, 1$	$s_1, -$	$s_2, -$	$s_5, -$

Q.3. Consider the incompletely-specified FSM that has 4 states, two inputs and two outputs, represented by the following state table:

Product	Input	Present State	Next State	Output
P1	10	S1	S2	11
P2	00	S2	S2	11
P3	01	S2	S2	00
P4	00	S3	S2	00
P5	10	S2	S1	11
P6	10	S3	S1	11
P7	00	S1	S1	--
P8	01	S3	S0	00
P9	11	S1	S1	10
P10	11	S3	S3	01
P11	11	S0	S0	11

(i) Assuming the following constraints, $S0 = S1 \text{ OR } S3$, and that the code of S2 is covered by all other state codes, the state table can be reduced into the table shown below. Using implicant merging, covering and disjunctive relations show step by step how you can obtain the reduced state table given below.

Input	Present State	Next State	Output
-0	S1, S2	S2	11
10	S2, S3	S1	11
00	S1	S1	--
01	S3	S0	00
11	S0, S1	S1	10
11	S0, S3	S3	01

- P5 and P6 can be merged using implicant merging into the following row:

10	S2, S3	S1	11
----	--------	----	----
- P1 can be changed to:

-0	S1	S2	11
----	----	----	----

if we impose the covering constraint $S1 \supseteq S2$
- P2 can be changed to:

-0	S2	S2	11
----	----	----	----

if we impose the covering constraint $S1 \supseteq S2$
- These two rows can now be merged to:

-0	S1, S2	S2	11
----	--------	----	----

- P_3 can be changed to:

$$0 - \begin{matrix} s_2 & s_2 & 00 \end{matrix}$$
- P_4 can be changed to:

$$0 - \begin{matrix} s_3 & s_2 & 00 \end{matrix}$$

if we impose the constraint that $s_0 \geq s_2$
- Now P_3 and P_4 can be merged into:

$$0 - \begin{matrix} s_2, s_3 & s_2 & 00 \end{matrix}$$
- If we impose the disjunctive constraint that $s_0 = s_1$ or s_3 , then P_{11} can be removed and P_9 and P_{10} changed to:

$$P_9 \quad 11 \quad s_0, s_1 \quad s_1 \quad 10$$

$$P_{10} \quad 11 \quad s_0, s_3 \quad s_3 \quad 01$$
- Finally, the following row can be eliminated if it is assumed that the code of s_2 is covered by all other codes i.e. the code of s_2 is the all-0 code:

$$0 - \begin{matrix} s_2, s_3 & s_2 & 00 \end{matrix}$$

(ii) Show the encoding constraint matrix and compute all the seed dichotomies of the encoding constraint matrix. Then, eliminate seed dichotomies that violate the given covering and disjunctive constraints.

Encoding constraint matrix:

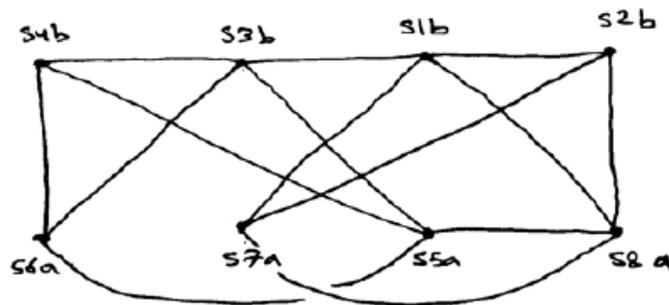
$$A = \begin{bmatrix} 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix}$$

Seed Dichotomies:

- | | |
|---|---|
| $s_{1a} : (s_1, s_2), (s_0) \times$
$s_{1b} : (s_0), (s_1, s_2)$ | $s_{2a} : (s_1, s_2), (s_3) \times$
$s_{2b} : (s_3), (s_1, s_2)$ |
| $s_{3a} : (s_2, s_3), (s_0) \times$
$s_{3b} : (s_0), (s_2, s_3)$ | $s_{4a} : (s_2, s_3), (s_1) \times$
$s_{4b} : (s_1), (s_2, s_3)$ |
| $s_{5a} : (s_0, s_1), (s_2)$
$s_{5b} : (s_2), (s_0, s_1) \times$ | $s_{6a} : (s_0, s_1), (s_3)$
$s_{6b} : (s_3), (s_0, s_1) \times$ |
| $s_{7a} : (s_0, s_3), (s_1)$
$s_{7b} : (s_1), (s_0, s_3) \times$ | $s_{8a} : (s_0, s_3), (s_2)$
$s_{8b} : (s_2), (s_0, s_3) \times$ |

- (iii) Compute all the prime dichotomies and eliminate those that violate the disjunctive constraints.

Prime Dichotomies:



- $P_1 : (s1b, s2b, s7a, s8a) : (s_0, s_3), (s_1, s_2)$
 $P_2 : (s3b, s4b, s5a, s6a) : (s_0, s_1), (s_2, s_3)$
 $P_3 : (s5a, s8a) : (s_0, s_1, s_3), (s_2)$
 $P_4 : (s1b, s3b) : (s_0), (s_1, s_2, s_3)$

Note that P_4 violates the disjunctive constraint and has to be discarded. Also, P_3 violates the disjunctive constraint if we assume 2-bits encoding.

- (iv) Find a state encoding satisfying the given constraints. Verify that your encoding satisfies all the constraints.

A minimum cover is P_1 and P_2 which results in the following state encoding

state	code
s_0	1 1
s_1	0 1
s_2	0 0
s_3	1 0

Note that the disjunctive constraint $s_0 = s_1 \text{ OR } s_3$ is satisfied since $11 = 01 \text{ OR } 10$. Also, the code of $s_2 = 00$, which is covered by all other codes.

Also, $s_1 \cdot s_2 = 0-$, which does not intersect with other codes.

$s_2 \cdot s_3 = -0$, which does not intersect with other codes.

$s_0 \cdot s_1 = -1$, which does not intersect with other codes.

$s_0 \cdot s_3 = 1-$, which does not intersect with other codes.

- (v) Using K-MAP, obtain the equations for the output and flip-flops. Compare your solution to the solution obtained by running the SIS command *stg_to_network* using the state codes obtained in (iii).

$I_1 I_0$	$F_1 F_0$	00	01	11	10
00	0	0	-	0	
01	0	-	-	1	
11	-	0	1	1	
10	0	0	-	0	

$$D_1 = I_0 F_1$$

$I_1 I_0$	$F_1 F_0$	00	01	11	10
00	0	1	-	0	
01	0	-	-	1	
11	-	1	1	0	
10	1	0	-	1	

$$D_0 = \bar{I}_1 F_0 + I_0 F_0 + \bar{I}_1 I_0 F_1 + I_1 I_0 \bar{F}_0$$

$I_1 I_0$	$F_1 F_0$	00	01	11	10
00	1	-	-	0	
01	0	-	-	0	
11	-	1	1	0	
10	1	1	-	1	

$$O_1 = I_1 \bar{I}_0 + \bar{I}_0 \bar{F}_1 + F_0$$

$I_1 I_0$	$F_1 F_0$	00	01	11	10
00	1	-	-	0	
01	0	-	-	0	
11	-	0	1	1	
10	1	1	-	1	

$$O_0 = \bar{I}_0 \bar{F}_1 + I_1 F_1$$

of literals = 21 literals

The circuit resulting based on the stg_to_network command is as follows:

```
sis> read_blif hw4q3_081.blif
sis> stg_to_network
sis> print
  [0] = IN_0 IN_1 LatchOut_v2 + IN_0' IN_1 LatchOut_v2
  [1] = IN_0 IN_1' LatchOut_v3' + IN_0' IN_1 LatchOut_v2 + IN_0' LatchOut_v3 + IN_1
LatchOut_v3
  {OUT_0} = IN_0 IN_1' LatchOut_v3' + IN_1 LatchOut_v3 + IN_1' LatchOut_v2'
  {OUT_1} = IN_0 IN_1 LatchOut_v2 + IN_0 IN_1' LatchOut_v3' + IN_1' LatchOut_v2'
sis> print_stats
hw4q3_081    pi= 2  po= 2  nodes= 4    latches= 2
lits(sop)= 31 #states(STG)= 4
```

Note that the number of literals is more than what we have obtained using K-map because the objective here is to minimize the number of products and not the number of literals. To optimize the number of literals, we need to do single output optimization using the command stg_to_network -e 2 which produces the following circuit:

```
sis> read_blif hw4q3_081.blif
sis> stg_to_network -e 2
sis> print
  [0] = IN_1 LatchOut_v2
  [1] = IN_0 IN_1' LatchOut_v3' + IN_0' IN_1 LatchOut_v2 + IN_0' LatchOut_v3
+ IN_1 LatchOut_v3
  {OUT_0} = IN_0 IN_1' + IN_1' LatchOut_v2' + LatchOut_v3
  {OUT_1} = IN_0 LatchOut_v2 + IN_1' LatchOut_v2'
sis> print_stats
hw4q2_081    pi= 2  po= 2  nodes= 4    latches= 2
lits(sop)= 21 #states(STG)= 4
```

- (vi) Perform state assignment using the program nova by running the SIS command *state_assign nova*. Compare the obtained solution to your solution in (v) in terms of number of literals.

The result produced is as follows which is worse than the solution obtained in (v).

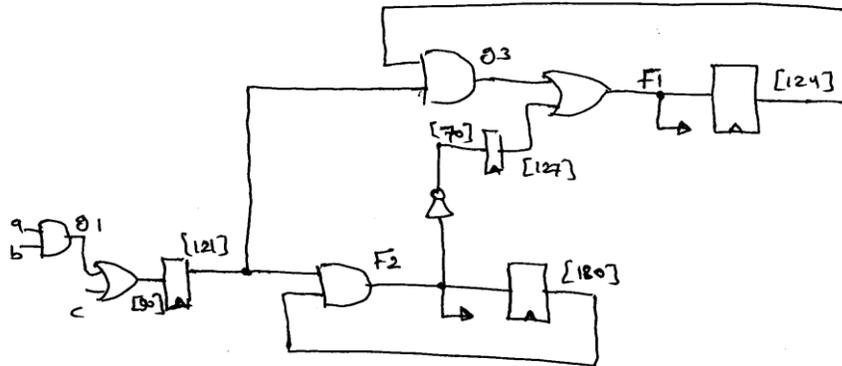
```
sis> read_blif hw4q3_081.blif
sis> state_assign nova
Running nova, written by Tiziano Villa, UC Berkeley
sis> print
  {OUT_0} = IN_0 IN_1' LatchOut_v2' + IN_1 LatchOut_v2 LatchOut_v3 + IN_1' LatchOut_v2 +
IN_1' LatchOut_v3' + LatchOut_v2 LatchOut_v3'
  {OUT_1} = IN_0 LatchOut_v2' + IN_1' LatchOut_v2 + IN_1' LatchOut_v3' + LatchOut_v2
LatchOut_v3'
  v4.0 = IN_0 IN_1' LatchOut_v2' + IN_0' IN_1 LatchOut_v3 + IN_0' LatchOut_v2 + IN_1
LatchOut_v2 LatchOut_v3 + LatchOut_v2 LatchOut_v3'
  v4.1 = IN_0 LatchOut_v2' + IN_0' LatchOut_v2 + IN_1 LatchOut_v2 LatchOut_v3
sis> print_stats
hw4q3_081    pi= 2  po= 2  nodes= 4    latches= 2
lits(sop)= 40 #states(STG)= 4
```



```

.mlatch dff_re D=[70] Q=[127] NIL 3
.mlatch dff_re D=f2 Q=[130] NIL 3
.gate and2 1A=a 1B=b O2=g1
.gate or2 1A=c 1B=g1 O1=[90]
.gate and2 1A=[121] 1B=[124] O2=g3
.gate inv 1A=f2 O=[70]
.gate or2 1A=g3 1B=[127] O1=f1
.gate and2 1A=[121] 1B=[130] O2=f2
.end

```



Note that the number of registers obtained by SIS is different due to our description of the circuit having the fanout connecting to G5 not coming directly from F2. This is why we were able to minimize the number of registers more than what the tool could have done. If we have connected F2 to a buffer representing S2 and then let S2 fanout, SIS will obtain the same solution we have obtained.