

COE 561, Term 101
Digital System Design and Synthesis
HW# 3

Due date: Tuesday, Dec. 14

Q.1. Consider the following function:

$$x = a d e + a f + a' b' c f + b c d e + b c f + c d' e' f$$

- (i) Compute all the kernels of X using the recursive kernel computation algorithm. Show all the steps.
- (ii) Compute all the kernels of X based on matrix representation. Compare your answer to the result obtained in (i).
- (iii) Use the sis command *print_kernel* and compare the kernels obtained to your answers in (i) and (ii).
- (iv) Find a good factor of X . Assume that input variables are sorted in lexicographic order. Determine the number of literals obtained. Compare your solution with the result obtained by running the sis commands *factor -g x; print_factor; print_stats -f*.

Q.2. Consider the following function:

$$x = a b c d + a b c' d' + a b' e + a b' f + a' b e + a' b f + a' b' c d + a' b' c' d' + c e' f + d e' f$$

- (i) Compute all double-cube divisors of x along with their bases and their weights. Show only double-cube divisors that have non-empty bases.
- (ii) Apply the fast extraction algorithm based on extracting double-cube divisors along with complements or single-cube divisors with two-literals. Show all steps of the algorithm. Determine the number of literals saved. Compare your solution with the result obtained by running the sis commands *fx*.

Q.3. Consider the logic network defined by the following expressions:

$$\begin{aligned} X &= A + C; \\ Y &= A X + X' B; \\ Z &= Y + X; \end{aligned}$$

Inputs are {A, B, C} and output is {Z}.

- (i) Compute the CDC set for the cut at the inputs of circuit Y.

- (ii) Compute the ODC set for node Y.
- (iii) Simplify the function of Y using both its ODC and CDC.
- (iv) Apply the sis command *full_simplify* and compare the solution obtained with your obtained solution based in (iii).

Q.4. Consider the logic network defined by the following expressions:

$$g = a b$$

$$h = a' b'$$

$$i = g + h$$

$$j = c d$$

$$k = i j e$$

$$l = i j f$$

$$x = k + l$$

Inputs are {a, b, c, d, e, f} and output is {x}. Assume that the delay of a gate is related to the number of its inputs. Also, assume that the input data-ready times are zero except for input a, which is equal to 2.

- (i) Draw the logic network graph and compute the data ready times and slacks for all vertices in the network.
- (ii) Determine the **maximum propagation delay** and the **topological critical path**.
- (iii) Suggest an implementation of the function *x* to reduce the delay of the circuit. What is the **maximum propagation delay** after the modified implementation?