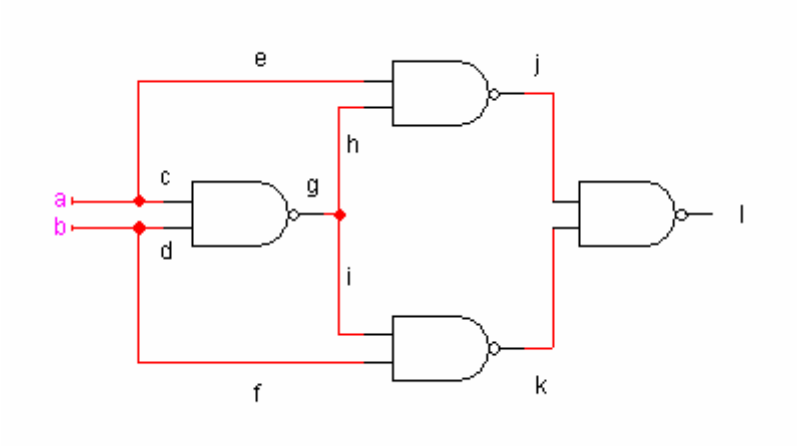
COE 571 Digital System Testing

Term 072

HW# 1

Due date: Wednesday, March 19

Q.1. Consider the circuit shown below:



(i) Find all the test vectors that detect the single stuck-at fault g stuck-at-1.

(ii) Find all the test vectors that detect the multiple stuck-at fault {e stuck-at-1, i stuck-at-0}.

(iii) Find all the test vectors that detect the AND bridging fault between lines a and b.

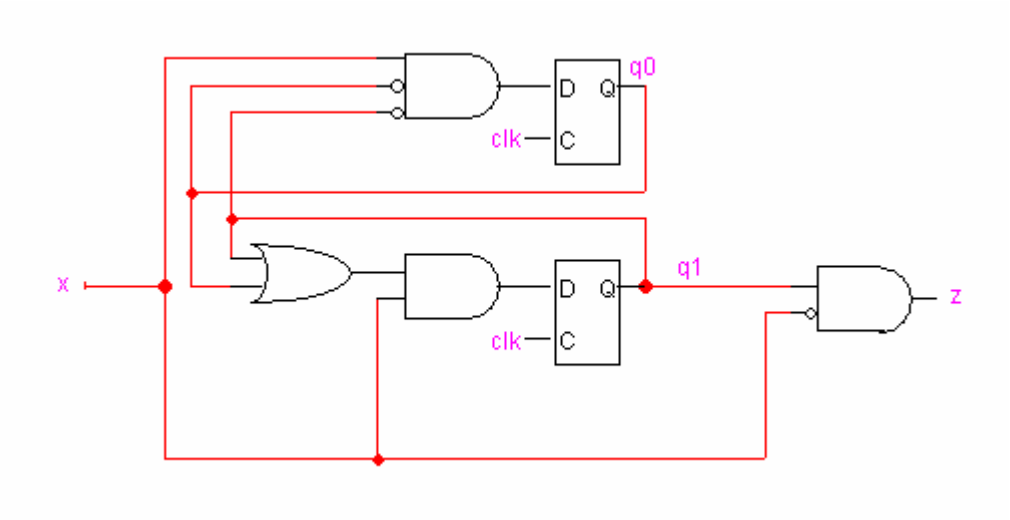
(iv) Starting with injecting faults on each line in the circuit, perform fault collapsing using fault equivalence relation.

(v) Determine the additional faults that could be removed using dominance relations.

(vi) Starting with the set of faults based on the checkpoint theorem (Theorem 4.2), perform fault collapsing using the equivalence and dominance relations. Compare the set of collapsed faults to what you obtained in (v).

(vii) Perform fault collapsing using HITEC. Compare the collapsed fault set to what you obtained in (iv) & (v).

Q.2. Consider the sequential circuit shown below, where z is a primary output and x is a primary input:



(i) Show an iterative array model of four time frames for this circuit.

(ii) Does the circuit have a synchronizing sequence? If yes, find one with the shortest length.

(iii) Derive a test sequence for detecting the fault z s-a-0. Verify your result by fault simulation using PROOFS.

(iv) Determine whether the fault x s-a-1 is detectable, strongly detectable, partially testable or redundant. Check whether the fault can be detected by HITEC or not and comment on the answer.